Digital Electronic Circuits

Architecture and circuit implementation of Mixed signal systems

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0.1 Summary of syllabus

Objective of this course

1. The circuit implementation of the signal processing procedure is shown by the concrete examples, especially analog-to-digital converter and digital-to-analog converter design.
2. You will learn semi-custom design methods with hardware description language (HDL). Following this, you may get started with the design of a custom LSI and FPGA (Field Programmable Gate Array) which have it's own distinctive features.

Schedule

1. Guidance for this subject
2. Laplace transform and Z transform
3. Transfer function
4. Digital and analog circuit implementation 1
5. Digital and analog circuit implementation 2
6. Oversampling converters
7. Nyquist rate converters
8. Quiz
9. Introduction of hardware description language
10. Example of HDL coding
11. HDL simulation (workshop)
12. Logic synthesis (workshop)
13. Place and Route (workshop)
14. Verification of your design (workshop)
15. Specification of your custom LSI or micro-art (workshop)
16. Submission of the report

References

- For students who wants to learn the practical CMOS analog mixed-signal circuit design
  - R. Jacob Baker, CMOS: Mixed-Signal Circuit Design, 2nd Edition, ISBN 978-0-470-29026-2, Wiley-IEEE Press (2009)
- Course wares
  - http://jaco.ec.t.kanazawa-u.ac.jp/edu/
  - http://cmosedu.com/
- The course material for the design project is available on the web site.
  - http://jaco.ec.t.kanazawa-u.ac.jp/edu/digi/lab2/

Requirements to pass through

- Passing mark in the total score is over 60% for each quarter.
- Digital electronic circuits A (Lecture)
  - Assignment: 40%
  - Final exam (Quiz): 60%
- Digital electronic circuits B (Lab course)
  - Attendance rate: 40%
  - Submission of the data of your design: 60%

0.3 Demarcation between analog and digital?

Advantages and disadvantages of technology scaling

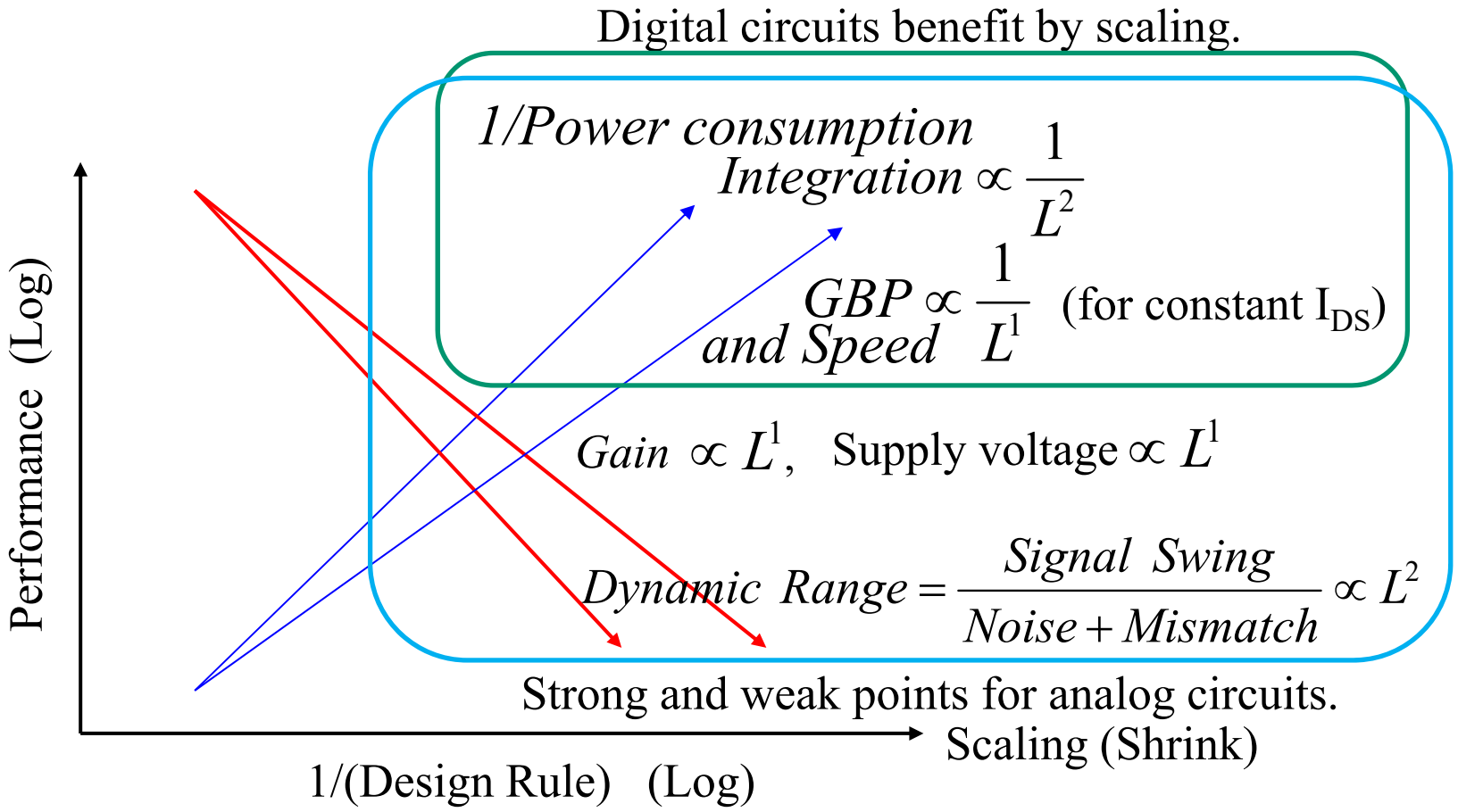


Figure of merit (FOM) of analog circuits

- Before ITRS2004 edition:

  FOM was defined for each category of circuits.
  - LNA: Low noise amplifier
  - VCO: Voltage controlled oscillator
  - PA: Power amplifier
  - ADC: Analog-to-Digital converter
  - SerDes(SERializer/DESerializer)

$$FOM_{LNA} = \frac{G \cdot IIP3 \cdot f}{(NF - 1) \cdot P}$$

$$FOM_{VCO} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\} \cdot P}$$

$$FOM_{PA} = P_{out} \cdot G_p \cdot PAE \cdot f^2$$

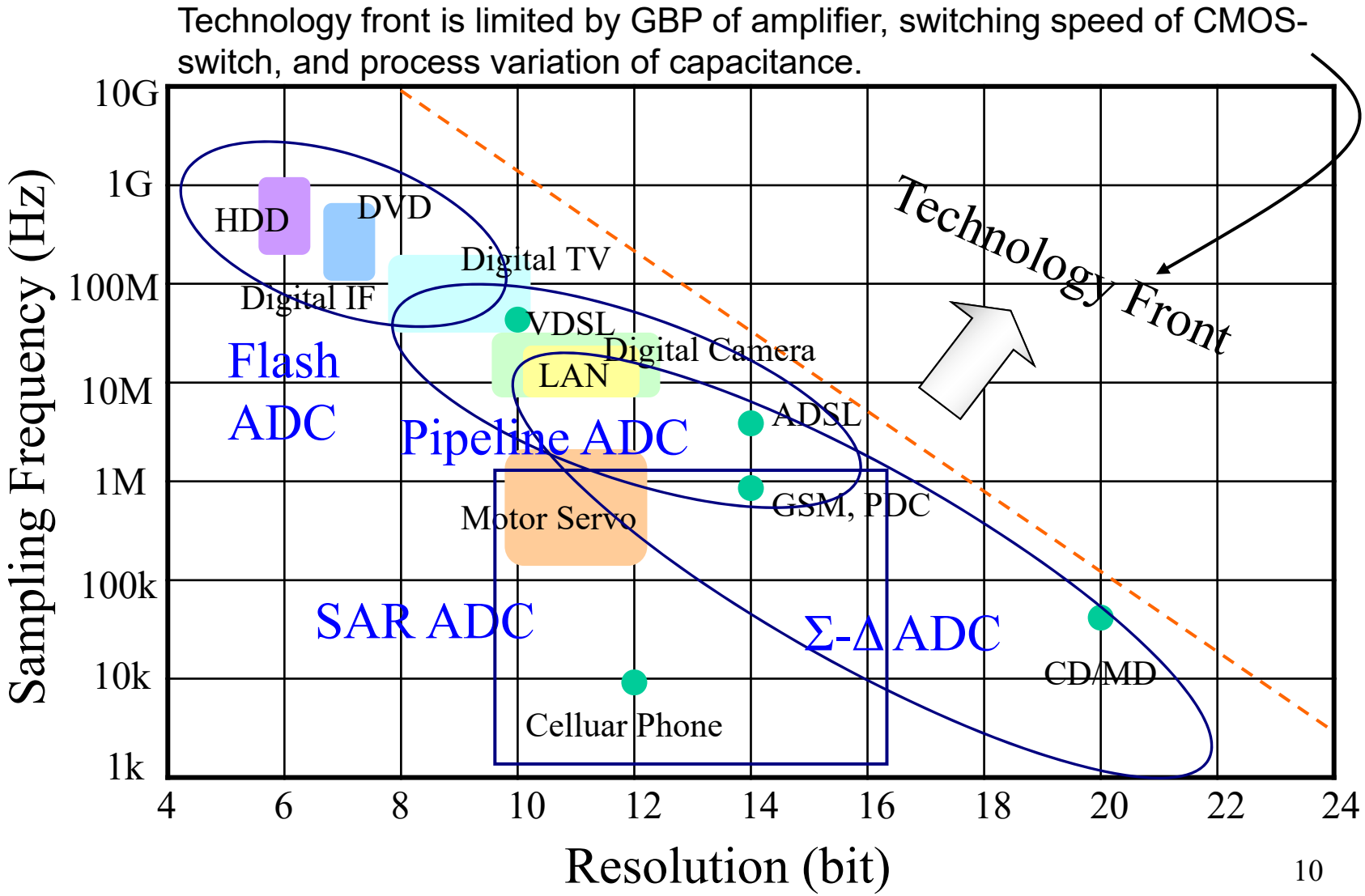
$$FOM_{ADC} = \frac{(2^{ENOB_0}) \cdot f_S}{P}$$

$$FOM_{SerDes} = \frac{R_B \cdot R_{MuxDeMux}}{P}$$

P : Power consumption
IIP3: Third Order Input Intercept Point
NF : Noise figure
L: Spurious power
PAE: Power efficiency

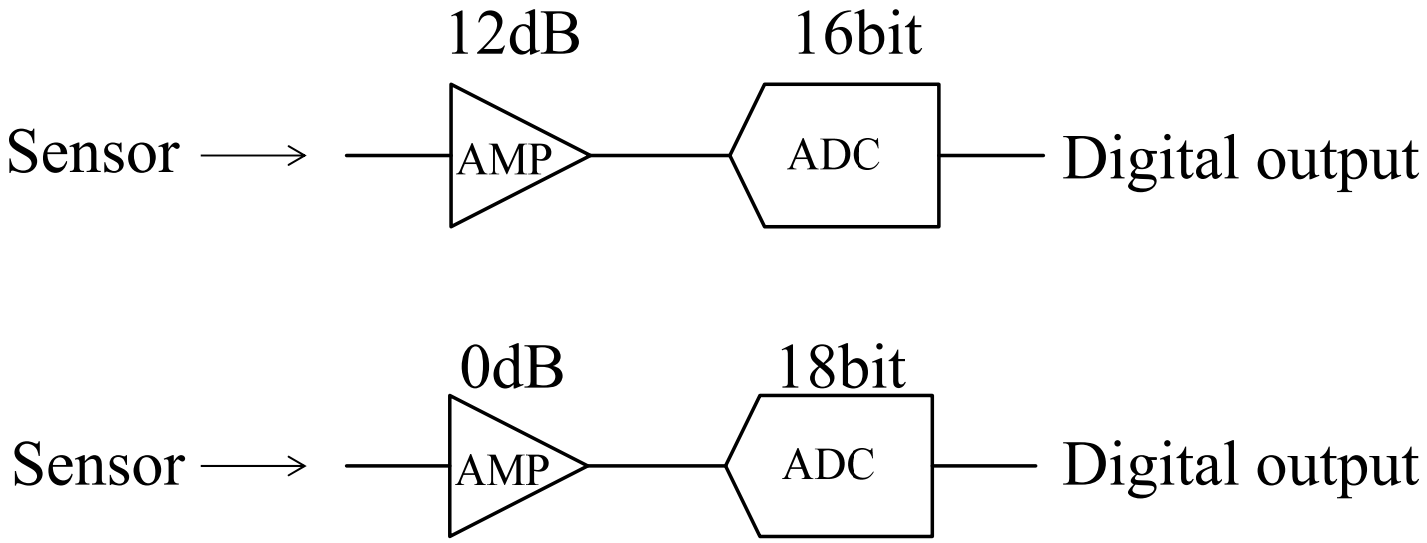
$ENOB_0$: Effective number of bits
f_S : Sampling frequency
R_B: Data Rate
$R_{MuxDeMux}$: Bit count of parallel data

Performance of ADC architecture



Quiz

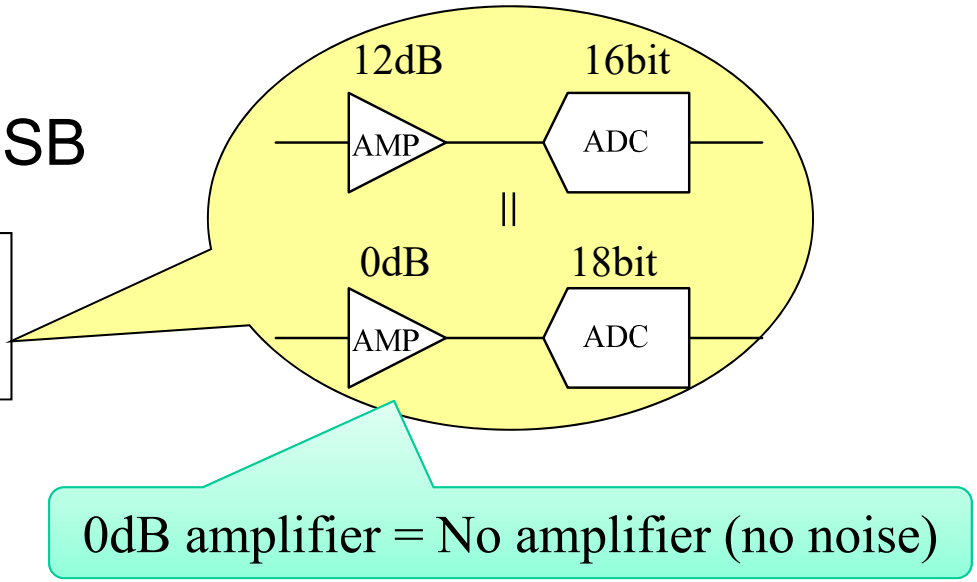
Which circuit is better for a sensitivity and a signal-to-noise ratio?



Suggested answer

Equivalent gain for LSB

1bit ≅ 6.02dB



Why is the increment of 1bit equivalent with the amplification of 6dB (2 times)?

Suggested answer

Maximum number of N-bit binary code = 2^N -1
Dynamic range of N-bit binary code system = (2^N -1)/1
Maximum number of (N+1)-bit binary code = 2^{N+1} -1
Dynamic range of (N+1)-bit binary code system = (2^{N+1} -1)/1

Then, the amplitude of signal that is equivalent for the differential dynamic range between (N+1)-bit and N bit system is corresponding to (2^{N+1} -1)/ (2^N -1) ≒ 2 ≒ 6.02dB

Note that this calculation is made on a condition of M = 0 (no noise shaping) and OSR = 1 (no oversampling). More precise analysis is shown in next slide.

Speed = Accuracy = Gain

SNR for quantization noise and ENOB(Effective number of bits) in oversampling condition

$$SNR_{\max}[dB] = 6.02 \cdot N + 1.76 - 20 \cdot \log[\frac{\pi^M}{\sqrt{2 \cdot M + 1}}] + (20 \cdot M + 10) \log OSR$$

$$ENOB[bit] = 1 + \frac{1}{6.02}[(20 \cdot M + 10) \log OSR - 20 \log(\frac{\pi^M}{\sqrt{2 \cdot M + 1}})]$$

M : Order of noise-shaping transfer function

OSR: Oversampling ratio

Example

Speed ⟶ Accuracy ⟶ Gain

M = 0, OSR = 128, then ENOB = 4.5[bit], ΔSNR_{max} = 27[dB]

M = 1, OSR = 128, then ENOB = 10.6[bit], ΔSNR_{max} = 64[dB]

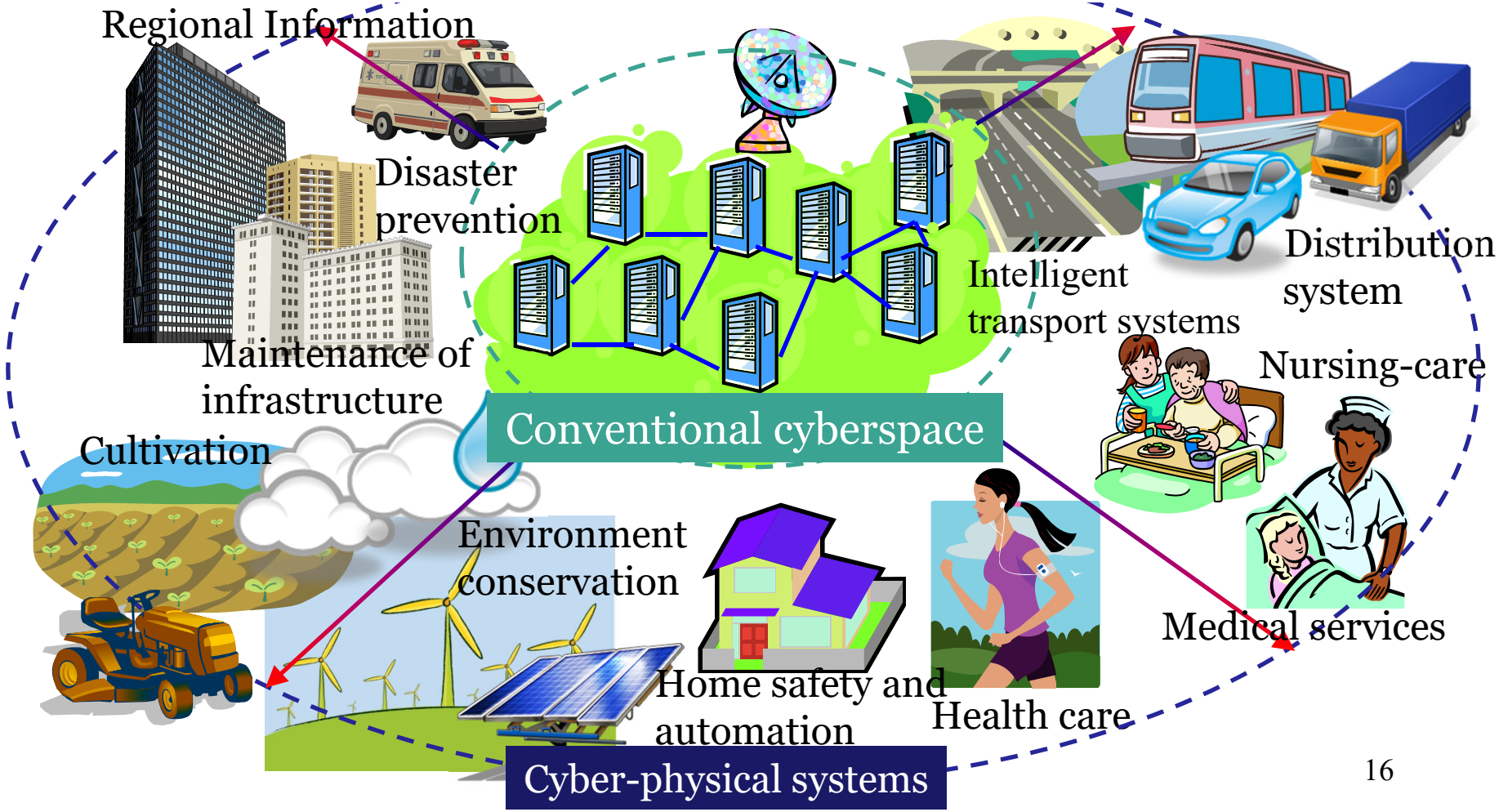
NOTE: The theoretical base will be discussed later.

0.2 Introduction

Growing information technology toward a real world and an dailv life

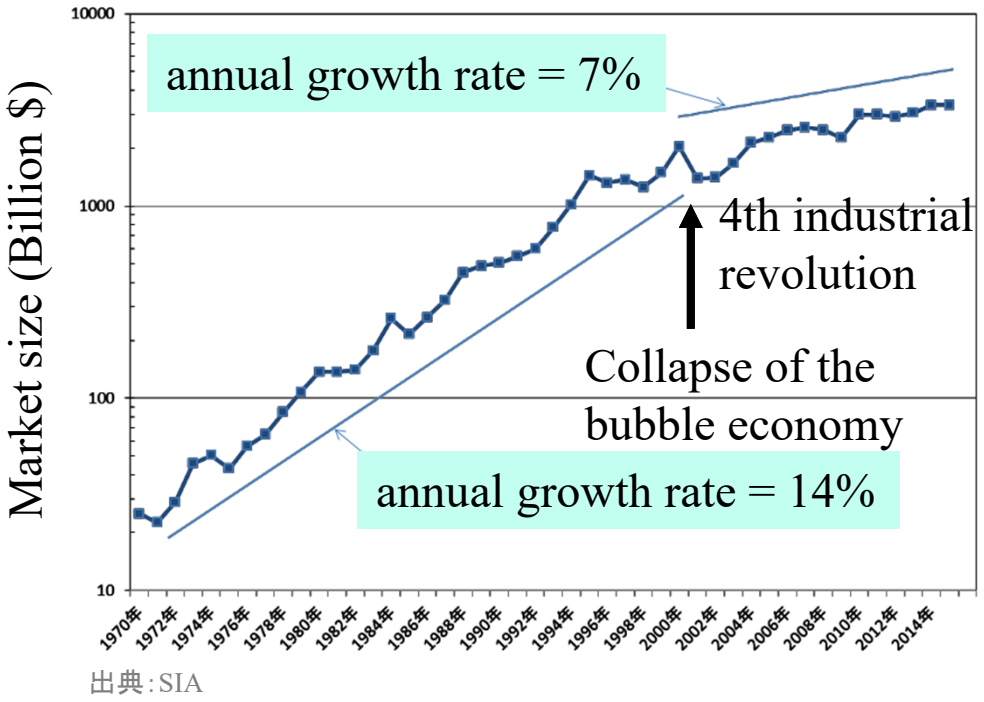
Keywords: Wireless communication, Energy Harvesting, Sensor integration

An analog mixed signal (AMS) LSI is fundamental to advanced electronic systems.



Growing semiconductor market

Japanese people should revise the wrong perspective on the semiconductor economy.



出典：SIA

2018 = $4,100 Billion

2.6%

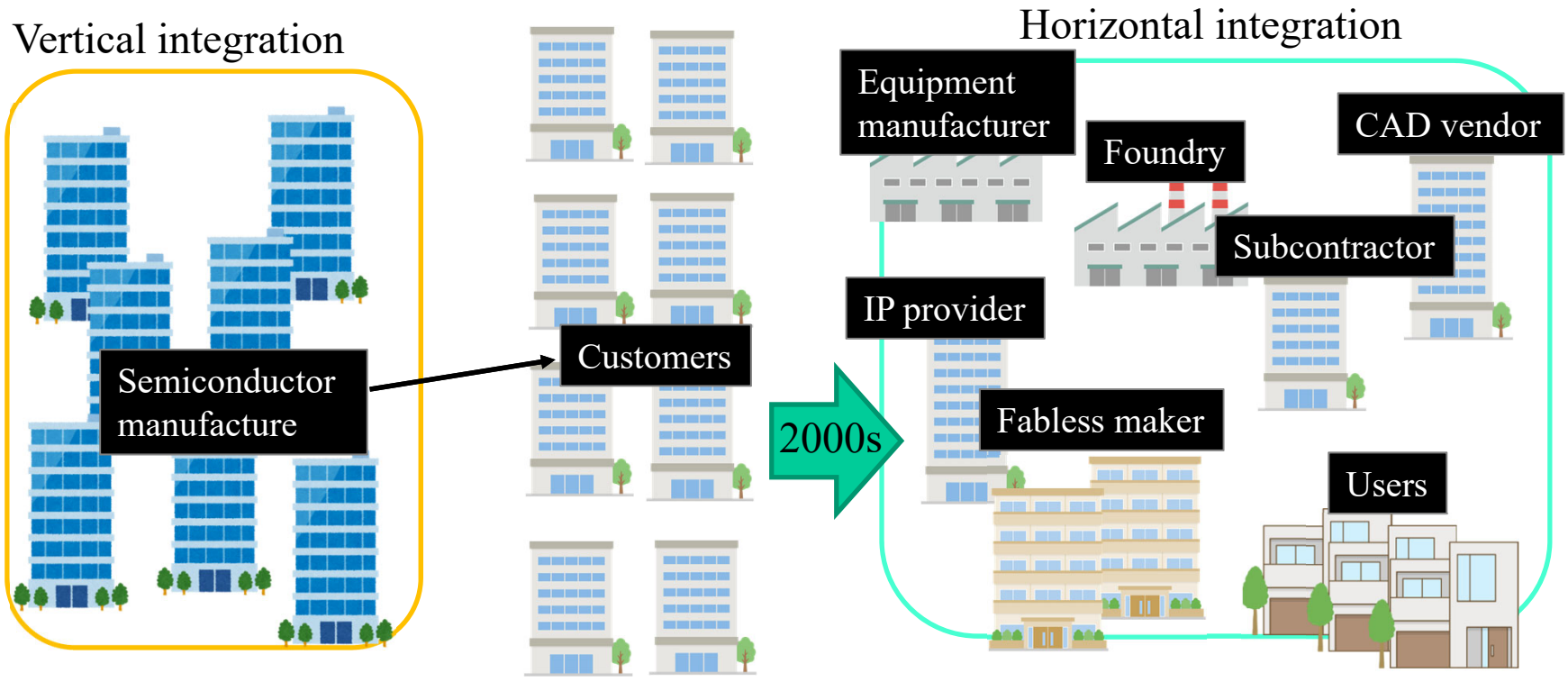
17%

4.3%

Recent trends of technology drivers

- AI processor (non-von Neumann computers)
- Nano-power devices (Energy harvesting)
- Integrated sensors (Bio-chip, human-sensory, Ultra-high precision)
- Ultra-high-speed & Terra-storage (Big data)

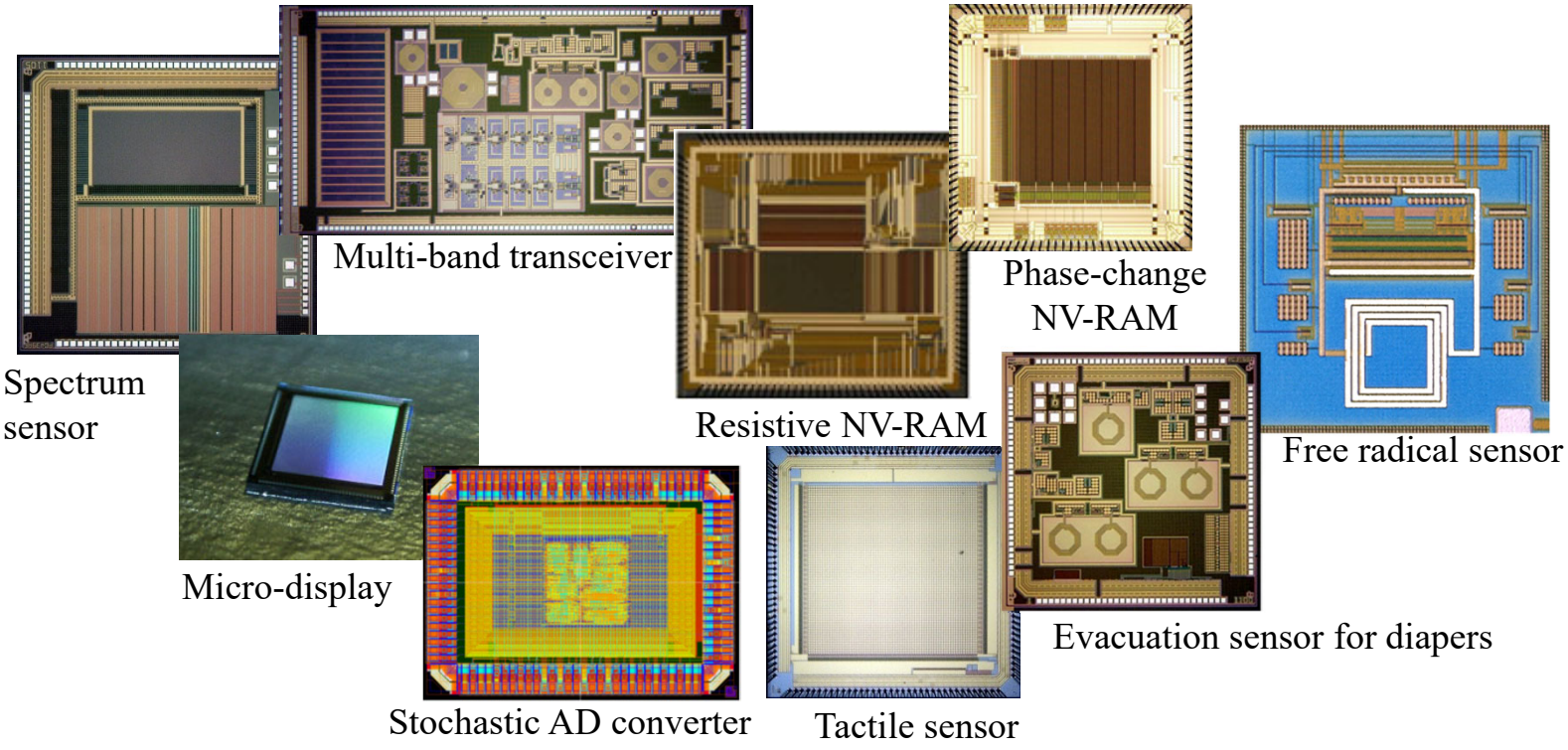
Transformation of industrial structure



Product Supply → Oligopoly

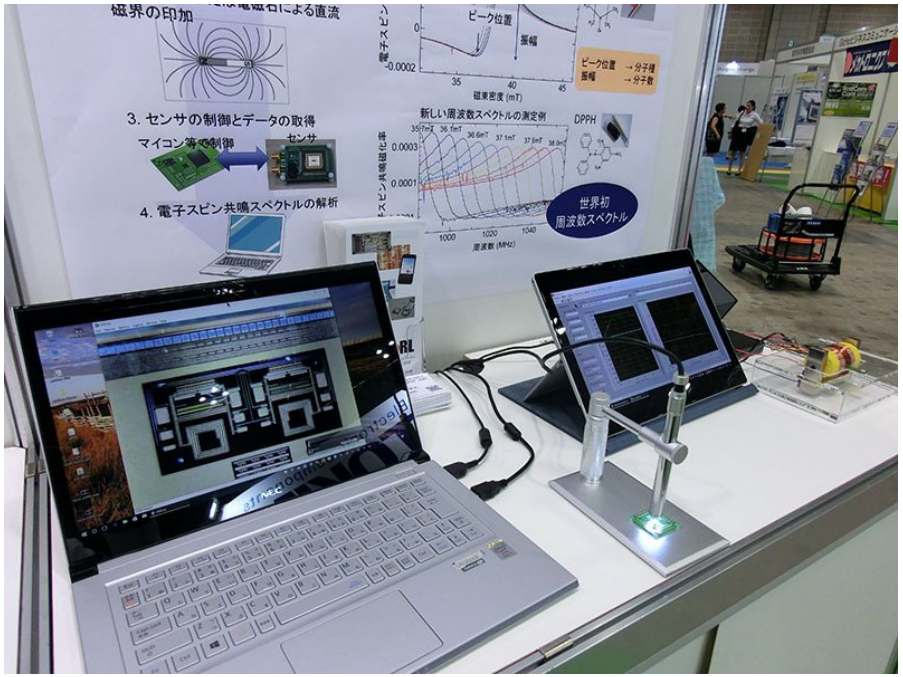
Service providing →
Various product demand

Semiconductor technology designed by users in the new era



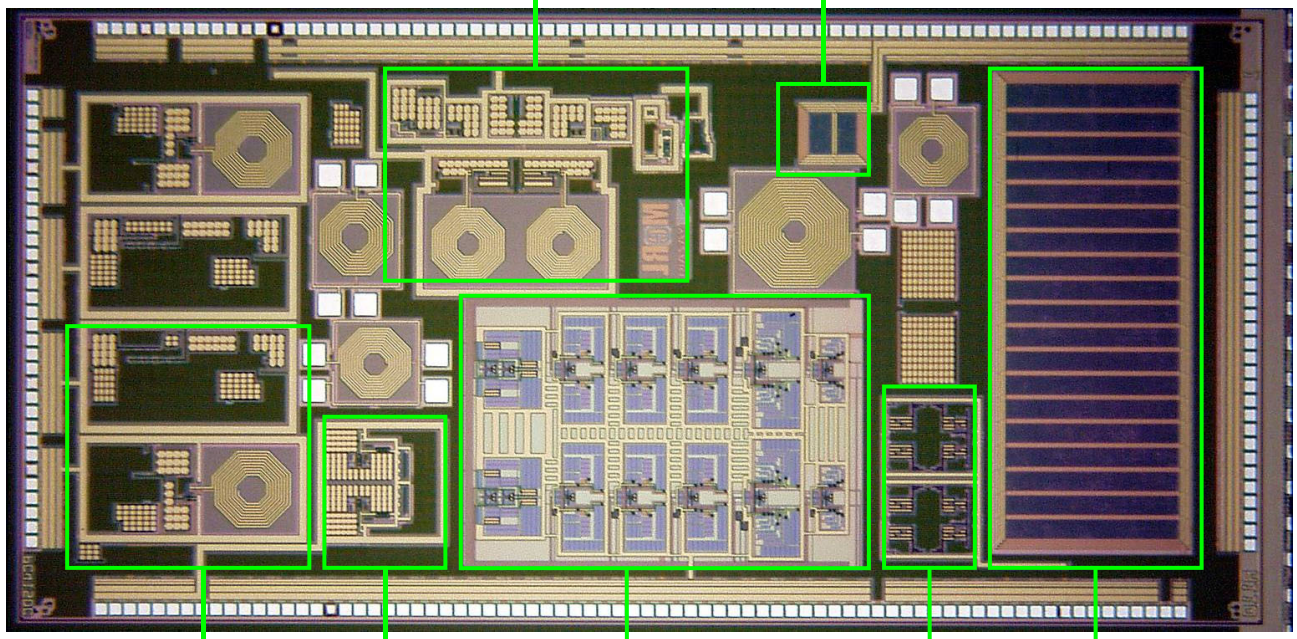
Development examples in Kanazawa University

IoT devices powered by thin film solar cell (Innovation Japan)

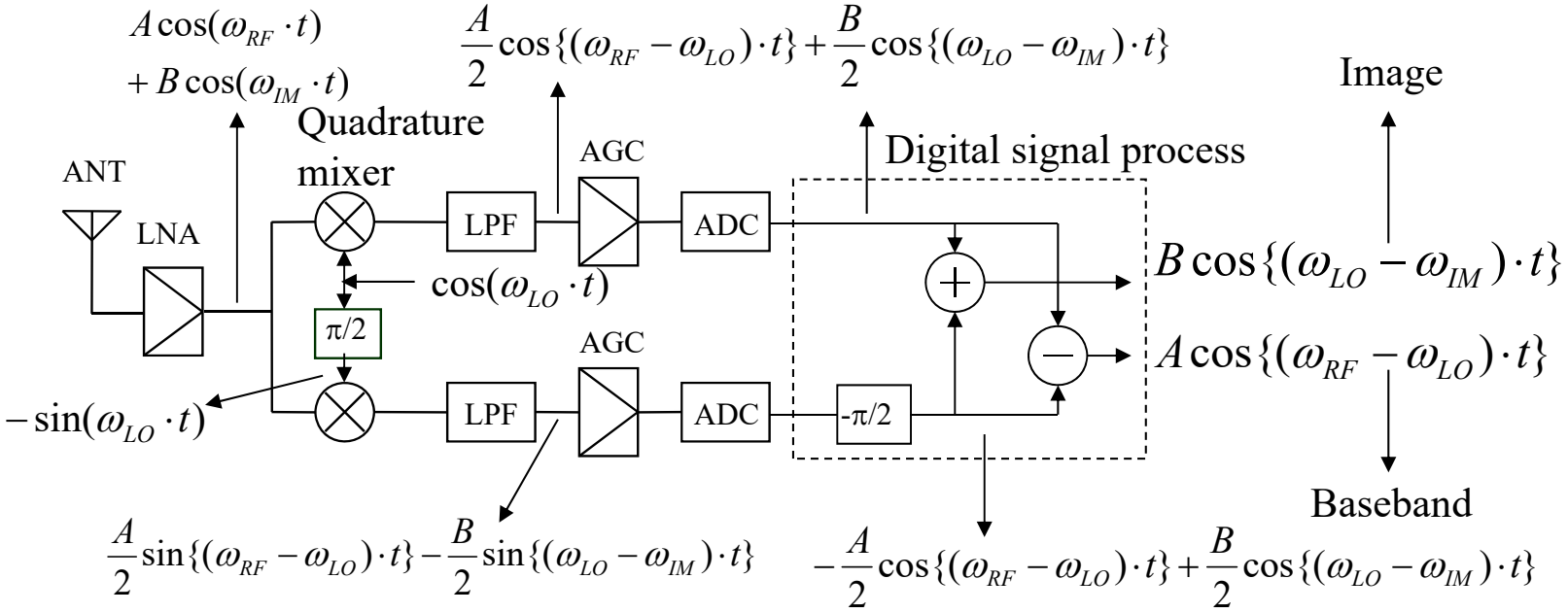


Active oxygen sensor (Sensor Expo Japan)

Example of Mixed-Signal LSI



Typical radio receiver architecture



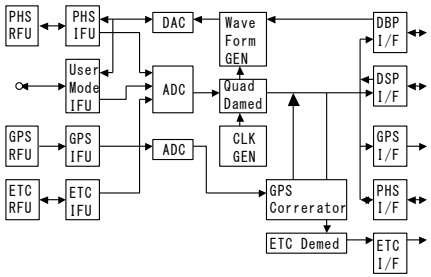
Signal processing of Hartley radio receiver

$\omega_{RF} = \omega_{LO}$ Direct conversion

$\omega_{RF} \doteqdot \omega_{LO}$ Low IF (Intermediate Frequency)

Digital design flow

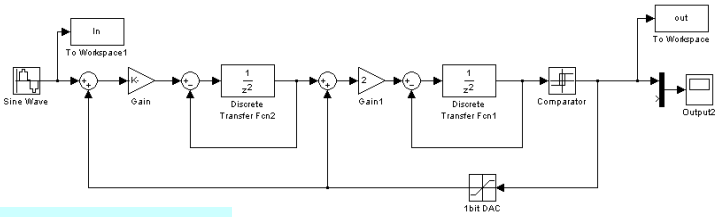
Block diagram of system architecture



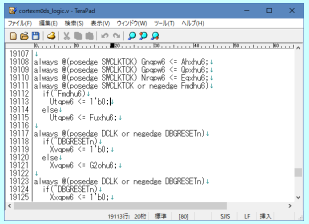
Specification sheet for digital block

項目	条件	規格値			設計値			単位
		Min.	Typ.	Max.	Min.	Typ.	Max.	
電源電圧		1.8	3.3	3.5	1.8	2.1	3.3	V
消費電流		—	—	2.2				mA
利得		—	15	—				dB
周波数		300	426	475				
雑音指数 (NF)		—	2	—				dB
1dBコンプレッションレベル		—	0	—				dBm
インターセプトポイント (IIP3)		—	9.6	—				dB
入力インピーダンス		—	50	—				Ω
出力インピーダンス		—	500	—				Ω
端子間アイソレーション (OUT→IN)				20				dB

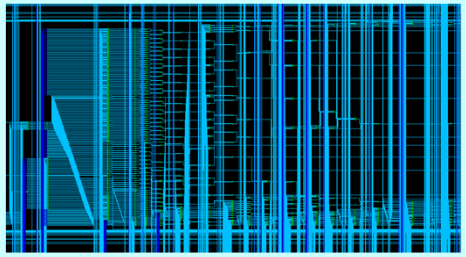
Signal flow and transfer function



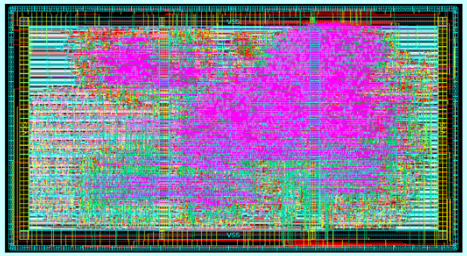
HDL (Hardware Description language)



Logic Synthesis



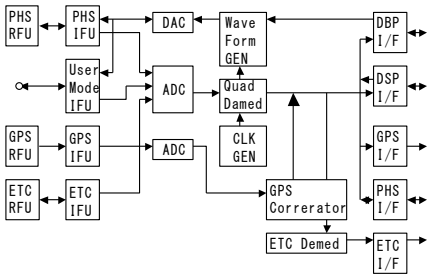
Place and Route



Marge to analog blocks

Analog design flow

Block diagram of system architecture



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周波数		300	426	475				
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1dBコンプレッションレベル		—	0	—				dBm
インタセプトポイント (IIP3)		—	9.6	—				dB
入力インピーダンス		—	50	—				Ω
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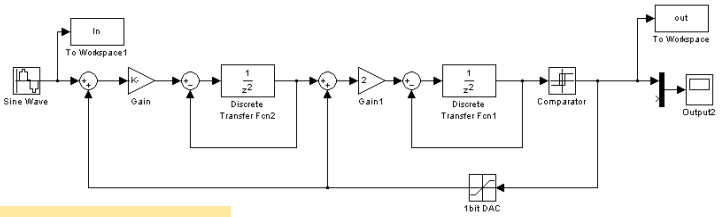
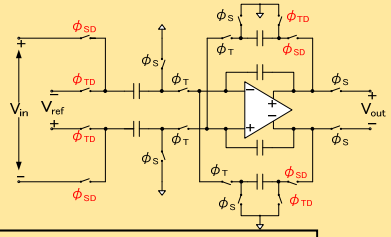
端子間アイソレーション (OUT→IN)				20				dB

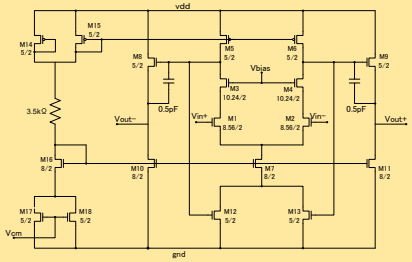
Signal flow and transfer function



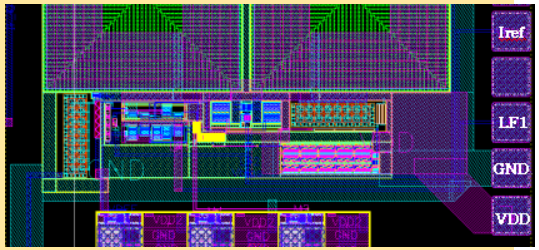
Circuit schematic with behavior models



Circuit schematic with Transistors

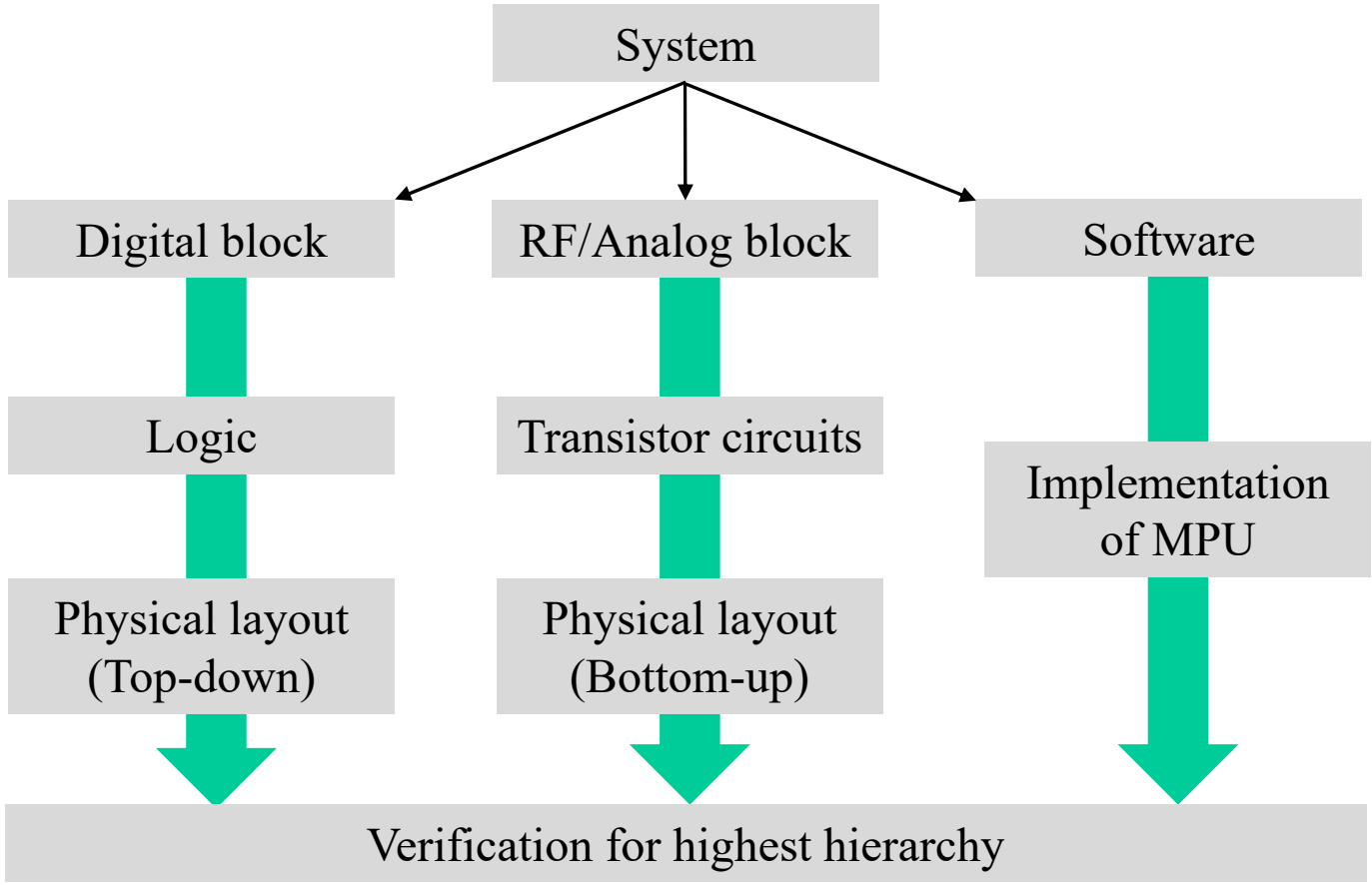


Layout artwork

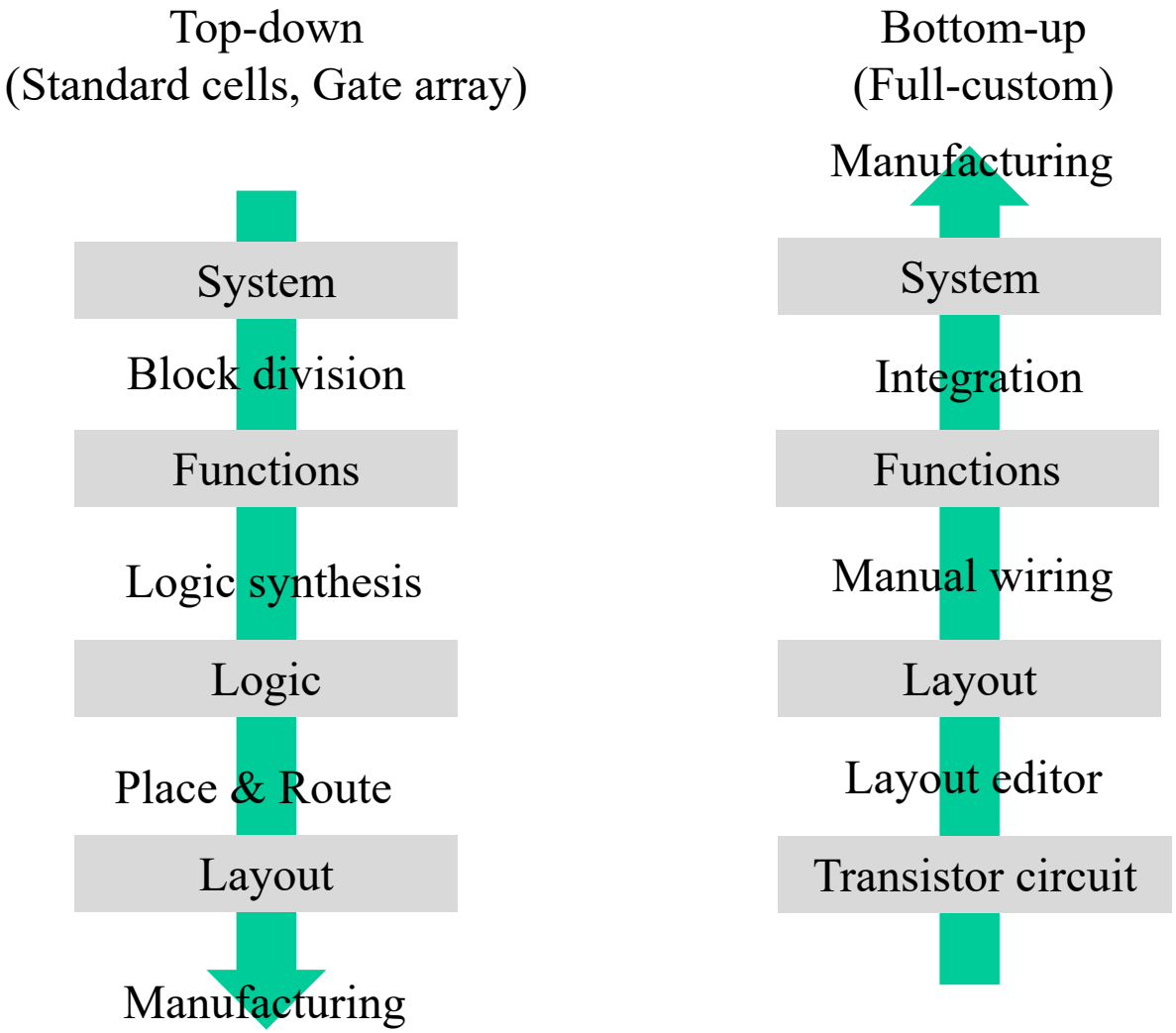


Marge to digital blocks

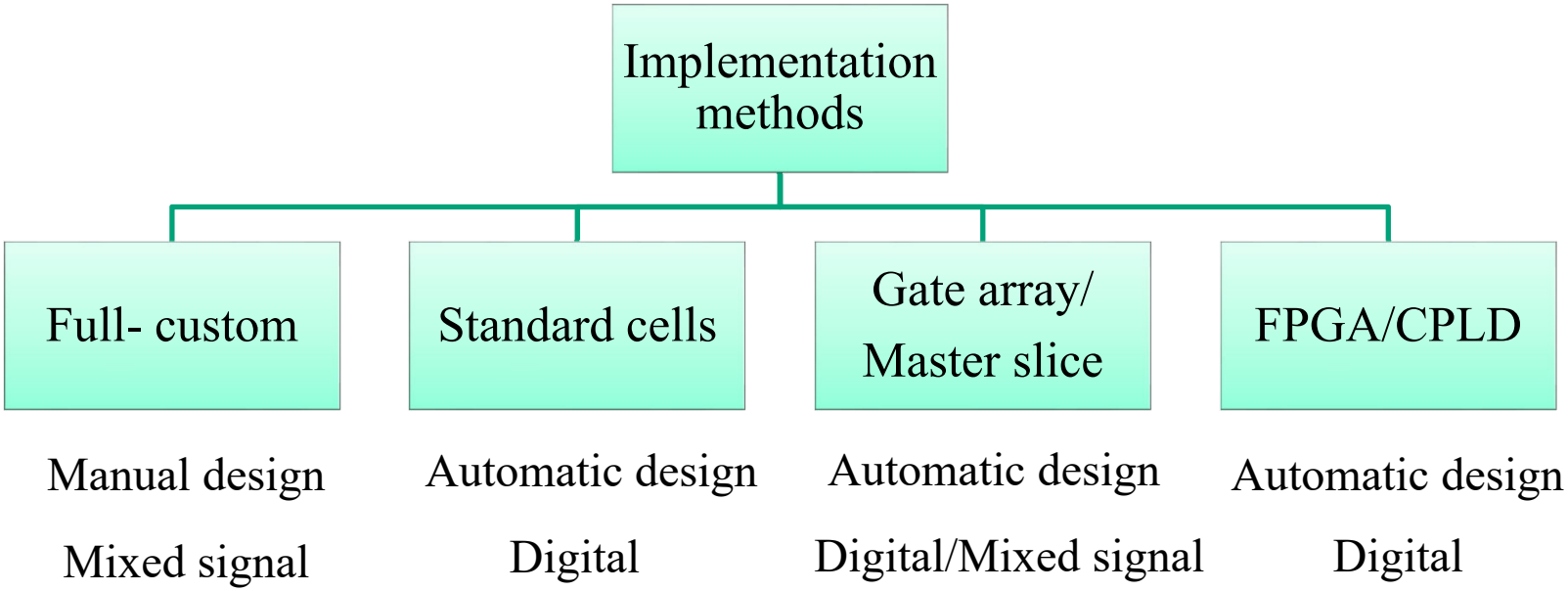
Design flow of mixed signal LSI



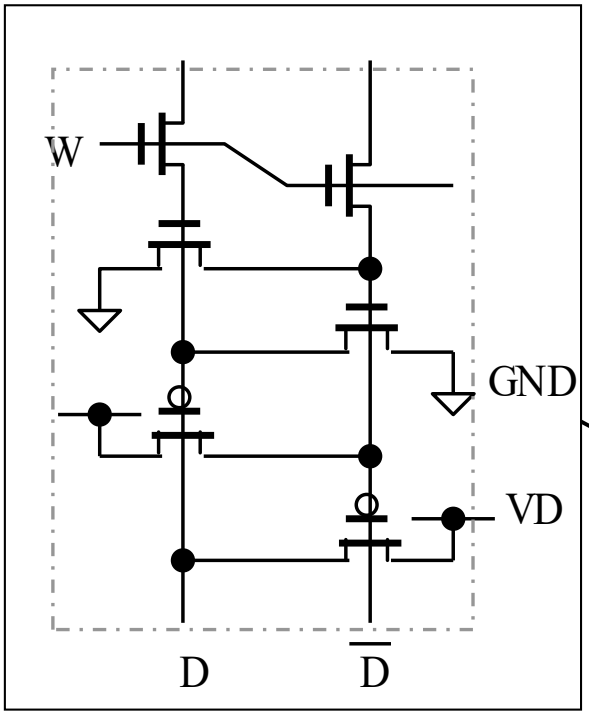
Hierarchical layout design technique



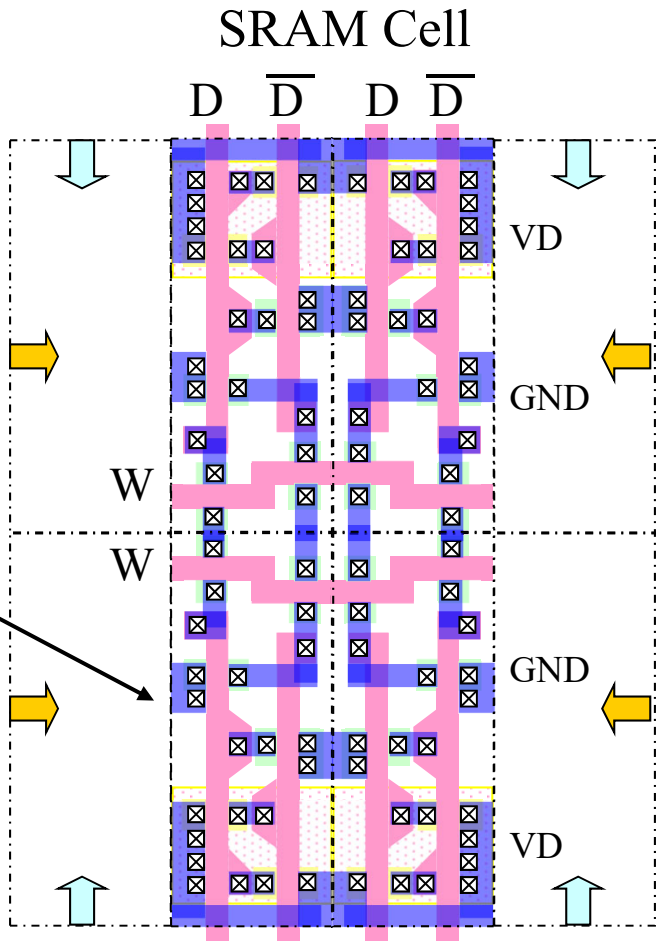
Implementation method of designed circuits

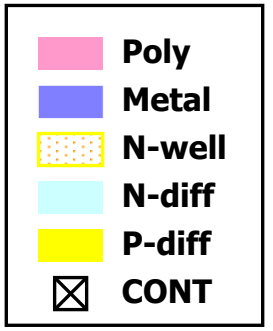


Full-custom

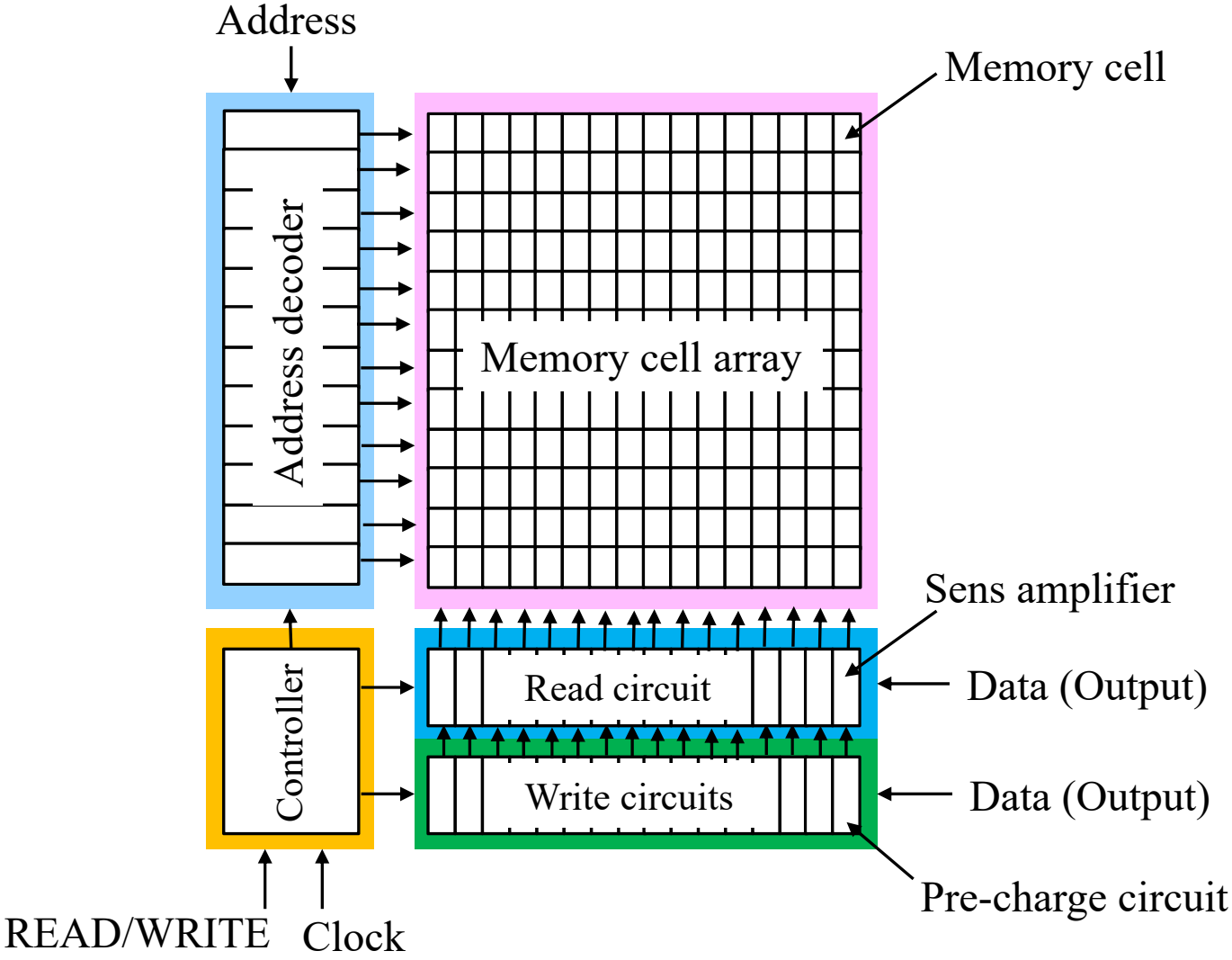


6T CMOS SRAM Cell



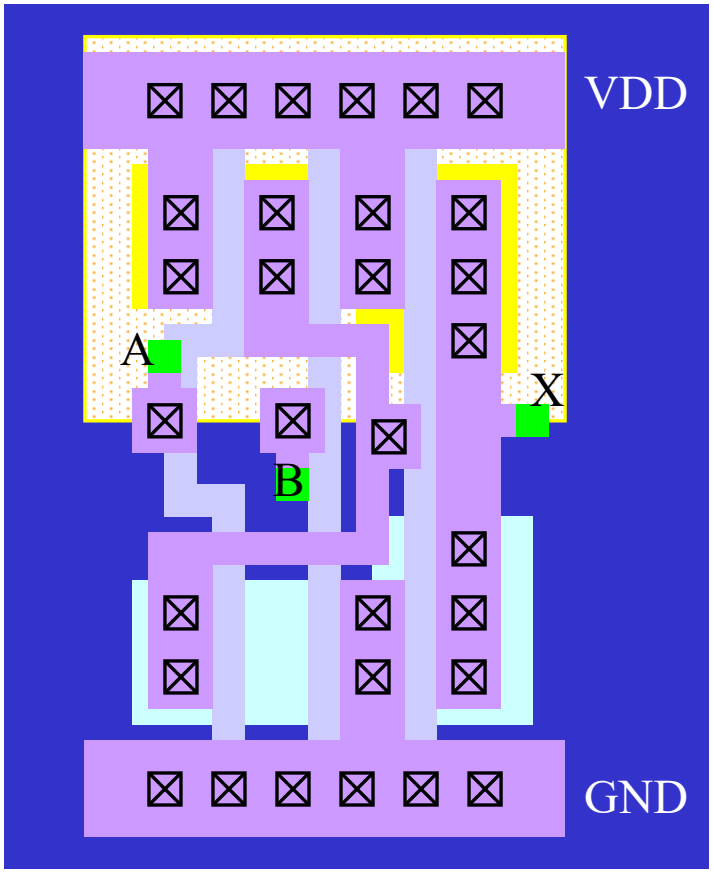


Structure of SRAM

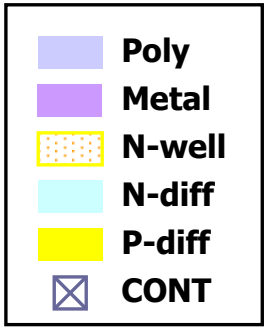


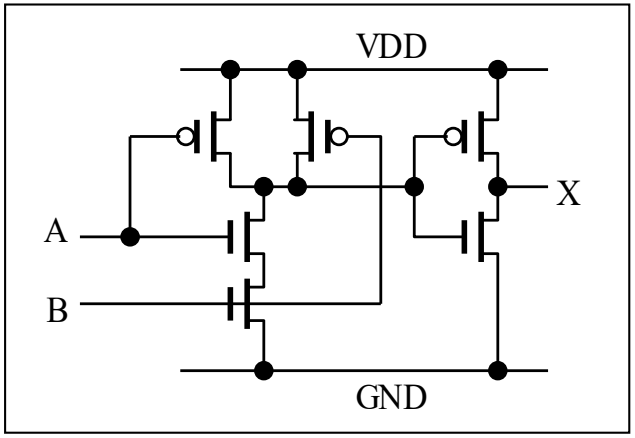
Standard cell

2-input AND cell

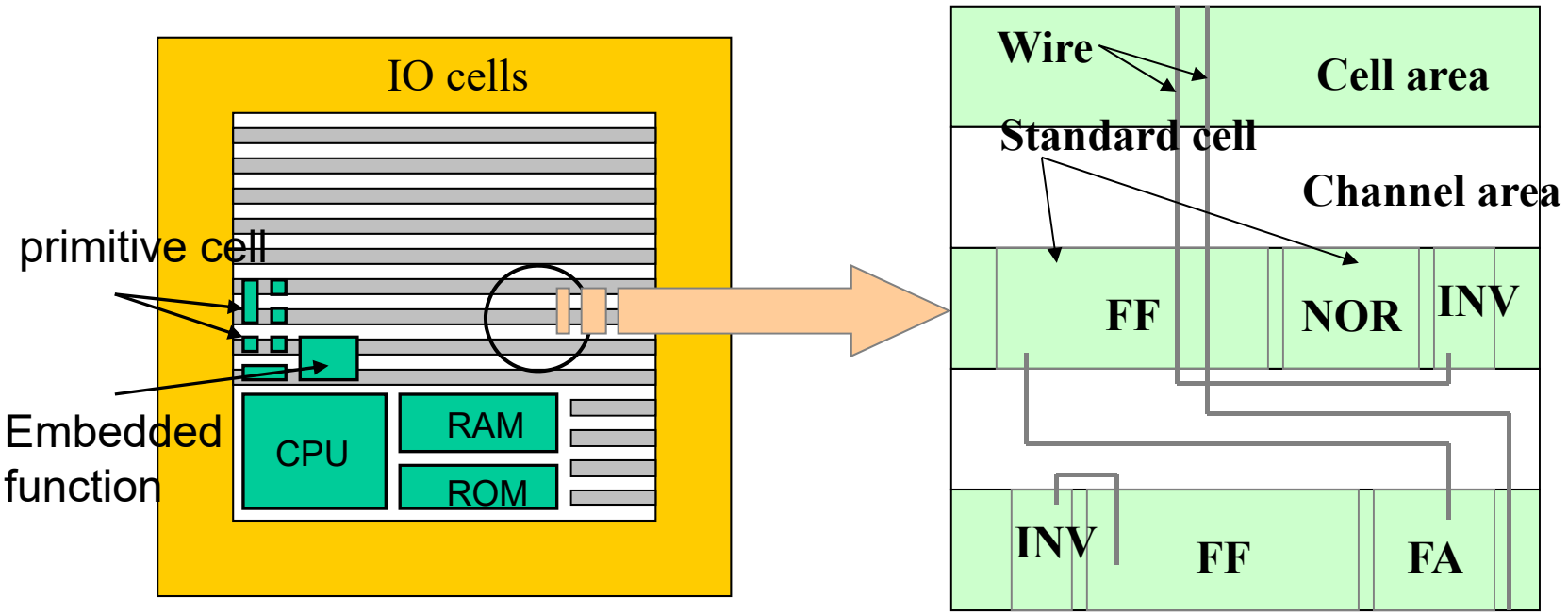


Input port



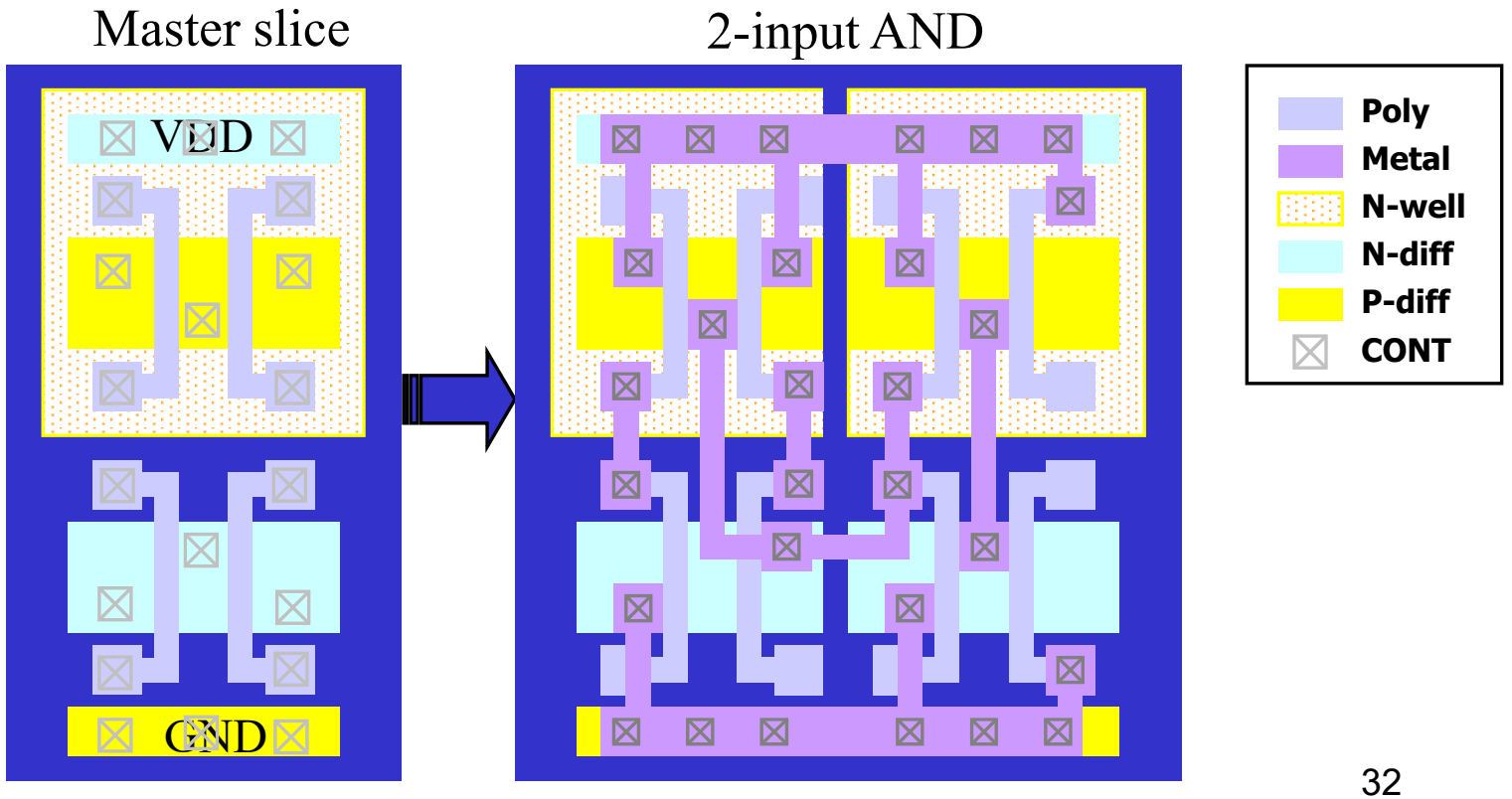


Structure of cell base IC

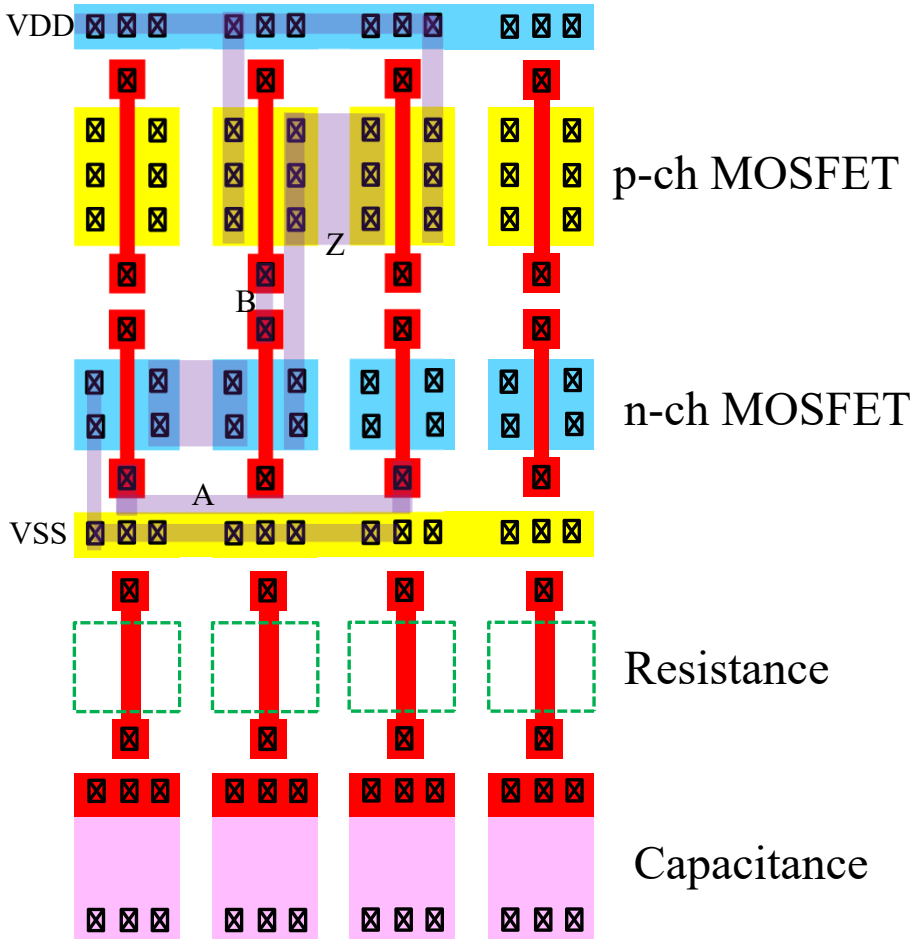


Gate Array

- The master slice is provided by manufacturer.
- The circuits and metal wire is designed by customer.

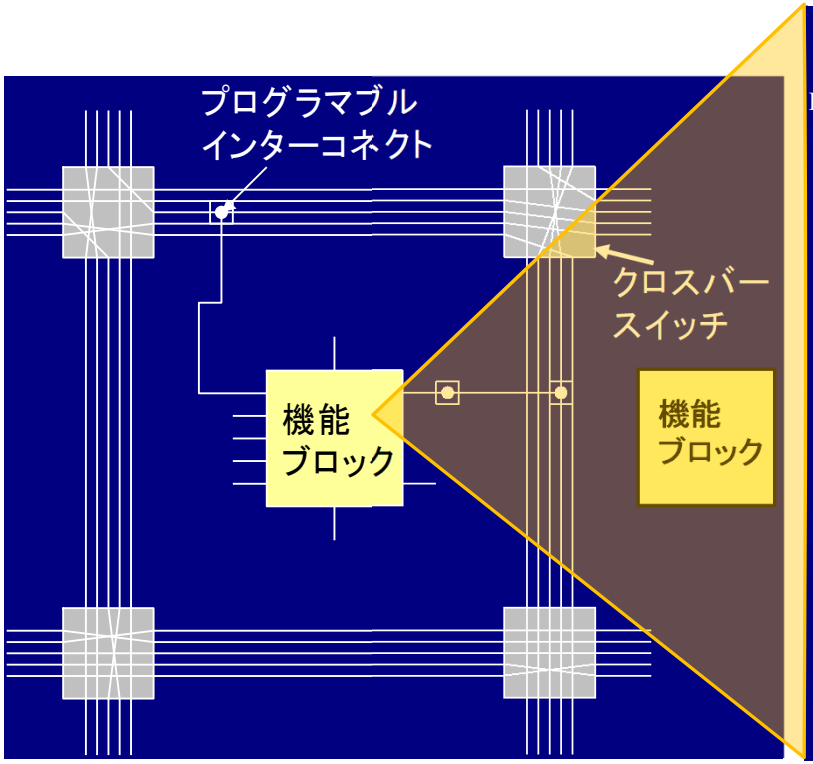


Analog master slice

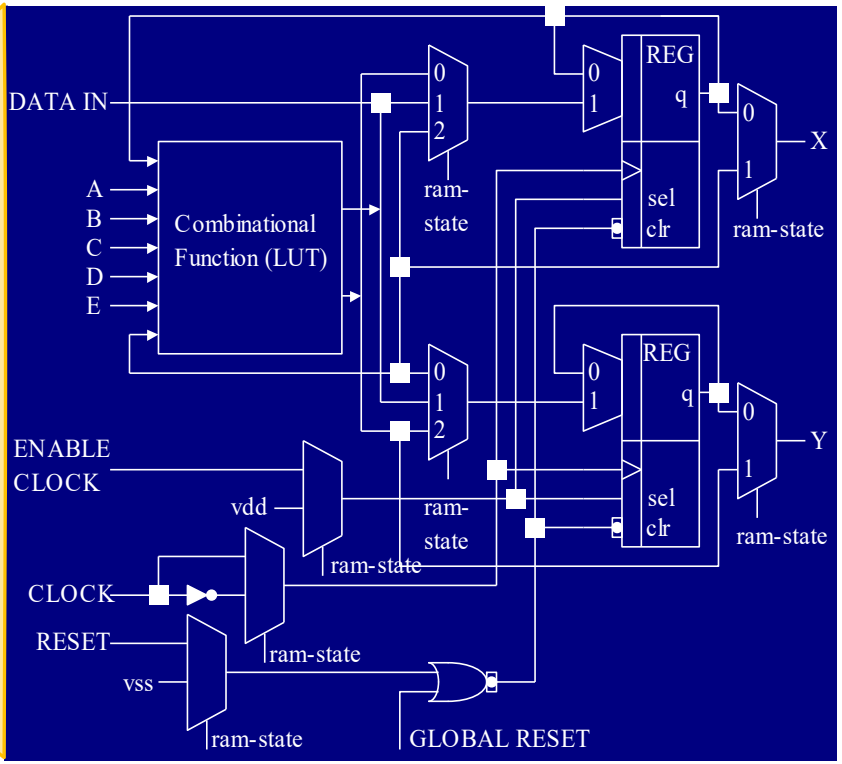


2-input NAND

Structure of FPGA

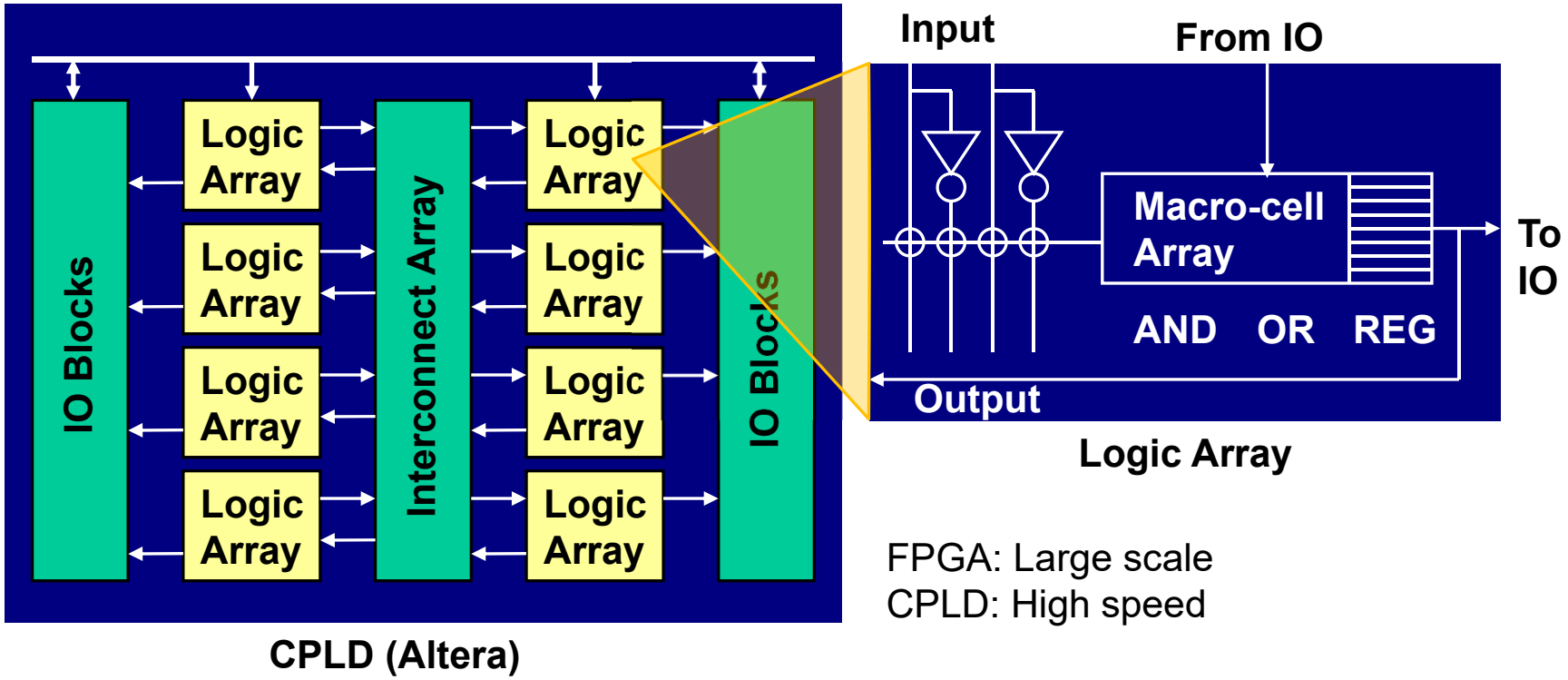


Local wiring and crossbar switch



Function block (Xilinx)

Structure of CPLD



FPGA: Large scale
CPLD: High speed