3. Data converters 1

(Oversampling converters)

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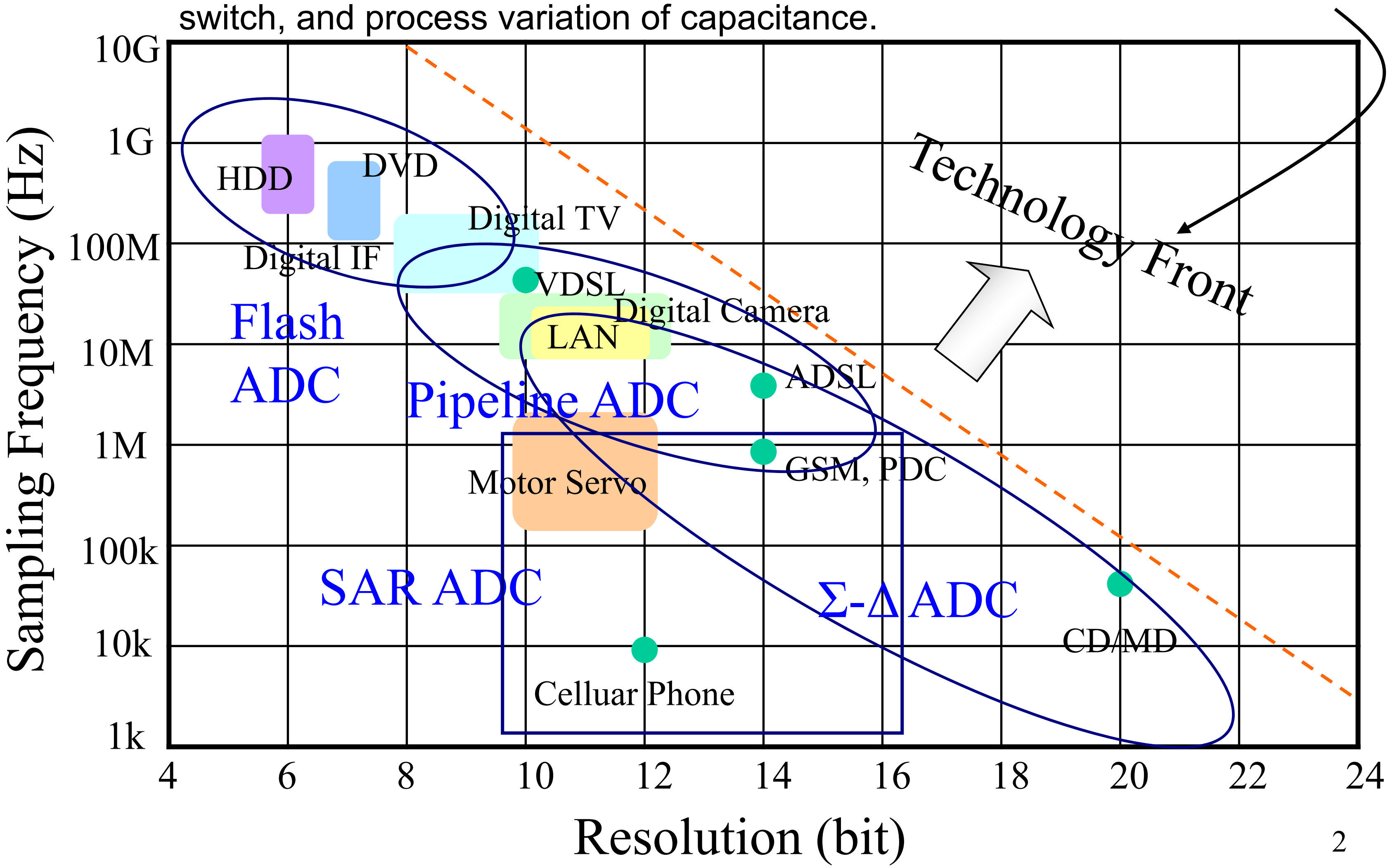
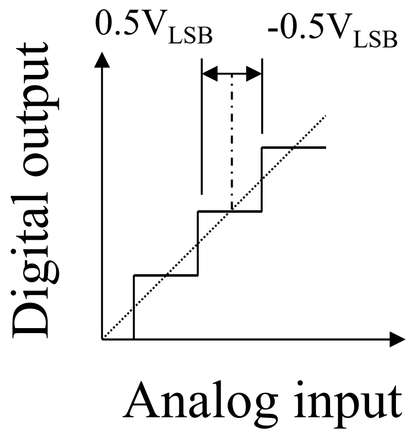
Performance of ADC architecture

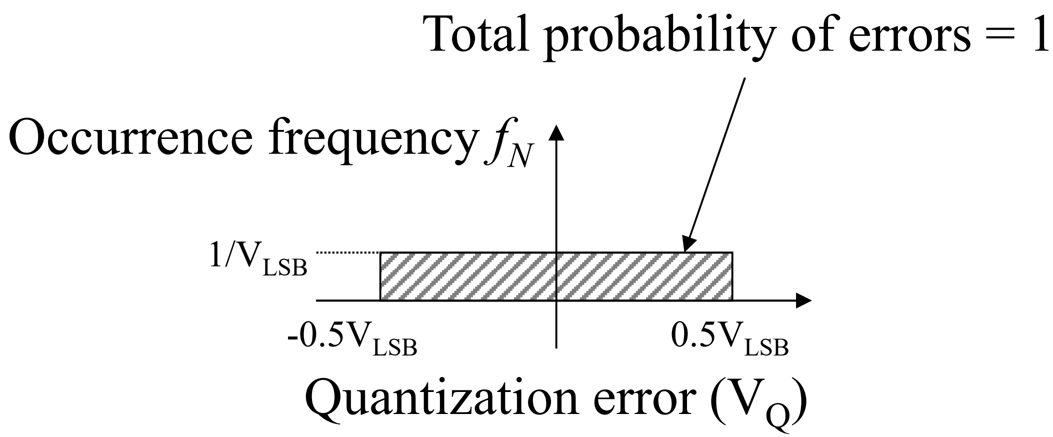
Technology front is limited by GBP of amplifier, switching speed of CMOS-switch, and process variation of capacitance.



3.1 Quantization noise and noise shaping

Quantization noise





N-bit quantization ⇨ $V_{\max} = (2^N - 1) \cdot V_{LSB}$

Noise level $$V_{Q\_RMS} = \sqrt{\int_{-\infty}^{\infty} V_Q^2 f_N(V_Q) dV_Q} = \sqrt{\frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{0.5V_{LSB}} V_Q^2 dV_Q} = \frac{V_{LSB}}{2\sqrt{3}}$$

Maximum Signal level $$V_{\max\_RMS} = \sqrt{\int_{-\infty}^{\infty} V_{in}^2 dV_Q} = \frac{V_{\max}}{2\sqrt{2}} = \frac{(2^N - 1)V_{LSB}}{2\sqrt{2}}$$

SNR of quantized signal

$$SNR(\text{dB}) = 10\log\frac{V^2{}_{\max\_RMS}}{V^2{}_{Q\_RMS}} = 10\log\frac{\left(\frac{2^N-1}{2\sqrt{2}}V_{LSB}\right)^2}{\left(\frac{V_{LSB}}{2\sqrt{3}}\right)^2} = 10\log\frac{3}{2}(2^N-1)^2$$

$$\cong 6.02N + 1.76 \quad (\text{dB})$$

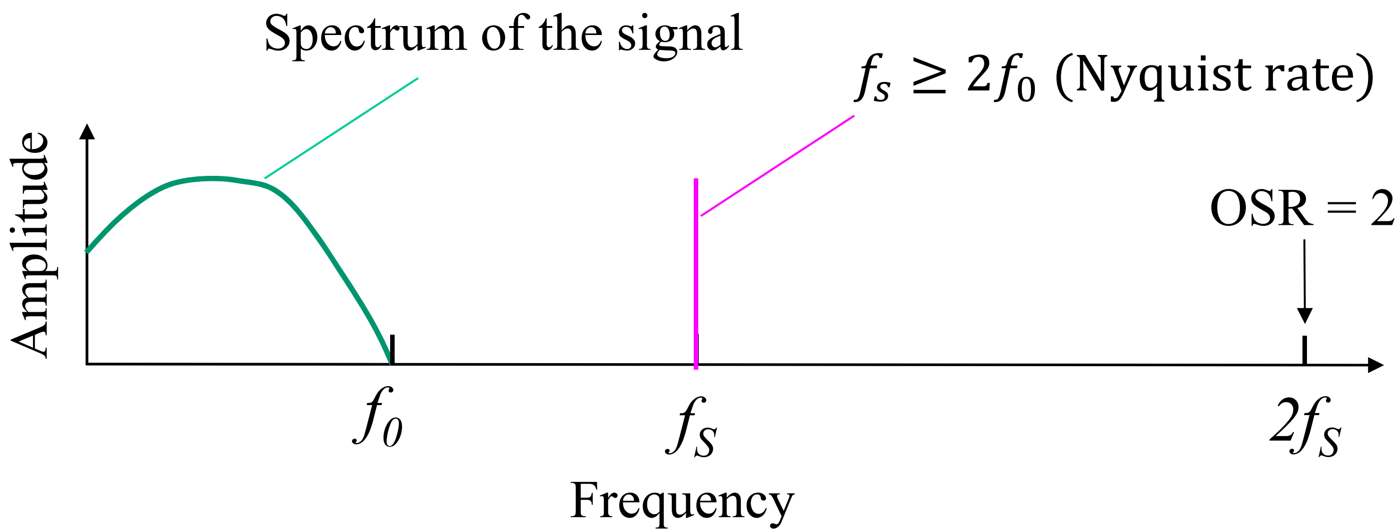
Oversampling

Oversampling ratio $OSR \equiv \frac{f_S}{2 \cdot f_0}$

f_s = Sampling rate
f_0 = Maximum signal frequency

Sampling theorem (Nyquist-Shannon's theorem): $f_0 \leq \frac{f_s}{2}$

The minimum sampling frequency $2f_0$ called Nyquist rate.



Quantization noise by oversampling

Assuming that the quantization error generates the white noise,

Noise power spectrum density $PDS_Q = \frac{V_{Q\_RMS}^2}{f_S} = \frac{\left(\frac{V_{LSB}}{2\sqrt{3}}\right)^2}{f_S} = \frac{V_{LSB}^2}{12 f_S}$

Noise power level in band $P_{Q\_RMS} = \int_{-f_0}^{f_0} PSD_Q df = \frac{V_{LSB}^2}{12 f_S} 2 f_0 = \frac{V_{LSB}^2}{12} \frac{1}{OSR}$

SNR in band width

$$SNR(\text{dB}) = 10\log\frac{V^2{}_{\max\_RMS}}{P_{Q\_RMS}} = 10\log\frac{\left(\frac{2^N-1}{2\sqrt{2}}V_{LSB}\right)^2}{\frac{V_{LSB}^2}{12}} OSR$$

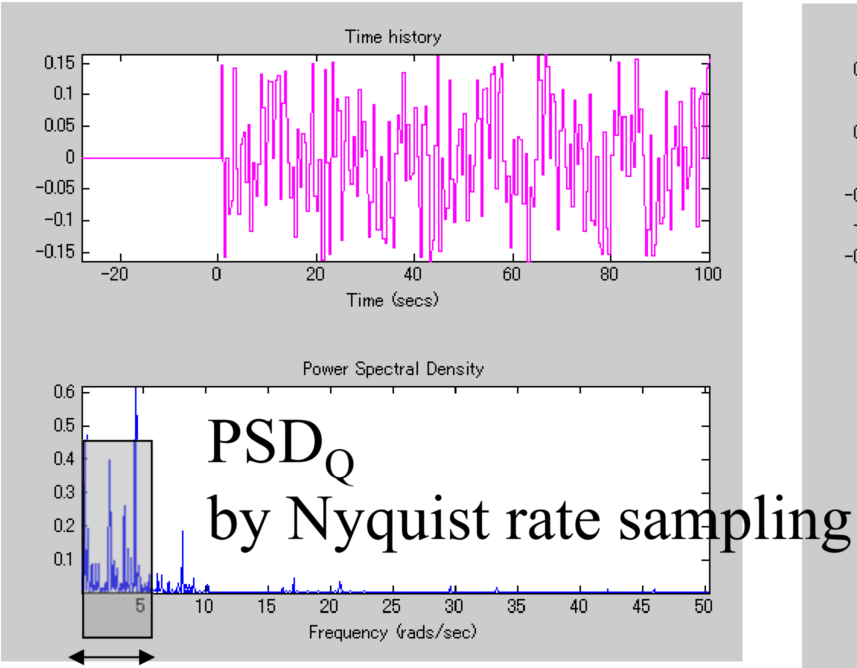
$$= 10\log\frac{3}{2}(2^N-1)^2 + 10\log OSR$$

$$\cong 6.02N + 1.76 + 10\log OSR \quad (\text{dB})$$

Noise reduction by over sampling

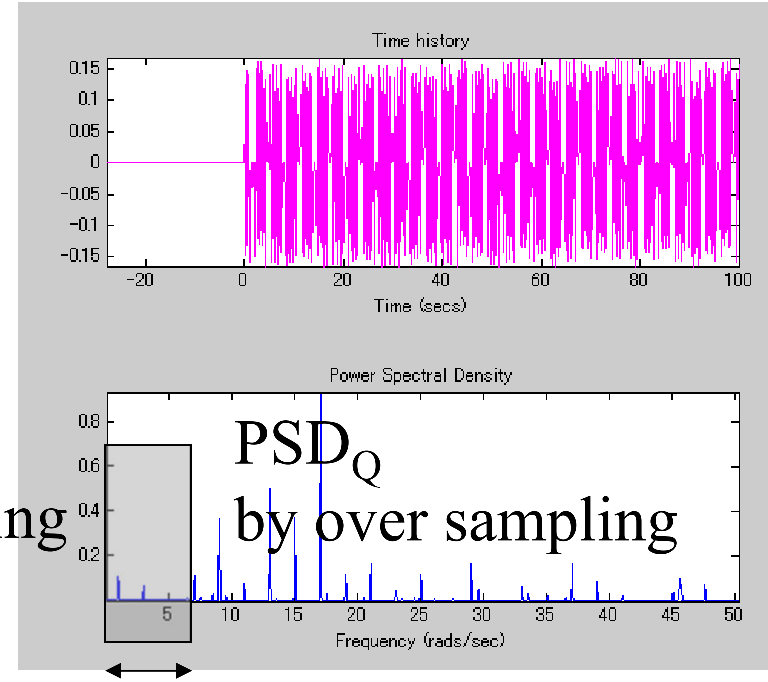
Quantization error

N = 1bit



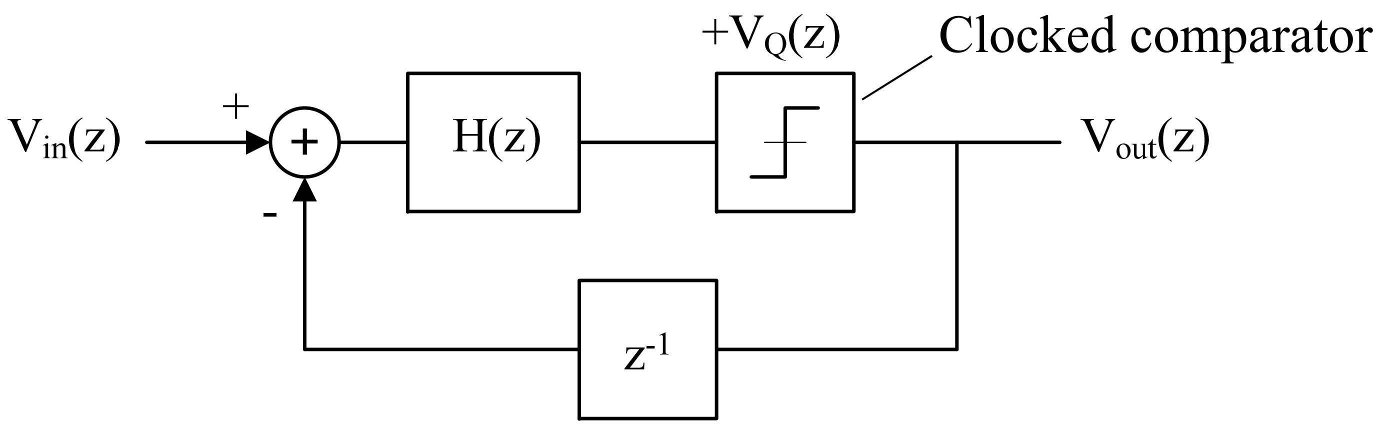
f_0 OSR = 1

N = 1bit



f_0 OSR = 8

Delta-sigma modulator



$$V_{out}(z) = H(z)\{V_{in}(z) - z^{-1}V_{out}(z)\} + V_Q(z)$$

$$V_{out}(z) = \frac{H(z)}{1 + z^{-1}H(z)} V_{in}(z) + \frac{1}{1 + z^{-1}H(z)} V_Q(z)$$

For example, $H(z) = \frac{1}{1 - z^{-1}}$ (BET Integral)

Transfer function of noise

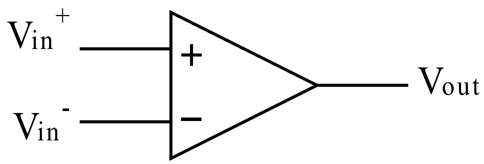
$$V_{out}(z) = V_{in}(z) + (1 - z^{-1})^M V_Q(z)$$ (Order M = 1)

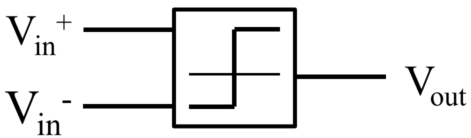
Zero @ *f = 0*

Function of analog comparator

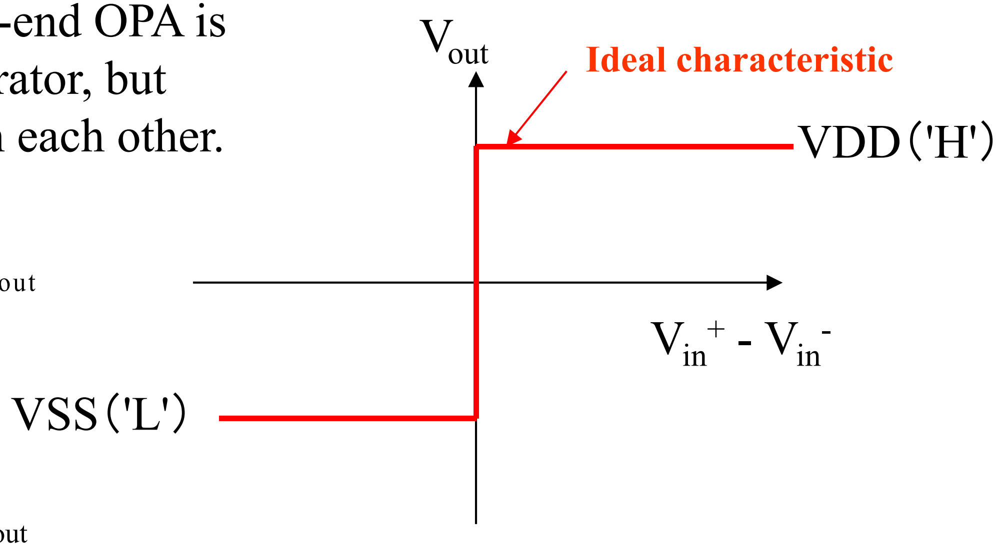
- If ($V_{in}^{+} > V_{in}^{-}$), then V_{out} = VDD (Logic level = 'H')
- If ($V_{in}^{+} < V_{in}^{-}$)，then V_{out} = VSS (Logic level = 'L')

The same symbol as a single-end OPA is sometimes used for a comparator, but the circuitry is different from each other.





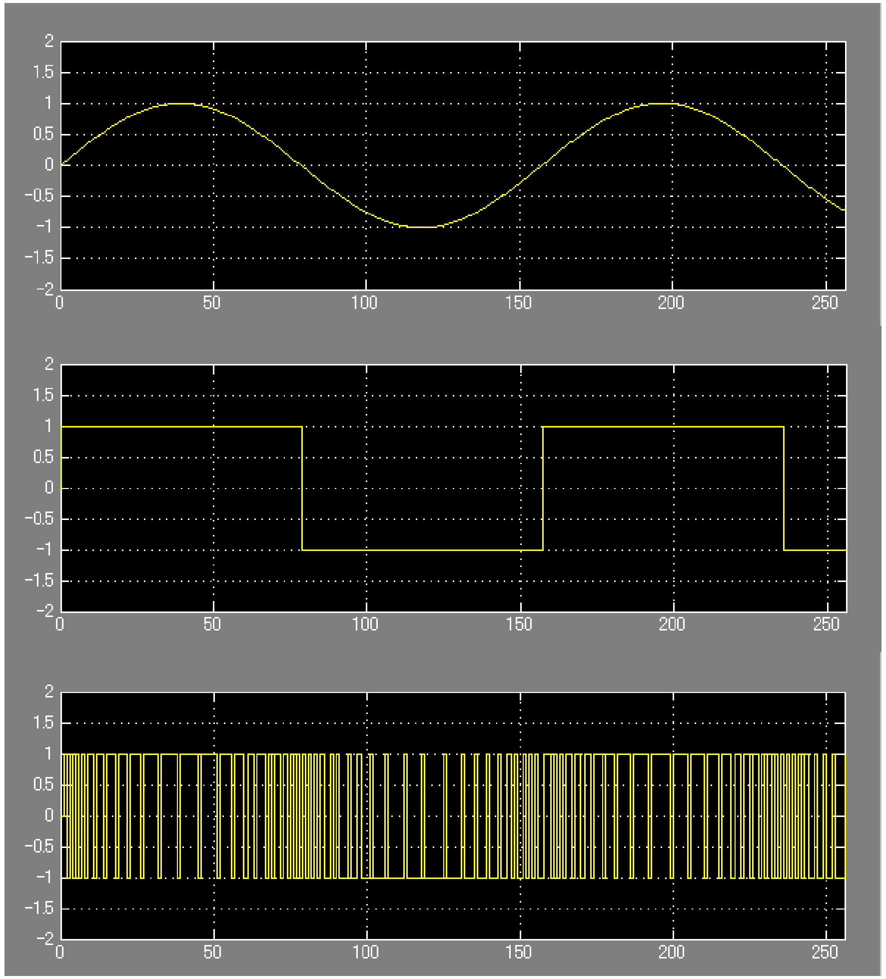
Symbol



コンパレータの2つの機能

- 電圧差が0Vになるタイミングの検知（クロックなし）
- あるタイミングでの電圧の大小比較（クロックあり）
- ここでは、後者を用いる

Time domain characteristic of delta-sigma modulator



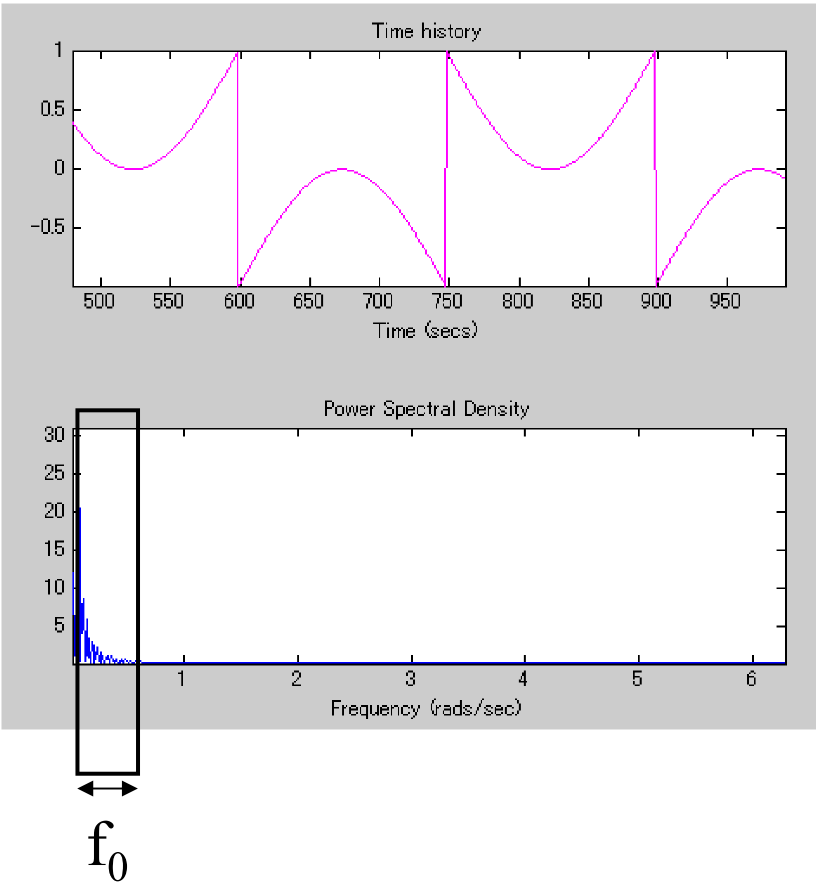
32 bit binary

Comparator
(OSR = 24)

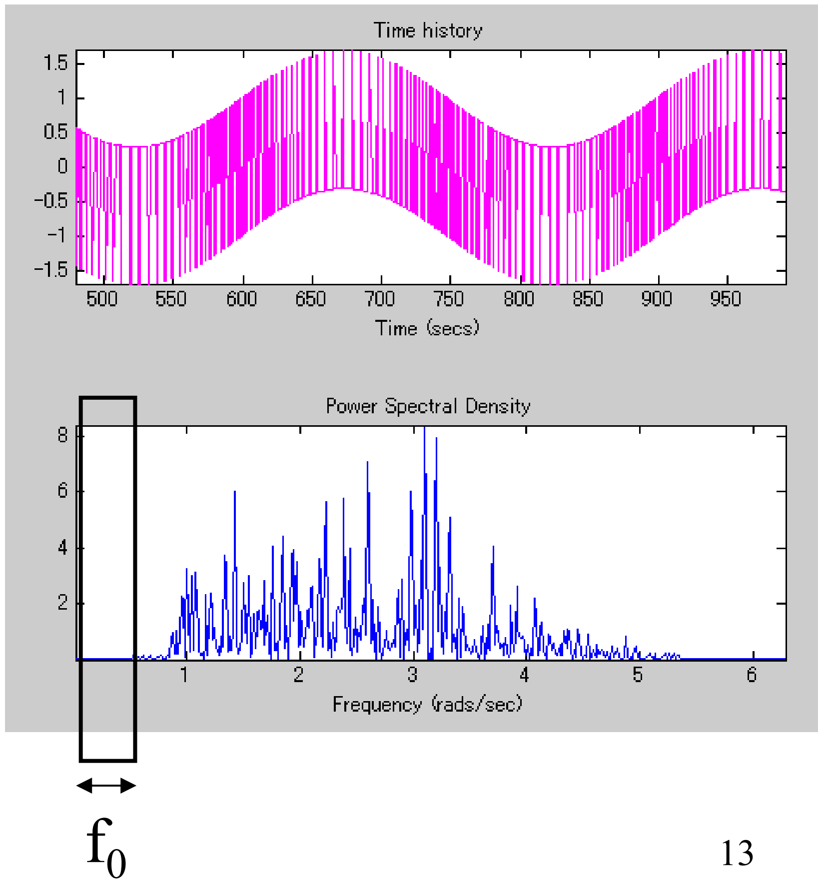
1-bit delta-sigma modulation
= Pulse-density modulation
(OSR = 24)

Noise shaping by delta-sigma modulation

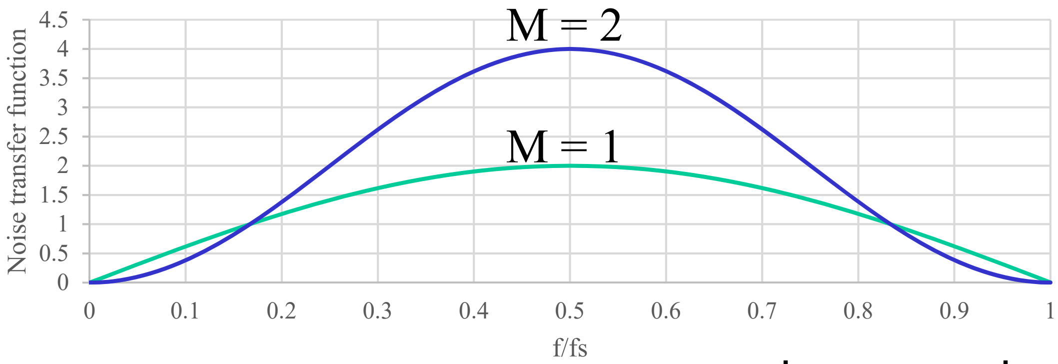
Error of comparator



Error of 1-bit delta-sigma modulation



Noise reduction by noise shaping



$$\frac{f}{f_S}$$

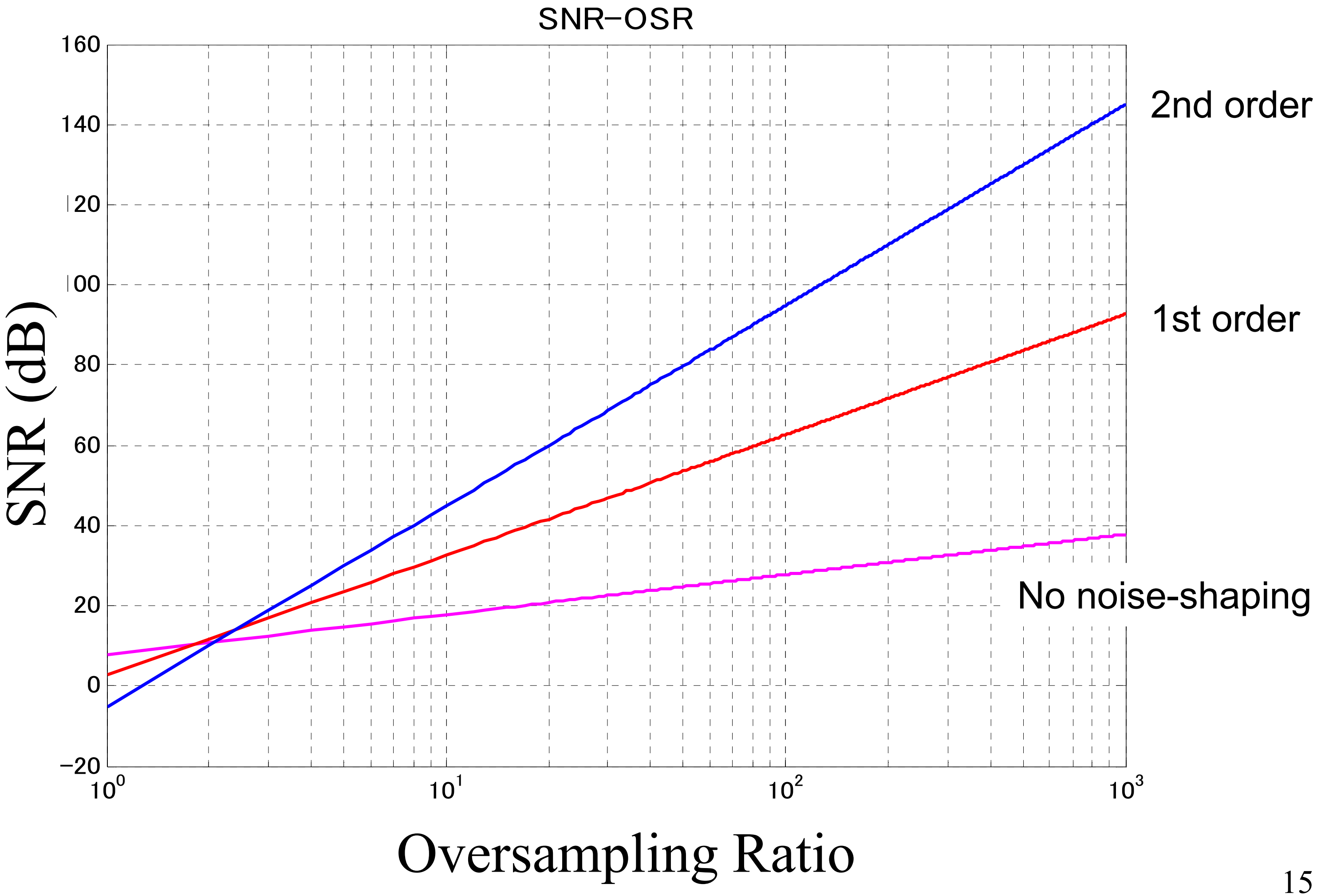
M =1 $$|(1-z^{-1})| = \left|1-e^{-j\omega T_S}\right| = \left|2\sin(\pi\frac{f}{f_S})\right|$$

M =2 $$|(1-z^{-1})^2| = \left|1-e^{-j\omega T_S}\right|^2 = \left|2\sin(\pi\frac{f}{f_S})\right|^2$$

$$SNR(dB) = \int_{-f_0}^{f_0} \frac{V_{\max\_RMS}^2}{P_{Q\_RMS}\cdot\left|2\sin(\pi\frac{f}{f_S})\right|^{2M}} df$$

$$\cong 6.02N + 1.76 - 20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right) + (20M+10)logOSR$$

SNR vs. OSR


SNR-OSR
SNR (dB)
Oversampling Ratio
2nd order
1st order
No noise-shaping
160
140
120
100
80
60
40
20
0
−20
10^0
10^1
10^2
10^3

Effective number of bits (ENOB)

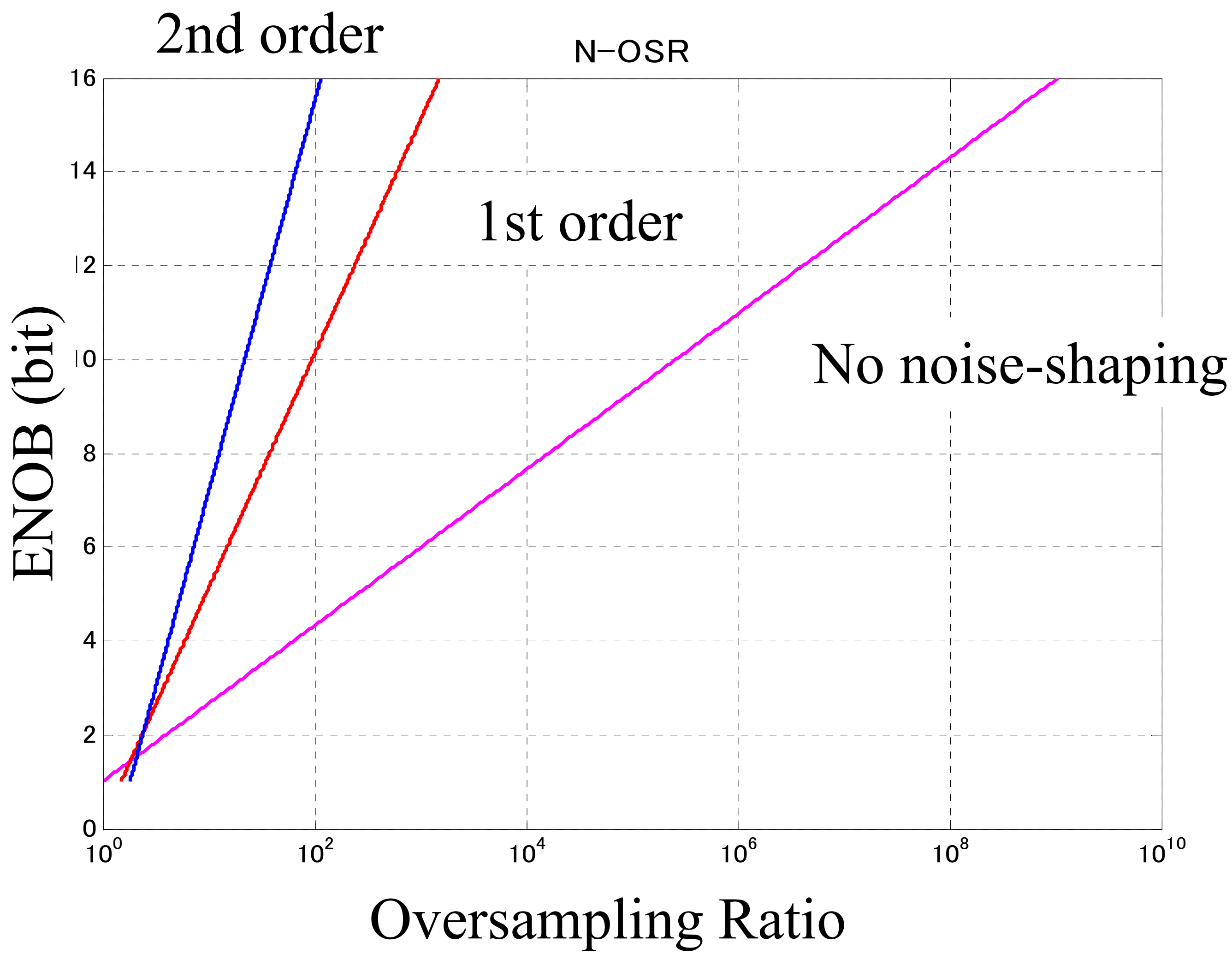
For 1-bit quantization (=Comparator),

Simple quantization Noise shaping (N = 1bit)

$$6.02ENOB + 1.76 = 6.02 + 1.76 - 20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right) + (20M + 10)logOSR$$

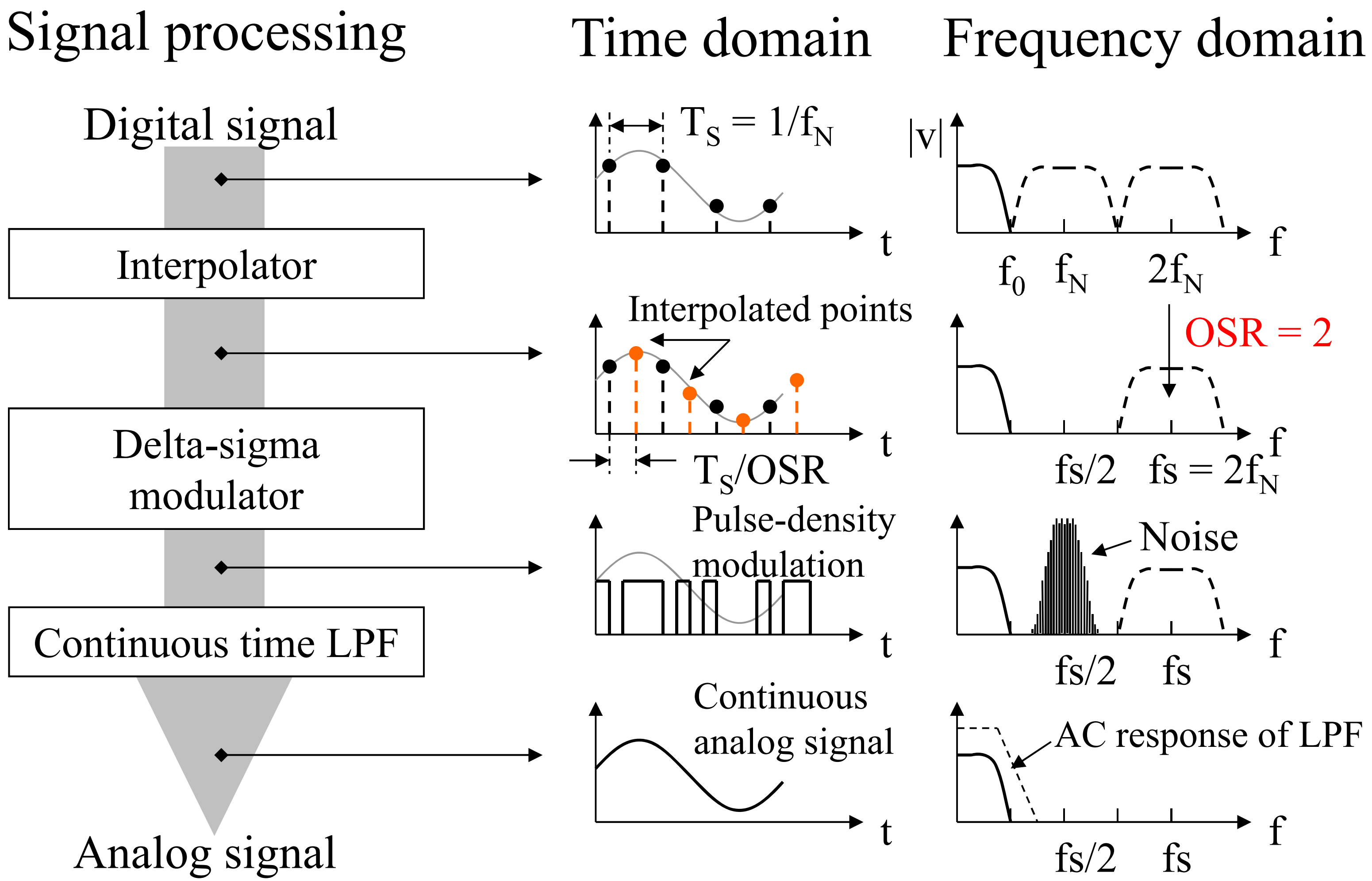
$$ENOB = 1 + \frac{1}{6.02}\left\{(20M + 10)logOSR - 20\log\left(\frac{\pi^M}{\sqrt{2M+1}}\right)\right\}$$

ENOB vs. OSR

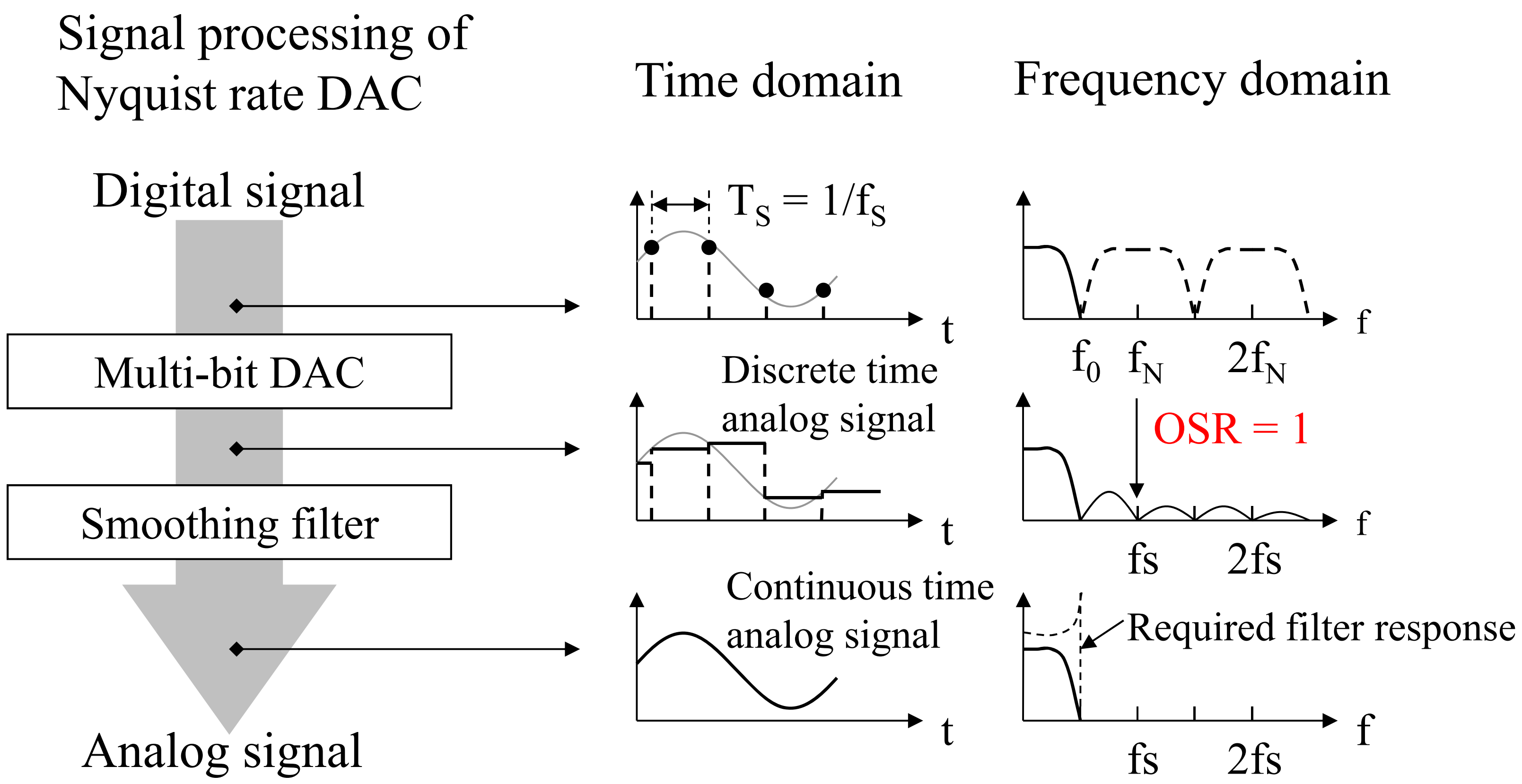

2nd order
N−OSR
1st order
No noise-shaping
ENOB (bit)
16
14
12
10
8
6
4
2
0
10^0
10^2
10^4
10^6
10^8
10^{10}
Oversampling Ratio

3.2 Oversampling DAC

Principle of oversampling DAC



Advantage of oversampling DAC



Nypuist rate DAC requires the ideal LPF for smoothing.

Appendix: Frequency response of sample and hold circuit

Sample and hold of the signal *x(t)*

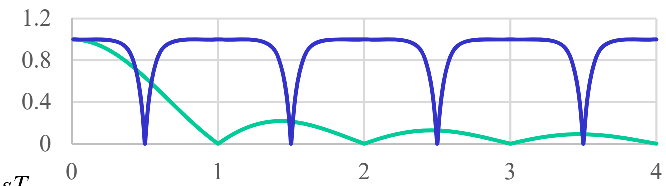
$$x_{du}(t) = \sum_n x(nT_S) \cdot \underbrace{\{u(t-nT_S) - u(t-(n+1)T_S)\}}_{\text{Step sampler}}$$

$\mathcal{L}$ ⇩

$$X_{du}(s) = \int_0^\infty \sum_n x(nT_S) \cdot \{u(t-nT_S) - u(t-(n+1)T_S)\} \cdot e^{-st} dt$$

$$= \sum_n x(nT_S) \cdot \int_0^\infty \{u(t-nT_S) - u(t-(n+1)T_S)\} \cdot e^{-st} dt$$

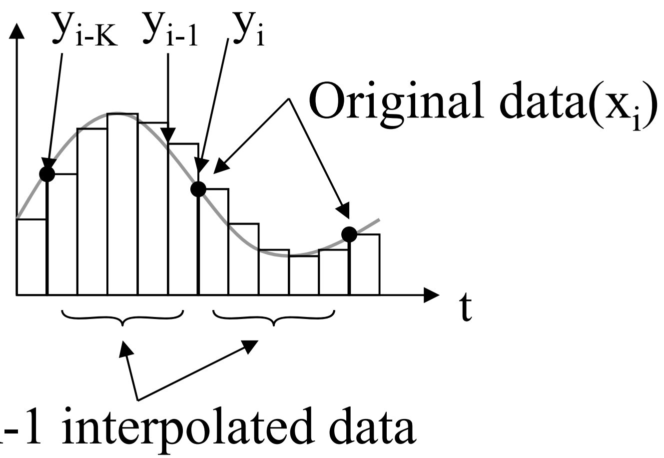
$$= \sum_n x(nT_S) \cdot \frac{e^{-snT_S}(1-e^{-sT_S})}{s}$$



$$= \frac{1-e^{-sT_S}}{s} \sum_n x(nT_S) \cdot e^{-snT_S} \xrightarrow{Z} \underbrace{\frac{1-e^{-sT_S}}{s}}_{\text{Transfer function of step sampler}} \underbrace{\sum_n x(nT_S) \cdot z^{-n}}_{\text{Impulse train}}$$

Transfer function of step sampler　　Impulse train

Interpolator



Sampling rate conversion
(up conversion)

$$f_S/K$$
$$e^{-sKT_S} = z^{-K}$$

$$(1-z^{-1})^{L+1} \xrightarrow{f_S/K} (1-z^{-K})^{L+1}$$

Example: Linear interpolation

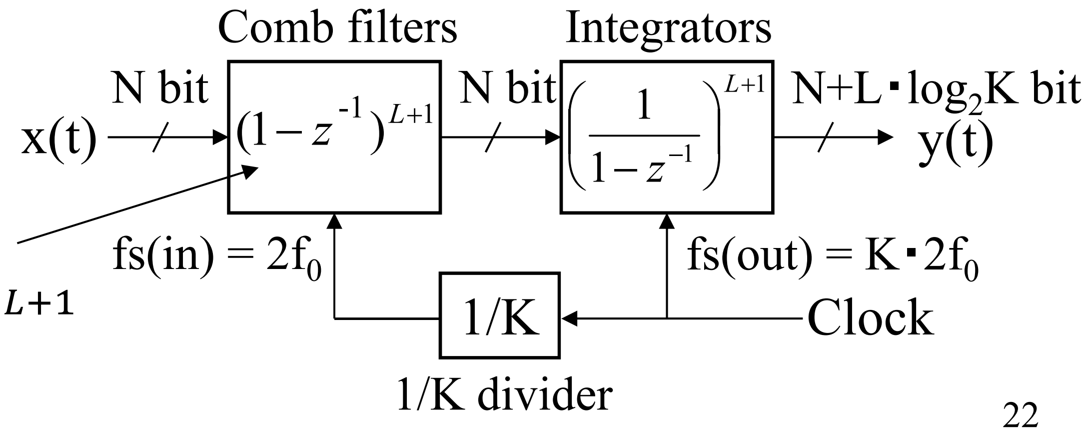
$$\frac{y_i - y_{i-1}}{T_S} = \frac{x_i - x_{i-K}}{K \cdot T_S}$$

Z

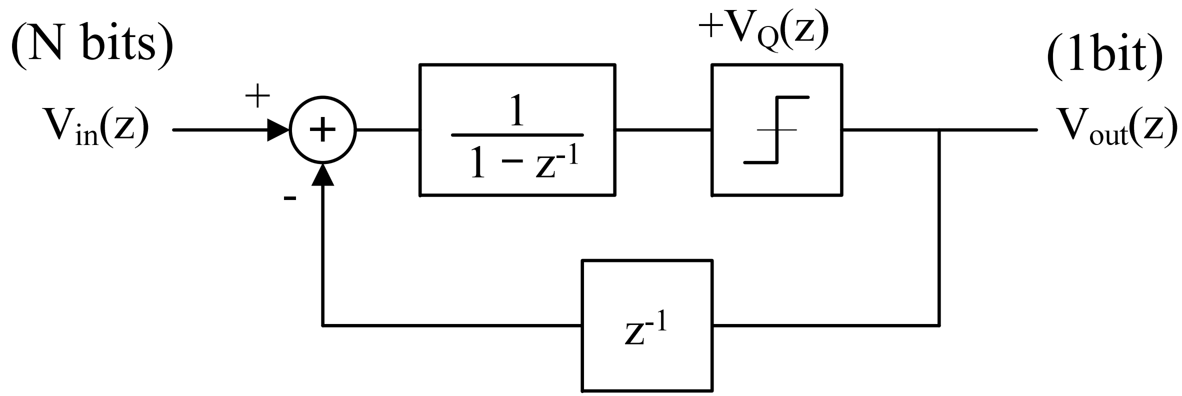
$$Y(z)(1-z^{-1}) = X(z)\frac{1-z^{-K}}{K}$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{K}\frac{1-z^{-K}}{1-z^{-1}}$$

Circuits implementation



Pulse-density modulation by delta-sigma modulator (DSM)

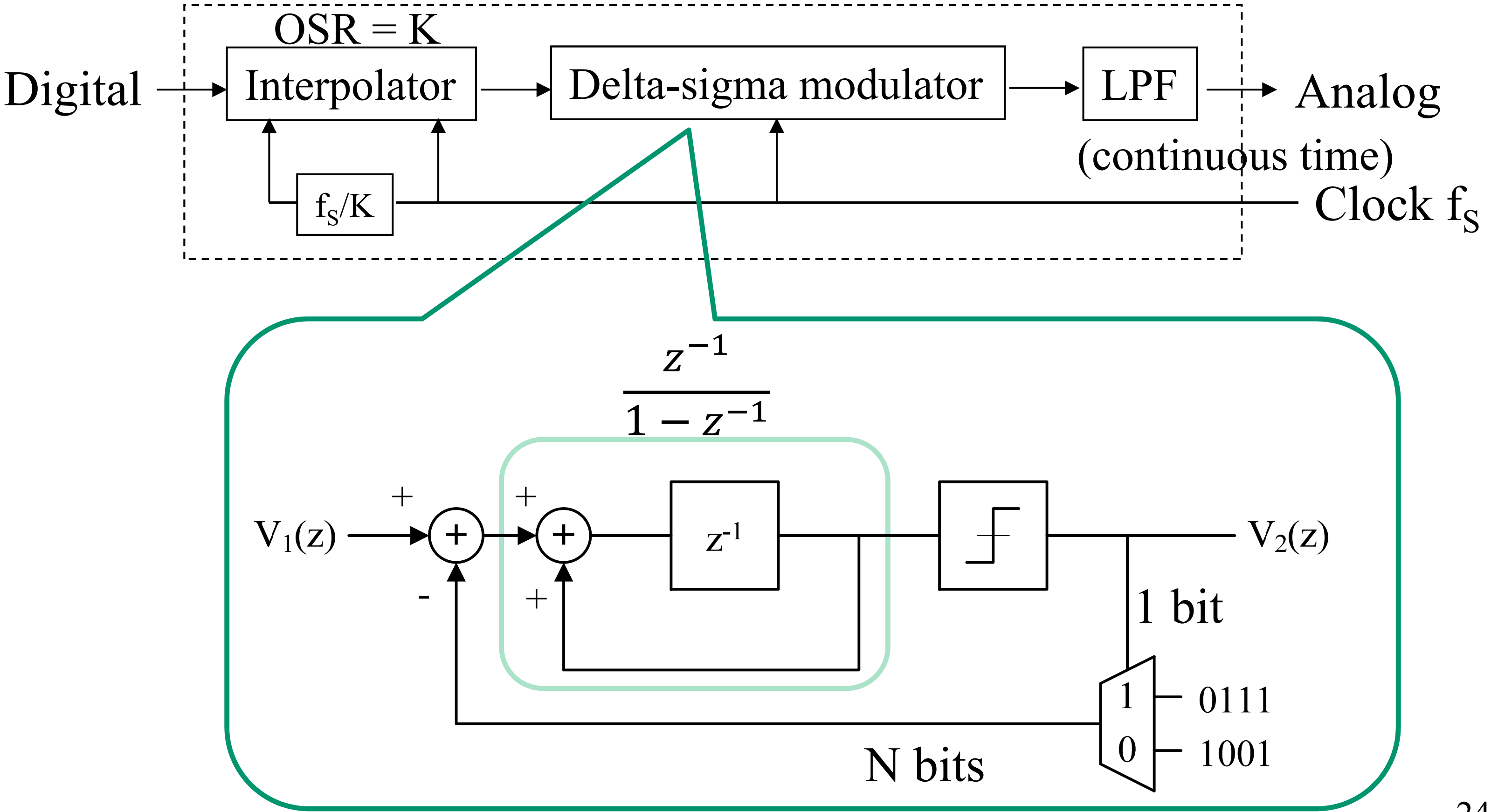


$$V_{out}(z) = V_{in}(z) + (1 - z^{-1})^M \, V_Q(z)$$

1 bit signal   N bits signal   Quantization noise

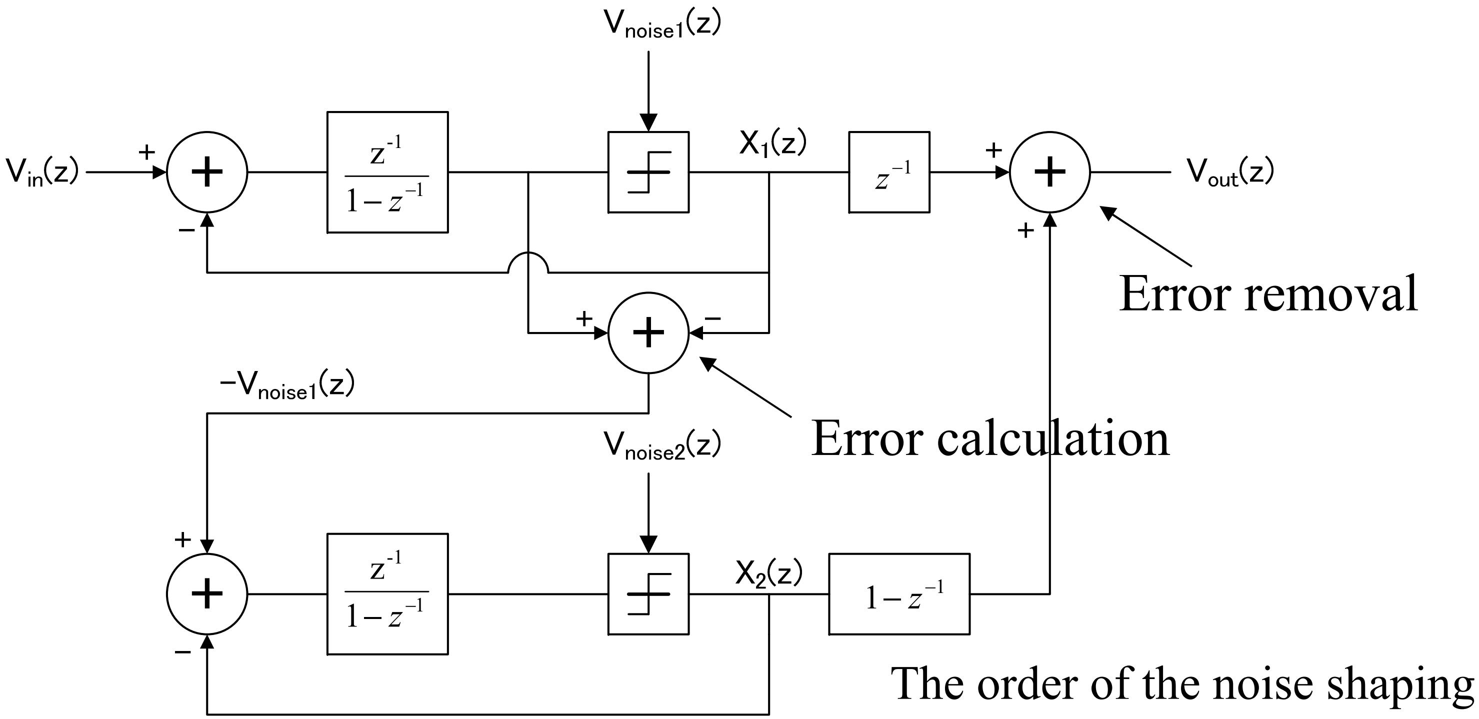
The figure shows the block diagram for the case of "M = 1".

Architecture of oversampling DAC



Higher order DSM

Multi-stage noise shaping (MASH)



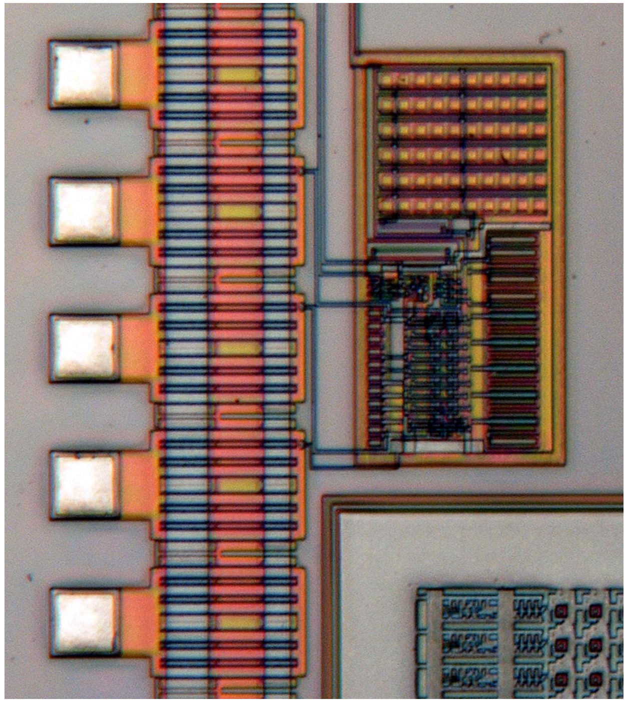
The order of the noise shaping is increased by repeating the error calculation.

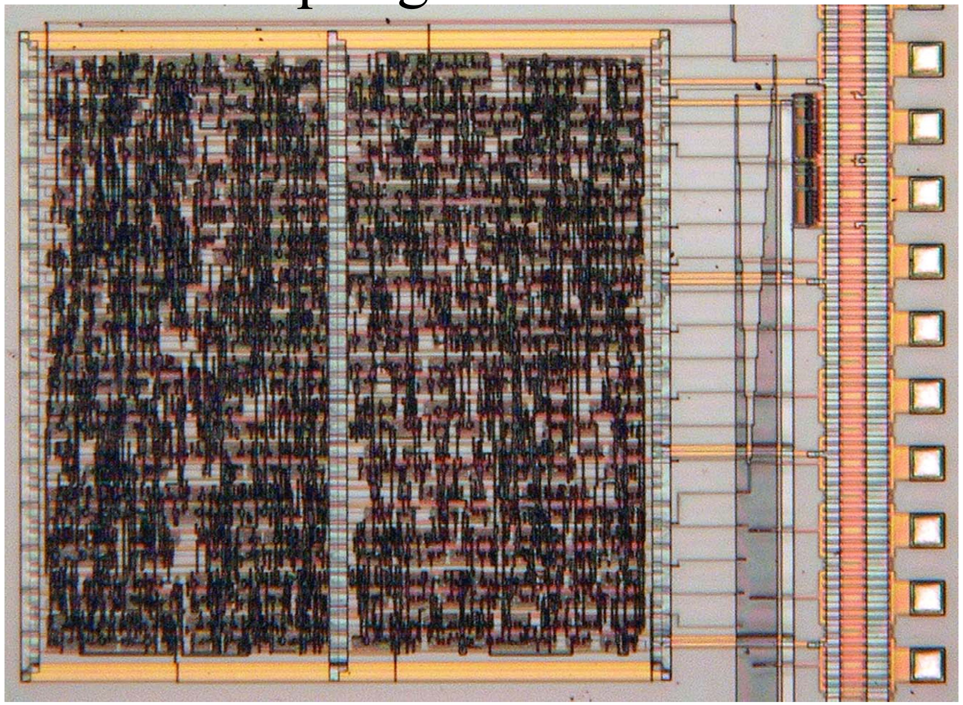
$$X_1(z) = z^{-1}V_{in}(z) + (1-z^{-1})V_{noise1}(z)$$

$$X_2(z) = -z^{-1}V_{noise1}(z) + (1-z^{-1})V_{noise2}(z)$$

$$V_{out}(z) = z^{-1}X_1(z) + (1-z^{-1})X_2(z) = z^{-2}V_{in}(z) + (1-z^{-1})^2 V_{noise2}(z)$$

Example of oversampling DAC

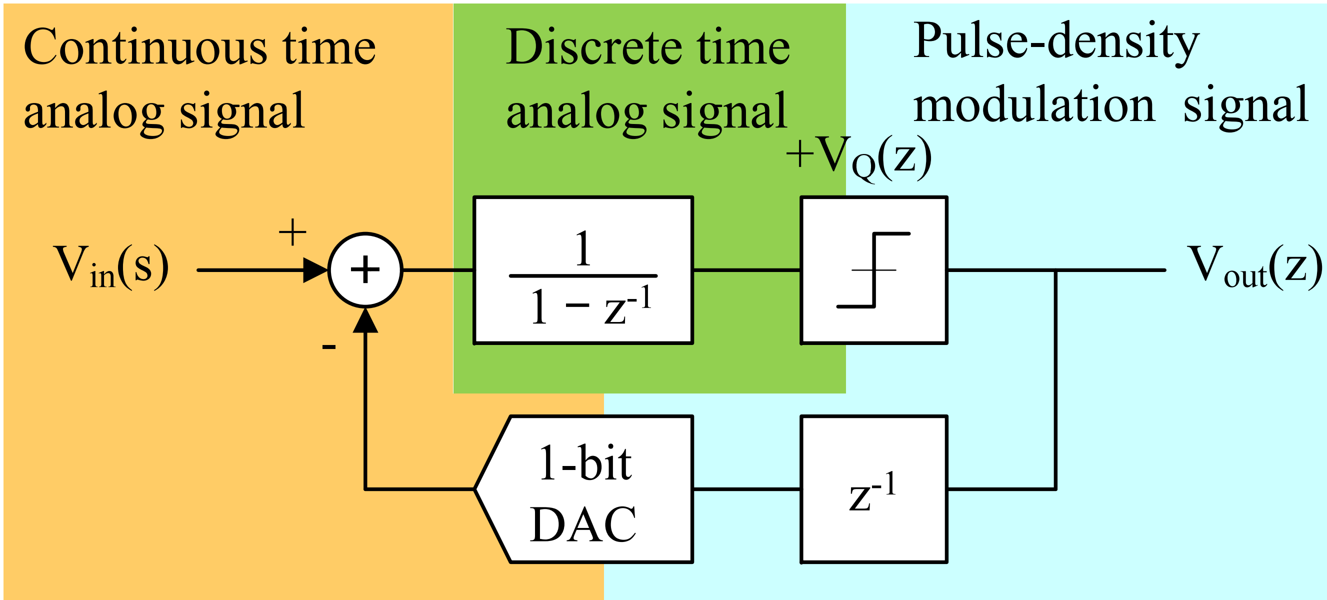




SOI-CMOS 0.6um, 16bit, 2nd order DSM, OSR=128

3.3 Delta-Sigma ADC

Principle of analog DSM



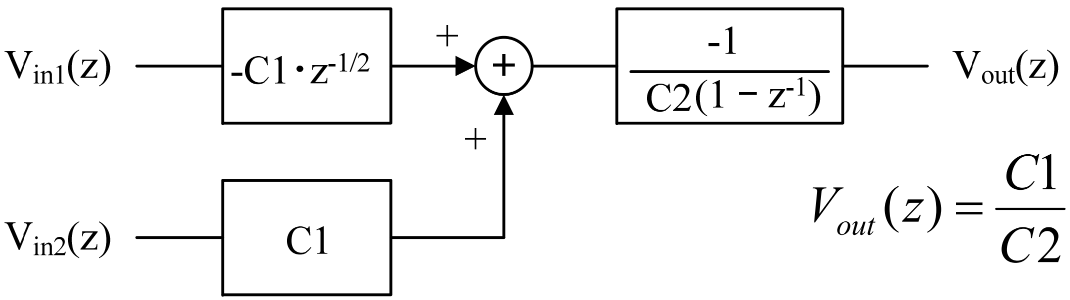
$$V_{out}(z) = V_{in}(z) + (1 - z^{-1})^M \, V_Q(z)$$

Pulse-density modulated signal

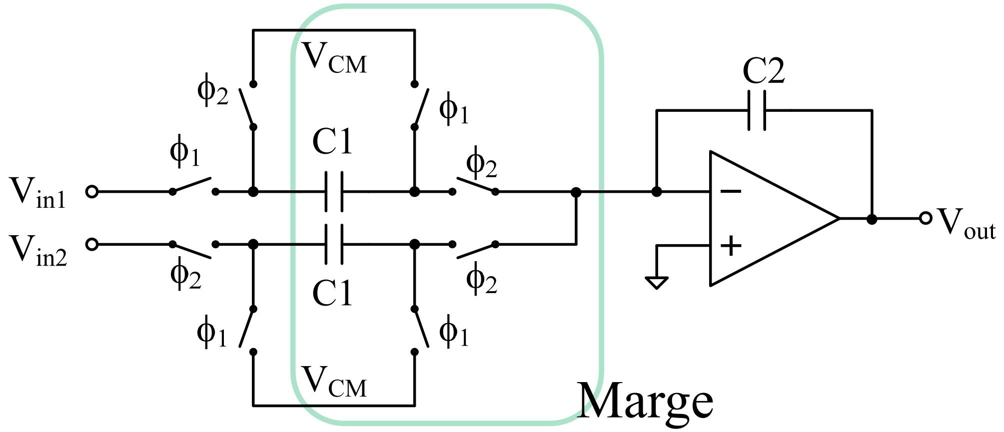
Continuous time analog signal

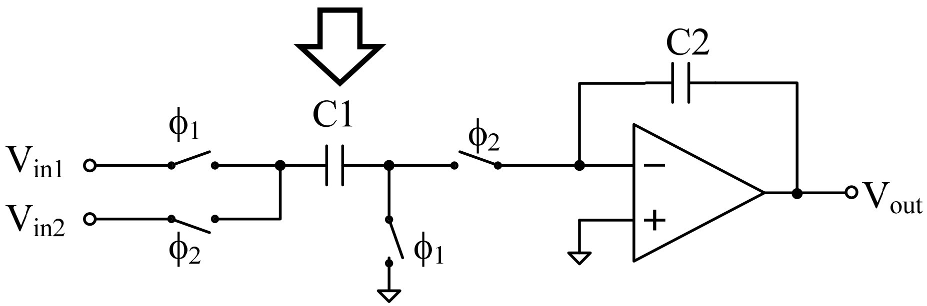
Quantization noise

DAI with reference input



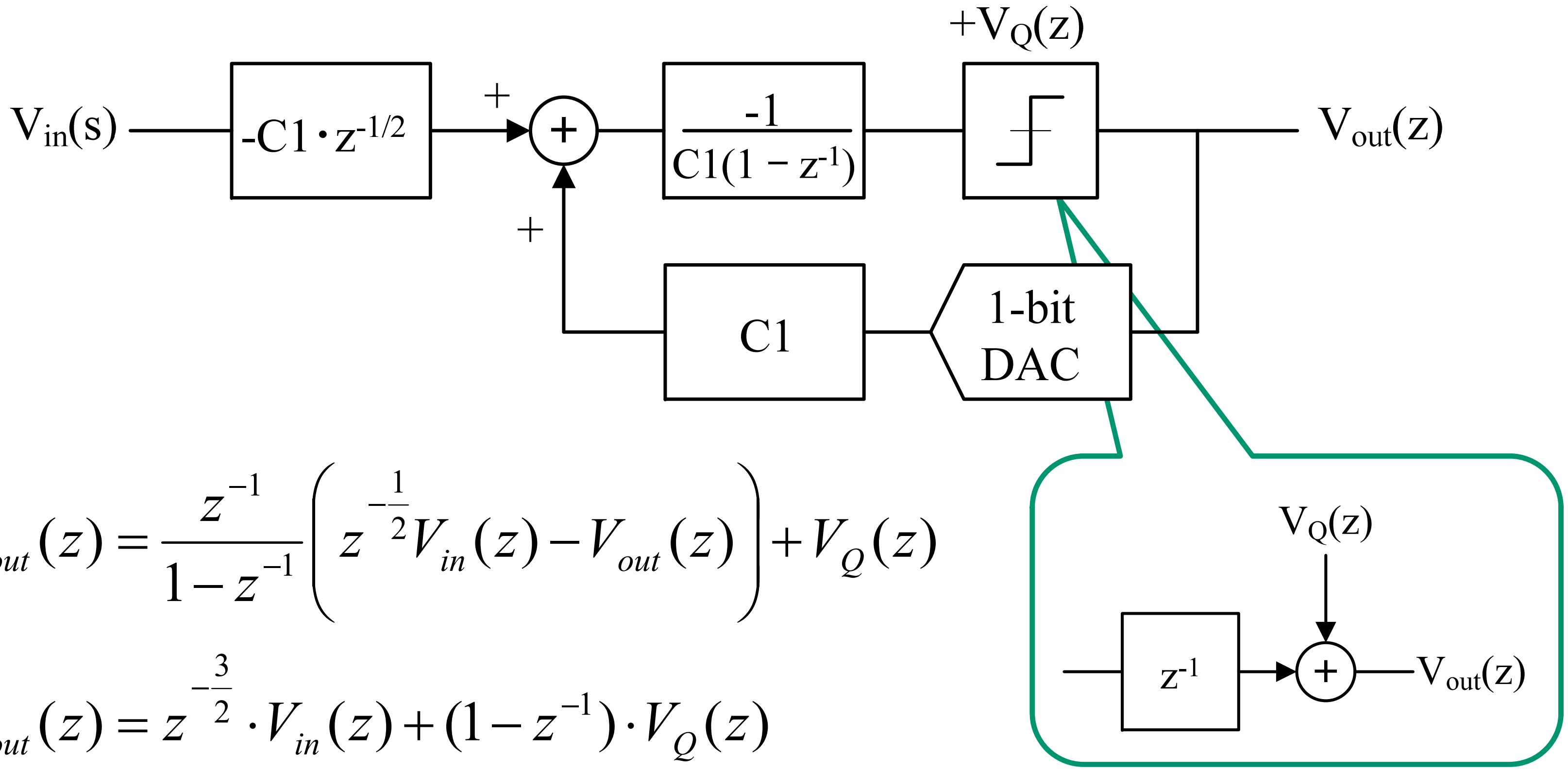
$$V_{out}(z) = \frac{C1}{C2}\frac{1}{1-z^{-1}}\{z^{-\frac{1}{2}}V_{in1}(z) - V_{in2}(z)\}$$





2-input DAI

Architecture of delta-sigma ADC



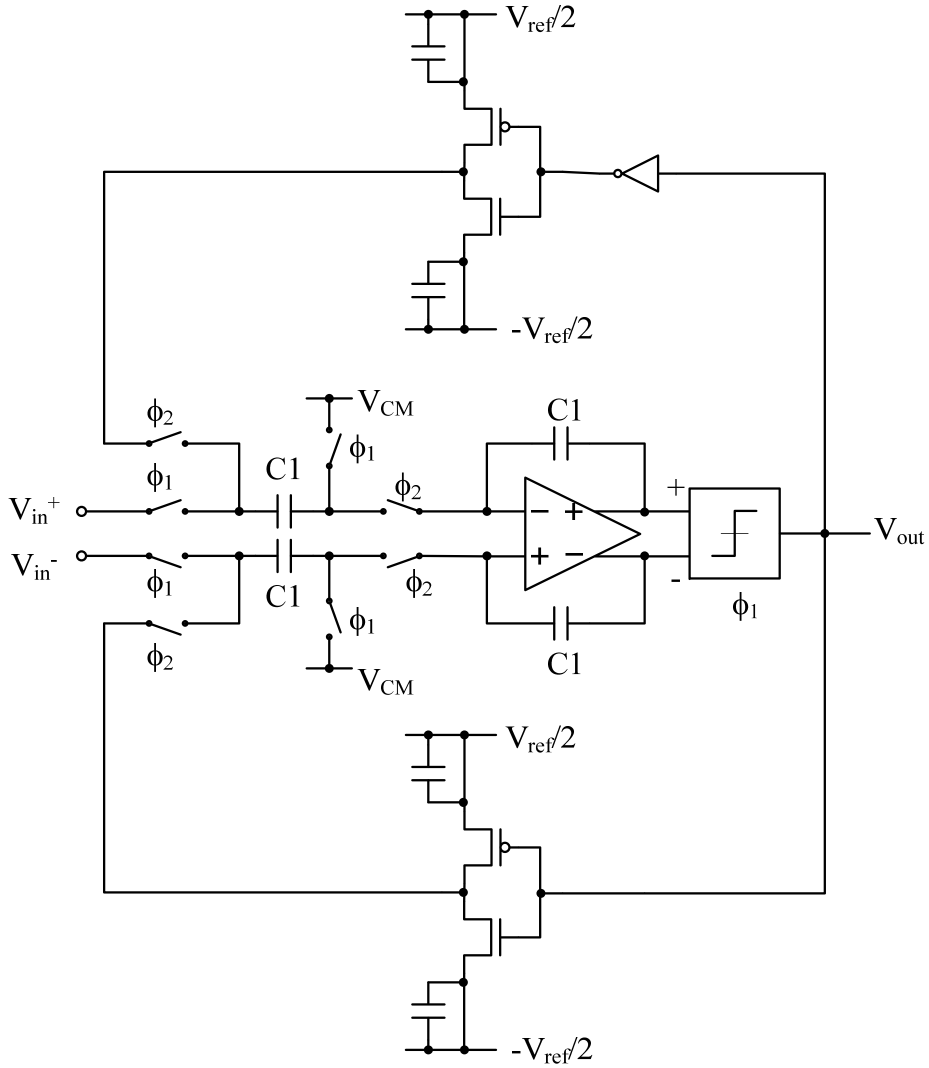
$$V_{out}(z) = \frac{z^{-1}}{1-z^{-1}}\left(z^{-\frac{1}{2}}V_{in}(z) - V_{out}(z)\right) + V_Q(z)$$

$$V_{out}(z) = z^{-\frac{3}{2}} \cdot V_{in}(z) + (1-z^{-1}) \cdot V_Q(z)$$

Transfer function of comparator

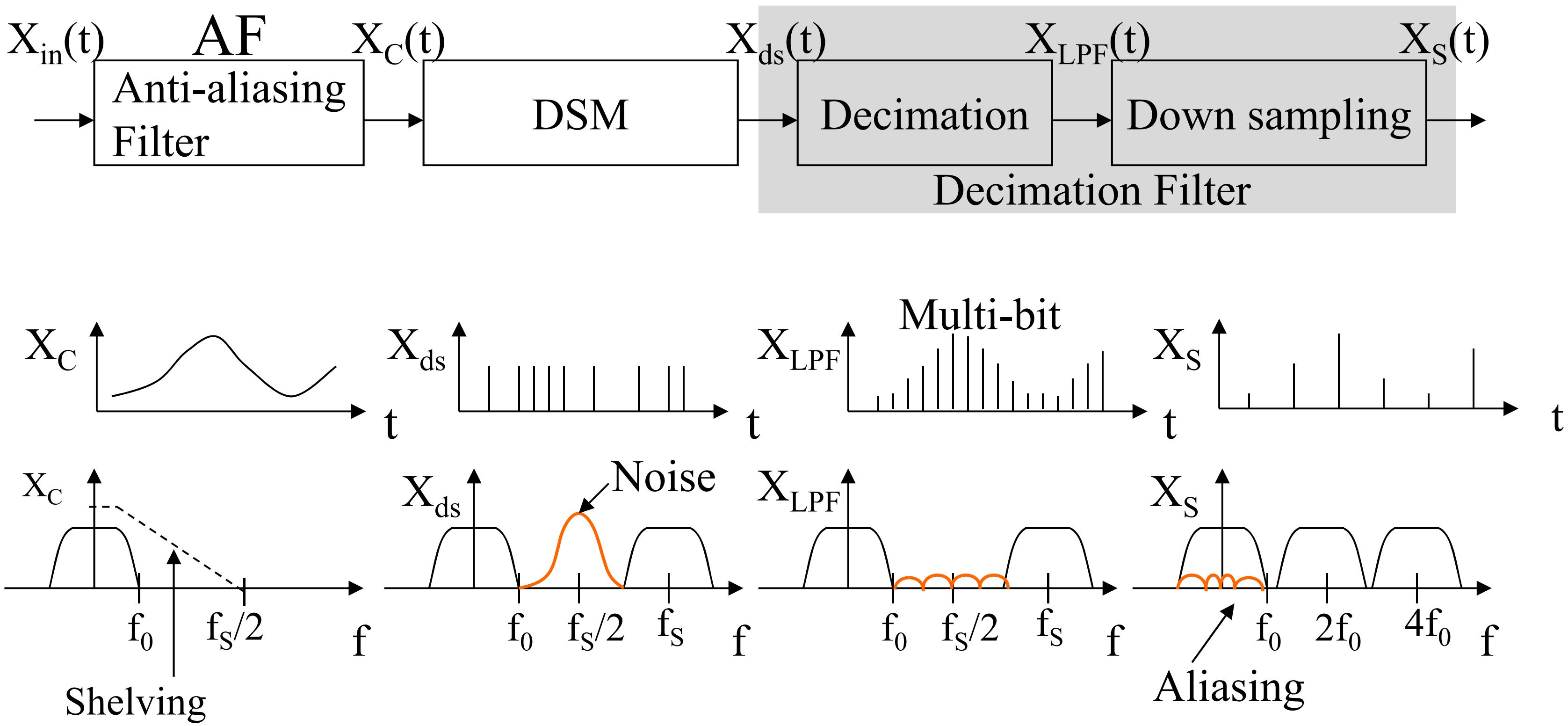
Full differential implementation

Analog input

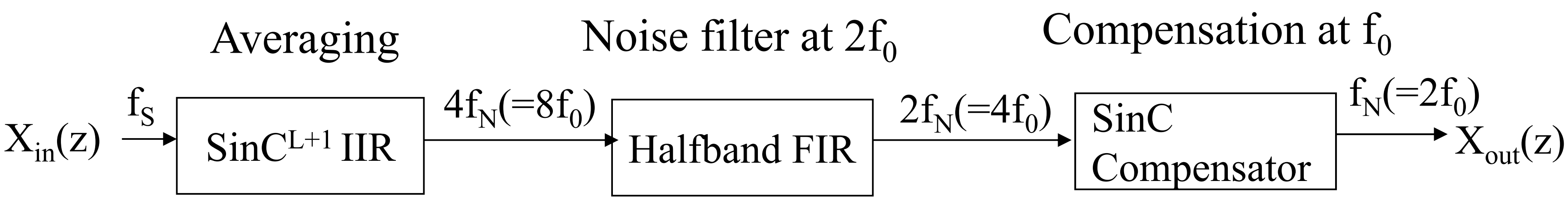


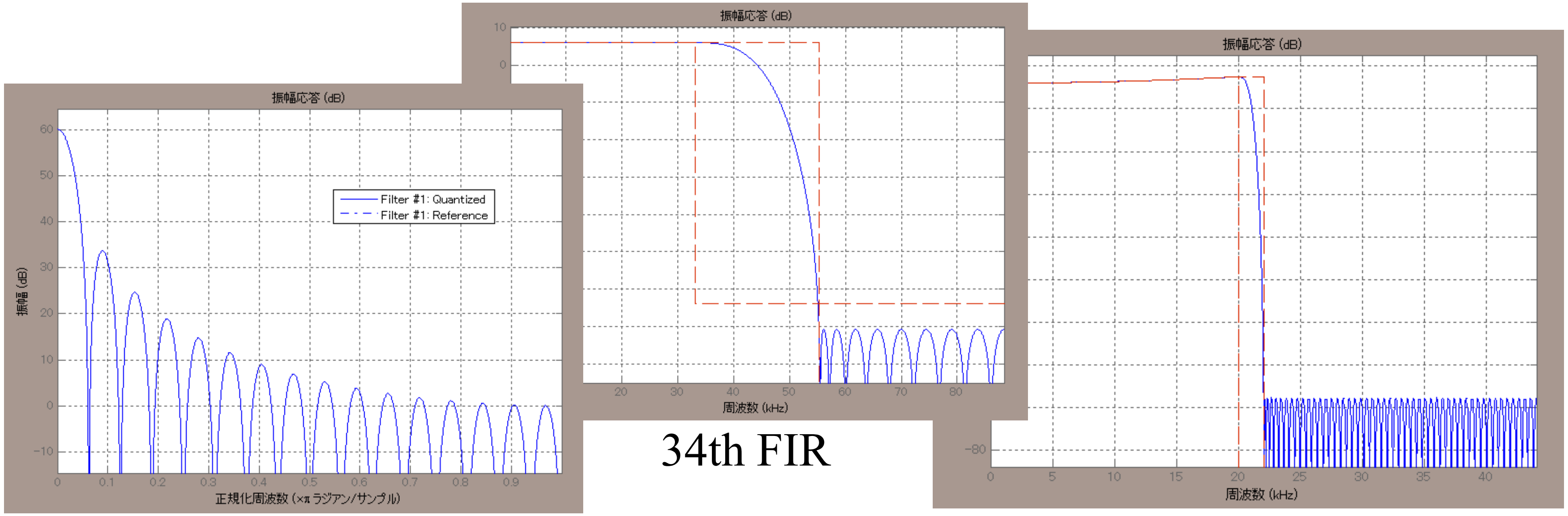
Pulse-density modulation

Conversion to binary signal



Structure of decimation filter





SinC IIR

34th FIR

186th FIR

Design of SinC^{L+1} filter

Averaging of M data $T_A = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i} \equiv \frac{X_{out}(z)}{X_{in}(z)}$

$$MX_{out}(z) = \{\sum_{i=0}^{M-1} z^{-i}\}X_{in}(z) = (z^{-1} + z^{-2} + \cdots + z^{-M})X_{in}(z) + (1 - z^{-M})X_{in}(z)$$

$$= Mz^{-1}X_{out}(z) + (1 - z^{-M})X_{in}(z)$$

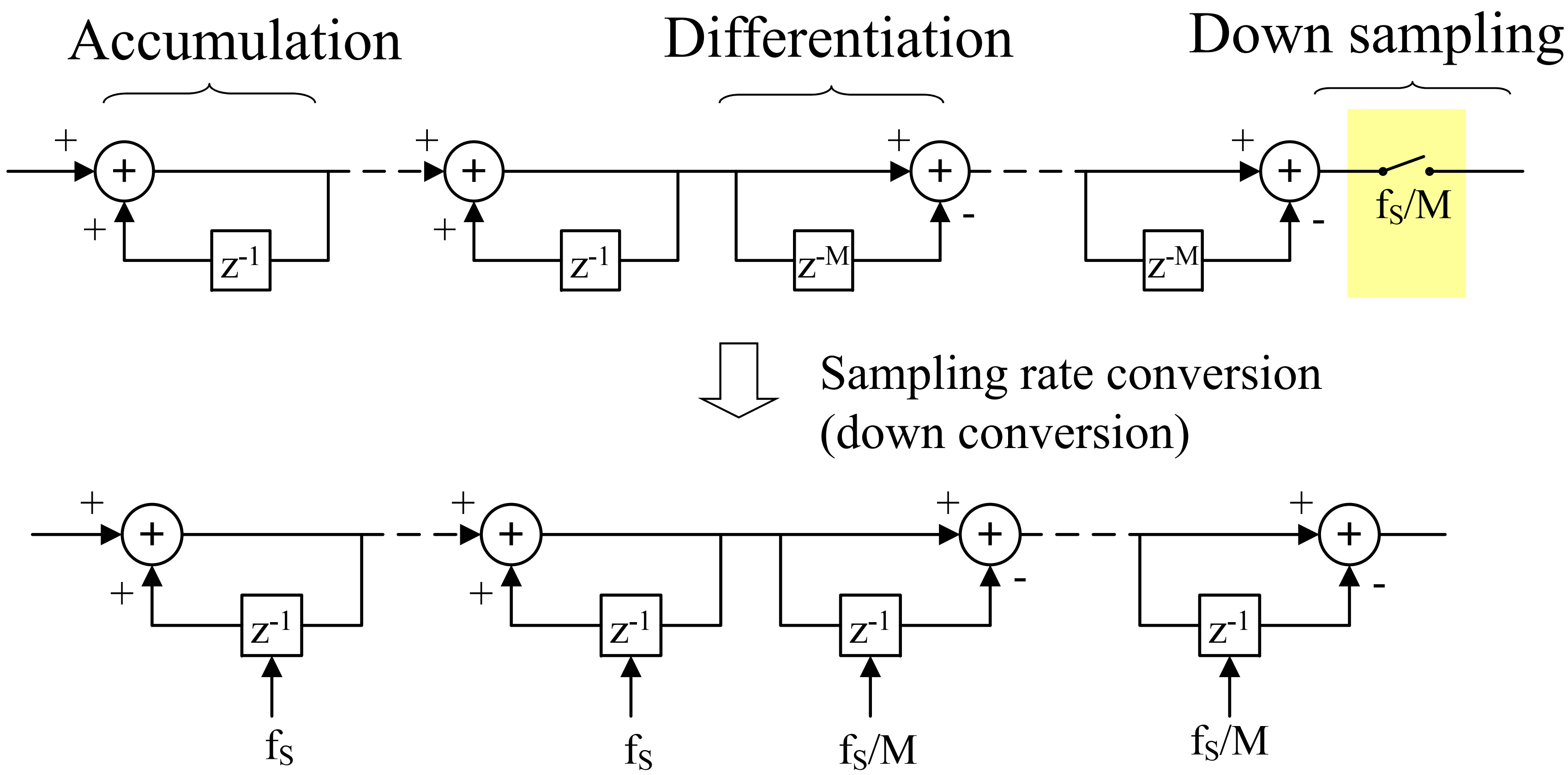
$$T_A = \frac{1}{M}\frac{1 - z^{-M}}{1 - z^{-1}}$$

SinC^{L+1} Filter $H_{SinC} = \frac{1}{M^{L+1}}\left[\frac{1 - z^{-M}}{1 - z^{-1}}\right]^{L+1}$

$$= \frac{1}{(1 - z^{-1})^{L+1}} (1 - z^{-M})^{L+1} \frac{1}{M^{L+1}}$$

Accumulation Differentiation Constant

Implementation of SinC^{L+1} Filter



SinC filter = CIC (Cascaded Integration-Comb) filter

Order of SinC^{L+1} Filter

Without noise shaping $SNR = 6.02 \cdot ENOB + 1.76$

With 1st-order noise shaping $SNR = 6.02 + 1.76 - 5.17 + 30\log OSR$

With 2nd-order noise shaping $SNR = 6.02 + 1.76 - 12.9 + 50\log OSR$

⇩

With 1st-order noise shaping $ENOB = 1 + (-5.17 + 30\log OSR)/6.02$

With 2nd-order noise shaping $ENOB = 1 + (-12.9 + 50\log OSR)/6.02$

Number of bits of decimation filter $N_{out} = N_{stage}\log_2(OSR)$

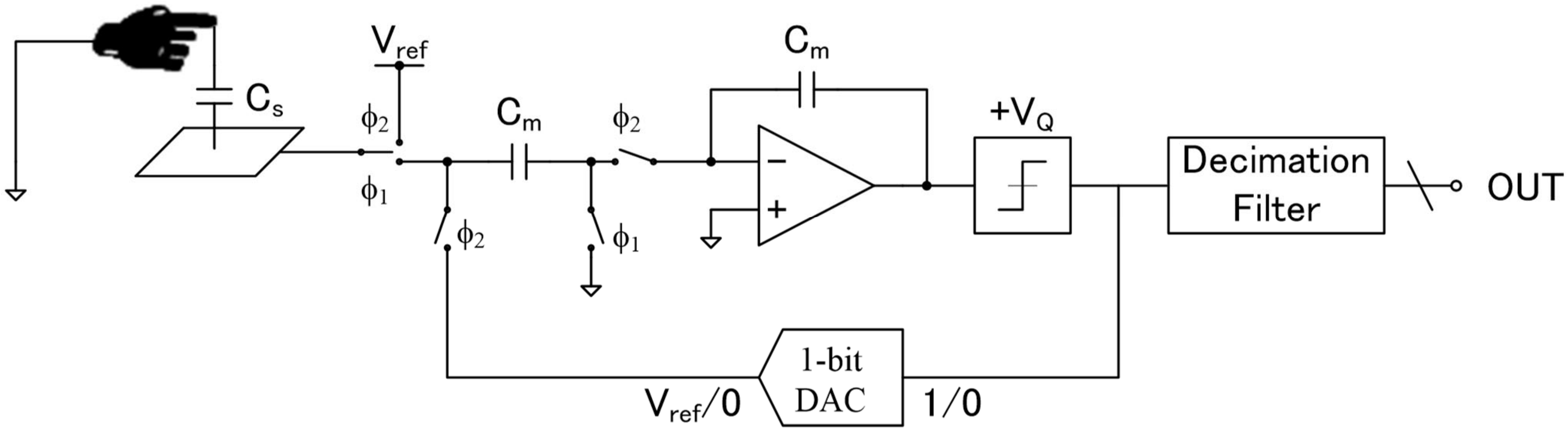
N_{out} must be larger than ENOB.

With 1st-order noise shaping $N_{stage} > \frac{ENOB}{\log_2(OSR)} \approx 1.5 > L$

With 2nd-order noise shaping $N_{stage} > \frac{ENOB}{\log_2(OSR)} \approx 2.5 > L$

where L is a order of the noise shaping.

Application example of cap sense (touch panel)



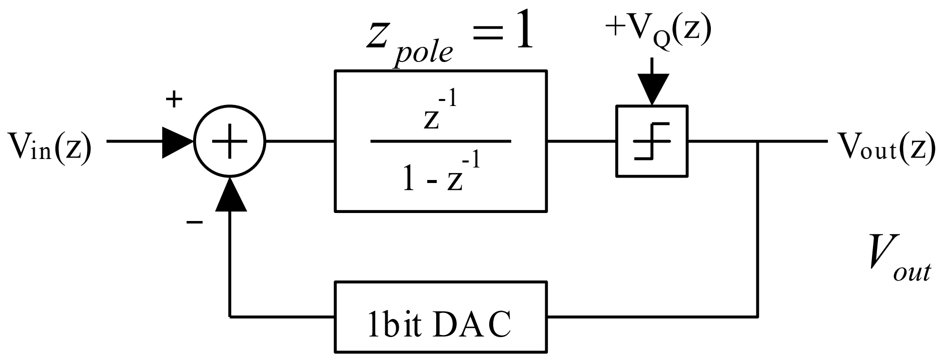
$$V_{out}(z) = z^{-\frac{3}{2}} \cdot V_{ref}(z) \frac{C_s}{C_s + C_m} + (1 - z^{-1}) \cdot V_Q(z)$$

When f = 0Hz and z = 1 (DC), $C_S = \dfrac{V_{out}}{V_{ref} - V_{out}} C_m$

3.4 Band-pass Delta-Sigma ADC

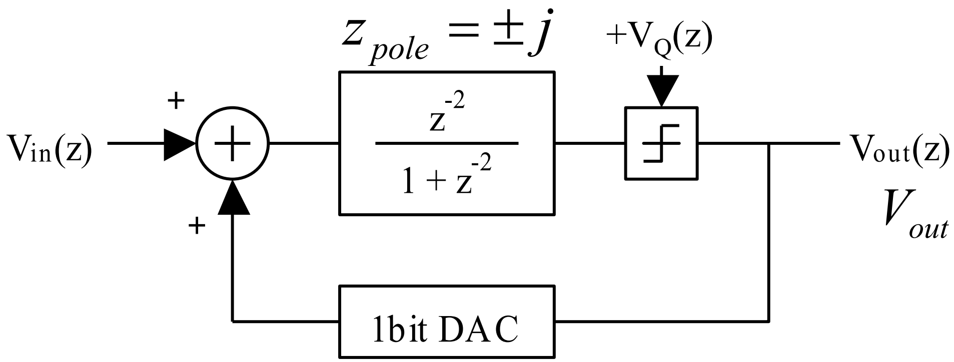
Transfer function of band-pass DSM

Low-pass DSM



$$V_{out}(z) = z^{-1}V_{in}(z) + \underbrace{(1 - z^{-1})}_{z_{pole} = 1}V_{noise}(z)$$

Band-pass DSM



$$V_{out}(z) = z^{-2}V_{in}(z) + \underbrace{(1 + z^{-2})}_{z_{pole} = \pm j}V_{noise}(z)$$

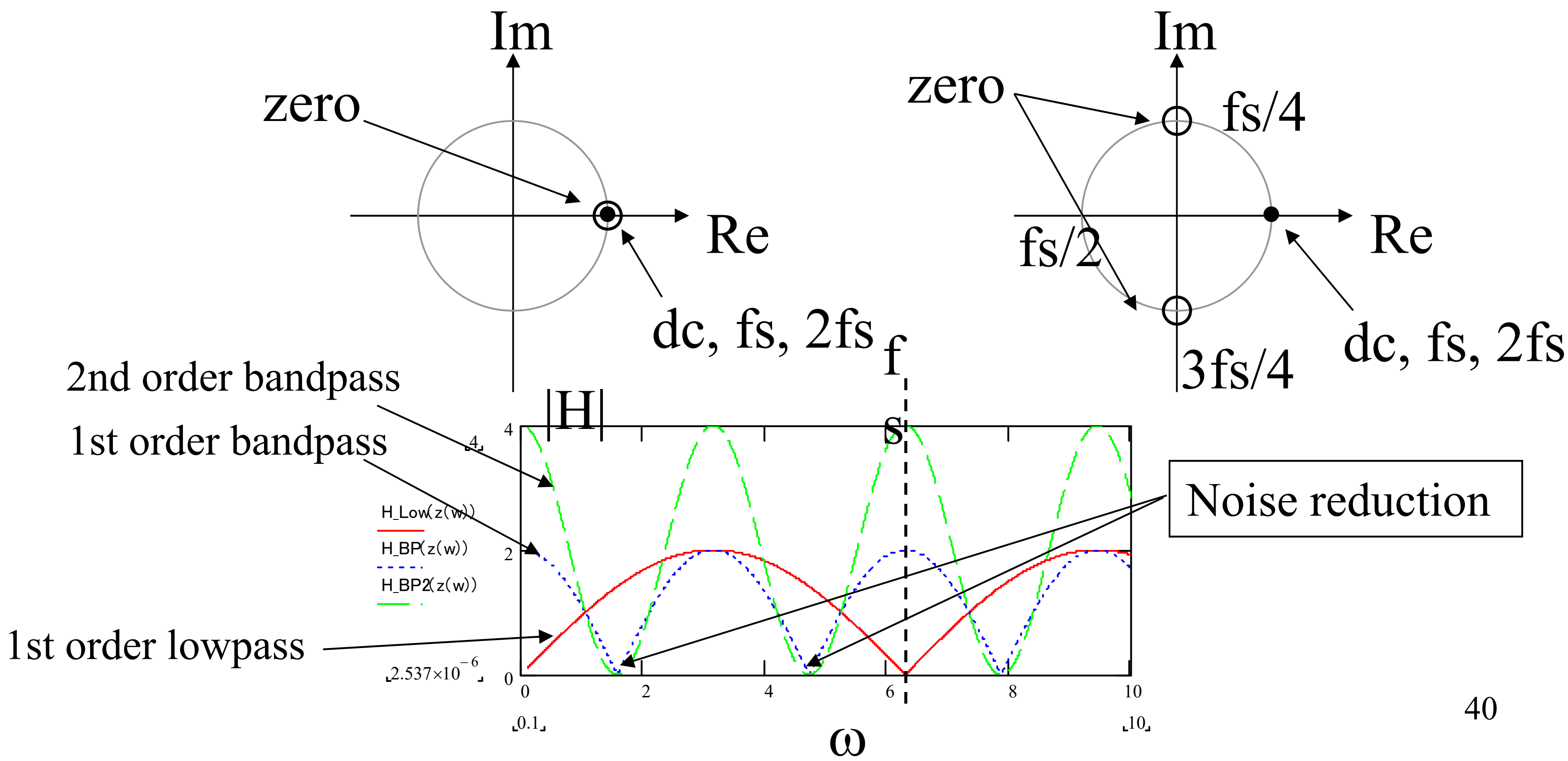
Noise shaping of band-pass DSM

Low-pass

$$V_{out}(z) = z^{-1}V_{in}(z) + (1 - z^{-1})V_{noise}(z)$$

Band-pass

$$V_{out}(z) = z^{-2}V_{in}(z) + (1 + z^{-2})V_{noise}(z)$$

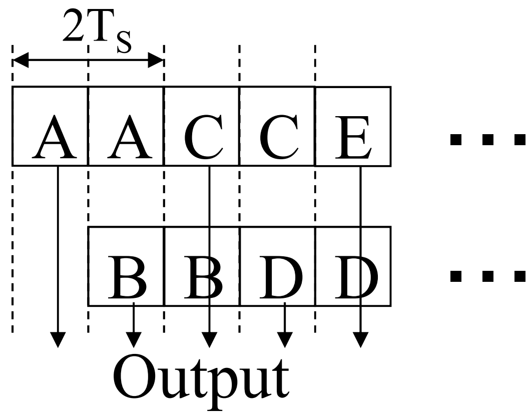


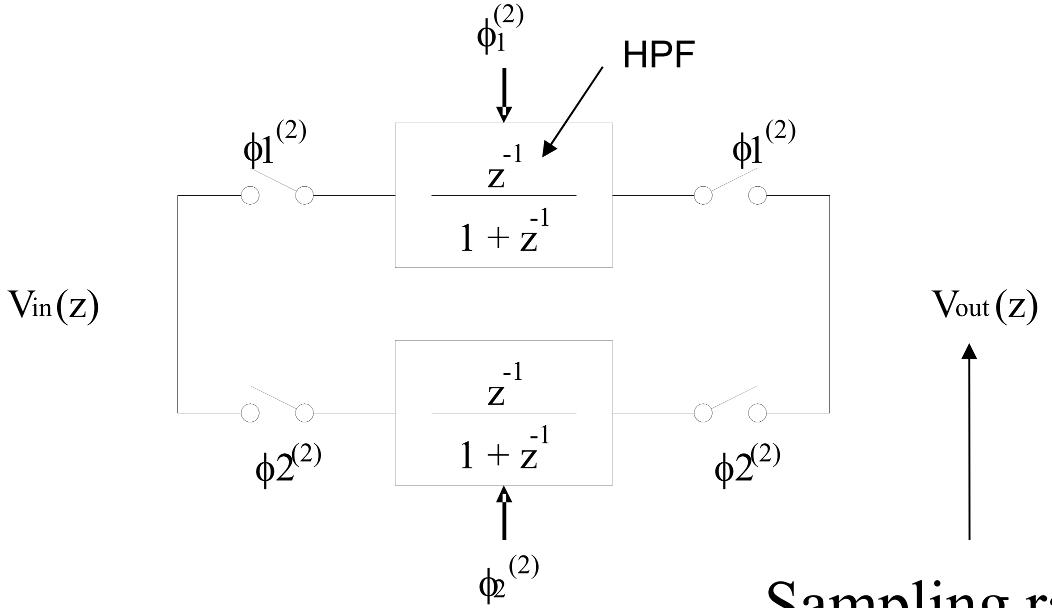
z^{-2} operation with N-Path technique

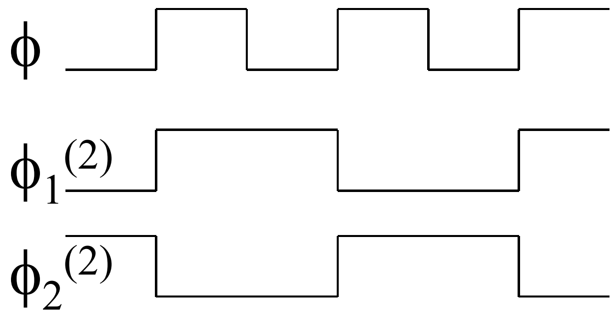
$T_S \rightarrow 2T_S$

$$z^{-1} = e^{-sT_S} \Rightarrow z^{-2} = e^{-s \cdot 2T_S} \Rightarrow$$

2 path technique



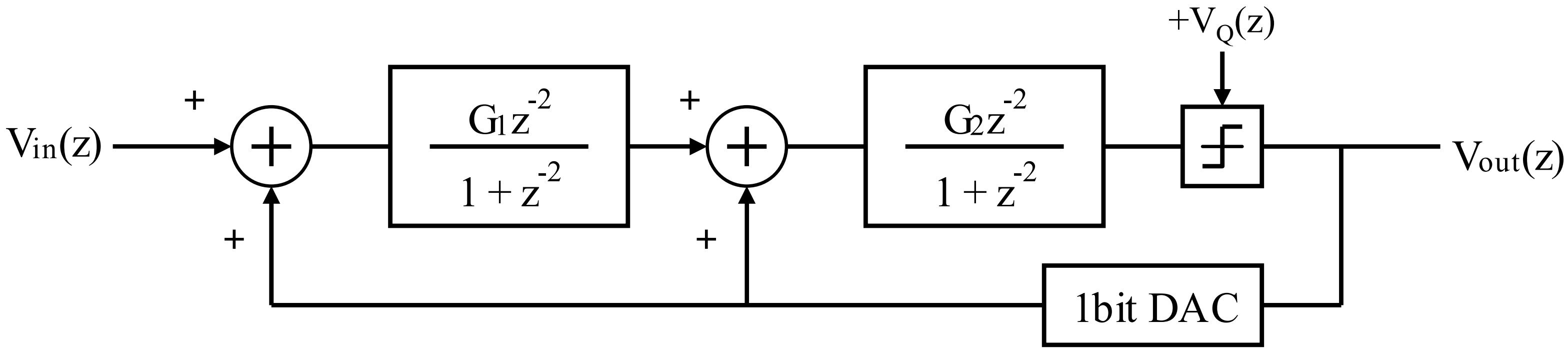




Sampling rate = T_S

4th order band-pass DSM

High-order band-pass ADC is often used for the wireless communication systems.



$$\begin{cases} G_1 = -0.5 \\ G_2 = 2 \end{cases} \Rightarrow V_{out}(z) = -z^{-4}V_{in}(z) + \underbrace{(1+z^{-2})^2}_{z=\pm j} V_{noise}(z)$$

Exercise

Question:
Derive the transfer function of the block diagram shown in the previous slide.

Example solution:

$$V_{out}(z) = \frac{G_2 z^{-2}}{1+z^{-2}}\{\frac{G_1 z^{-2}}{1+z^{-2}}(V_{in}(z)+V_{out}(z))+V_{out}(z)\}+V_{noise}(z)$$

$$(1-\frac{G_1 G_2 z^{-4}}{(1+z^{-2})^2}-\frac{G_2 z^{-2}}{1+z^{-2}})\cdot V_{out}(z) = \frac{G_1 G_2 z^{-4}}{(1+z^{-2})^2}V_{in}(z)+V_{noise}(z)$$

$$\frac{(1+z^{-2})^2 - G_1 G_2 z^{-4} - G_2 z^{-2}(1+z^{-2})}{(1+z^{-2})^2}V_{out}(z) = \frac{G_1 G_2 z^{-4}}{(1+z^{-2})^2}V_{in}(z)+V_{noise}(z)$$

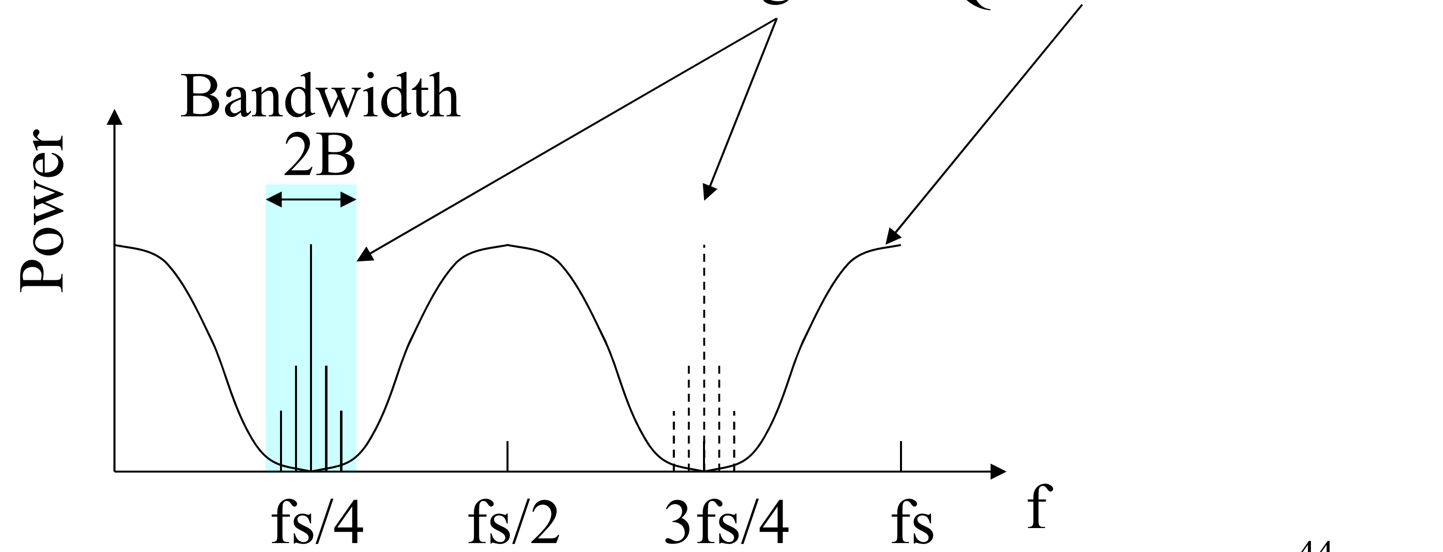
$$V_{out}(z) = \frac{G_1 G_2 z^{-4}\cdot V_{in}(z)+(1+z^{-2})^2\cdot V_{noise}(z)}{1+2z^{-2}+z^{-4}-G_1 G_2 z^{-4}-G_2 z^{-2}-G_2 z^{-4}}$$

Oversampling rate of band-pass ADC

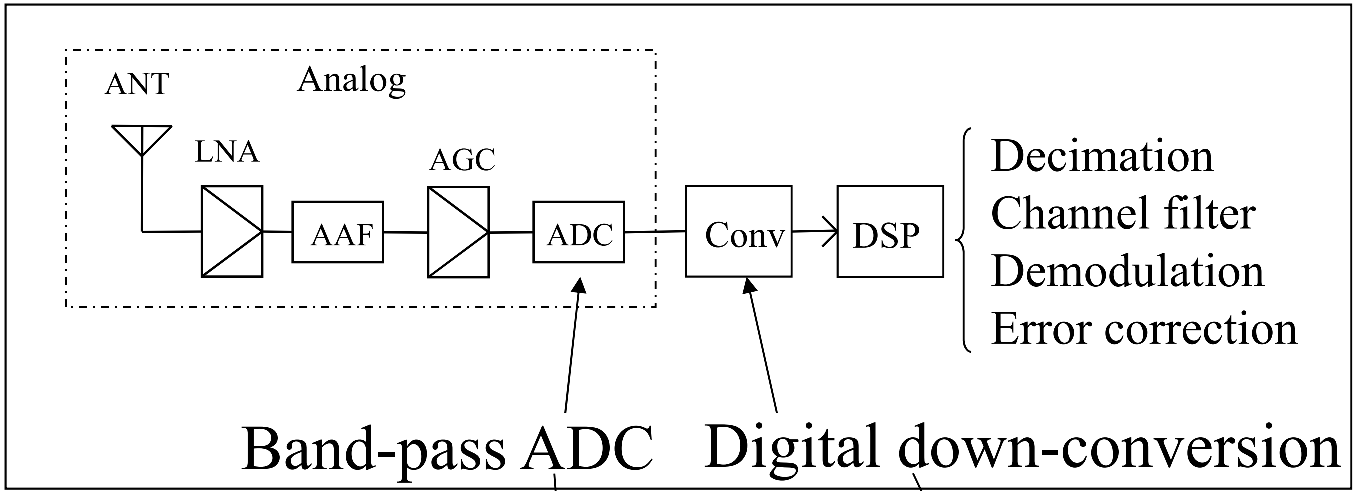
The OSR of the band-pass DSM cannot be determined by the carrier frequency, but should be calculated by the bandwidth of the converted signal.

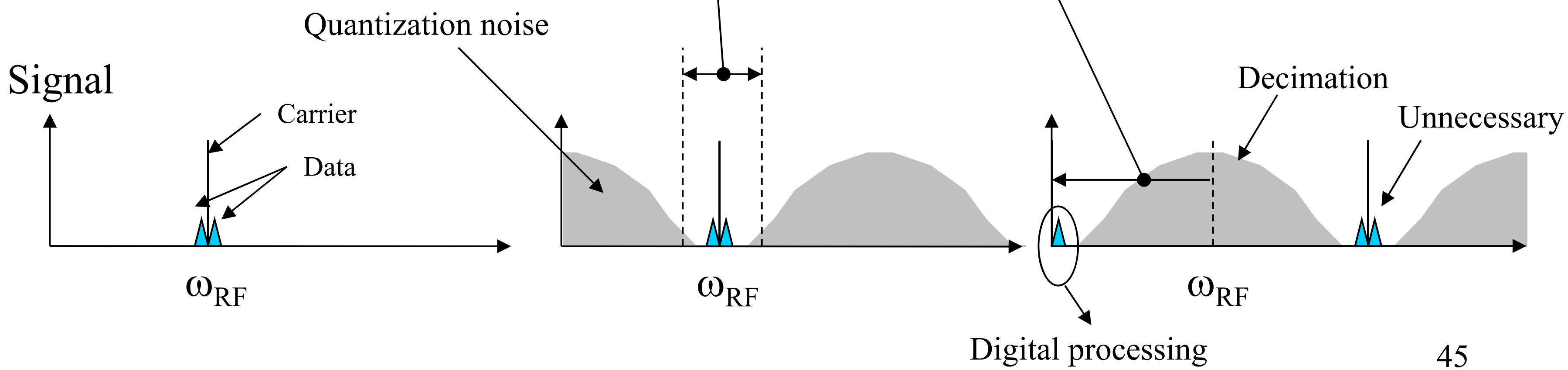
$$OSR = \frac{f_S}{2 \cdot (2B)}$$

$$V_{out}(z) = \underbrace{z^{-4} V_{in}(z)}_{\text{Signal}} + \underbrace{(1+z^{-2})^2 V_Q(z)}_{\text{Quantization noise}}$$



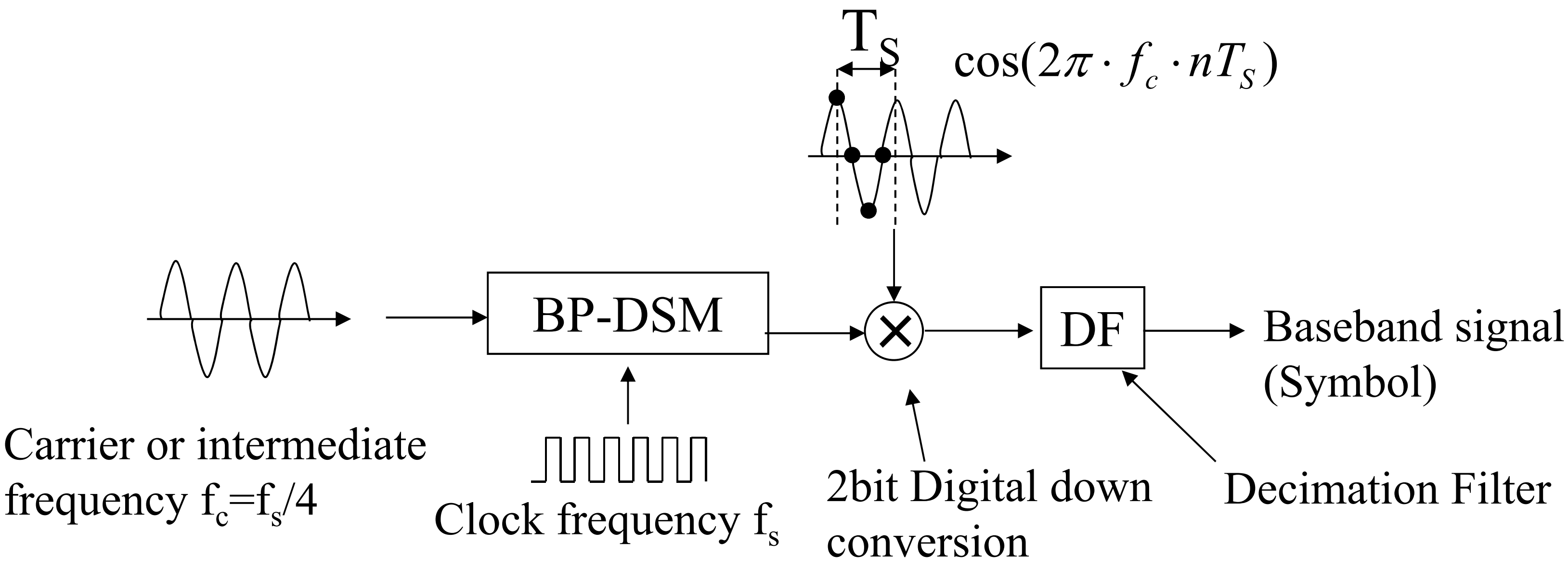
Receiver architecture





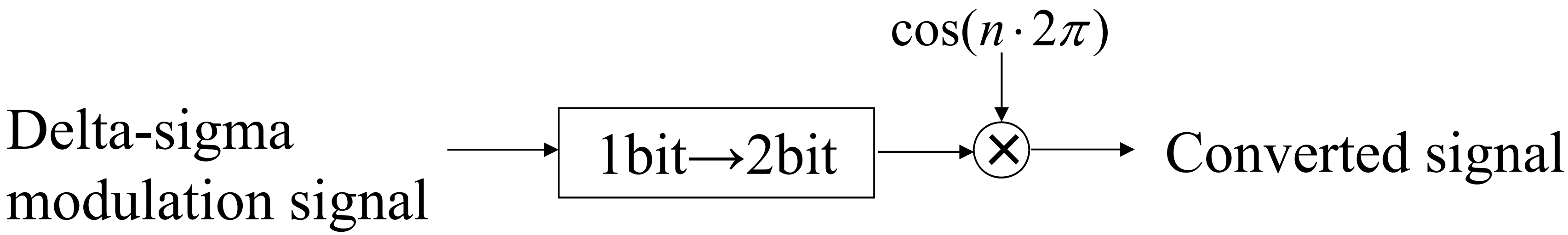
Digital down-conversion

When $f_s = 4f_c$, the digital down conversion can be implemented by 2-bit logic.



$$\cos(2\pi \cdot f_c \cdot nT_S) = \cos(2\pi \frac{f_S}{4} n \frac{1}{f_S}) = \cos(n\frac{\pi}{2}) = \{1,0,-1,0\}$$ 2-bit-at-a-time

Example of 2-bit multiplier



1bit→2bit extension

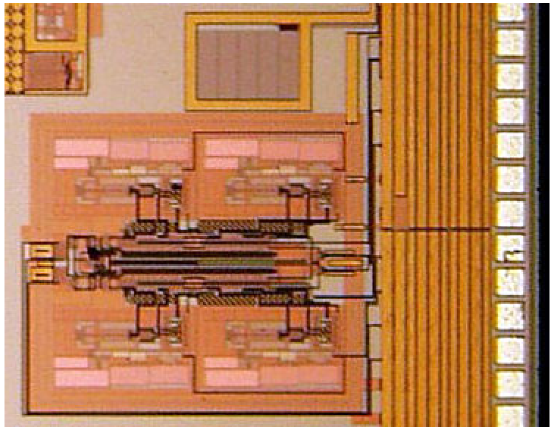
a	A
0	11(-1)
1	01(1)

2bit multiplier

A	B	OUT
11 (-1)	00 (0)	00 (0)
01 (1)	00 (0)	00 (0)
11 (-1)	01 (1)	11 (-1)
01 (1)	01 (1)	01 (1)
11 (-1)	11 (-1)	01 (1)
01 (1)	11 (-1)	11 (-1)
·	·	DC
·	·	DC
·	·	DC

Example of band-pass DSM

CMOS 0.25um,
OSR = 256,
4th-order noise shaping,
ENOB = 14bit



Down conversion, Decimation, and Demodulation