

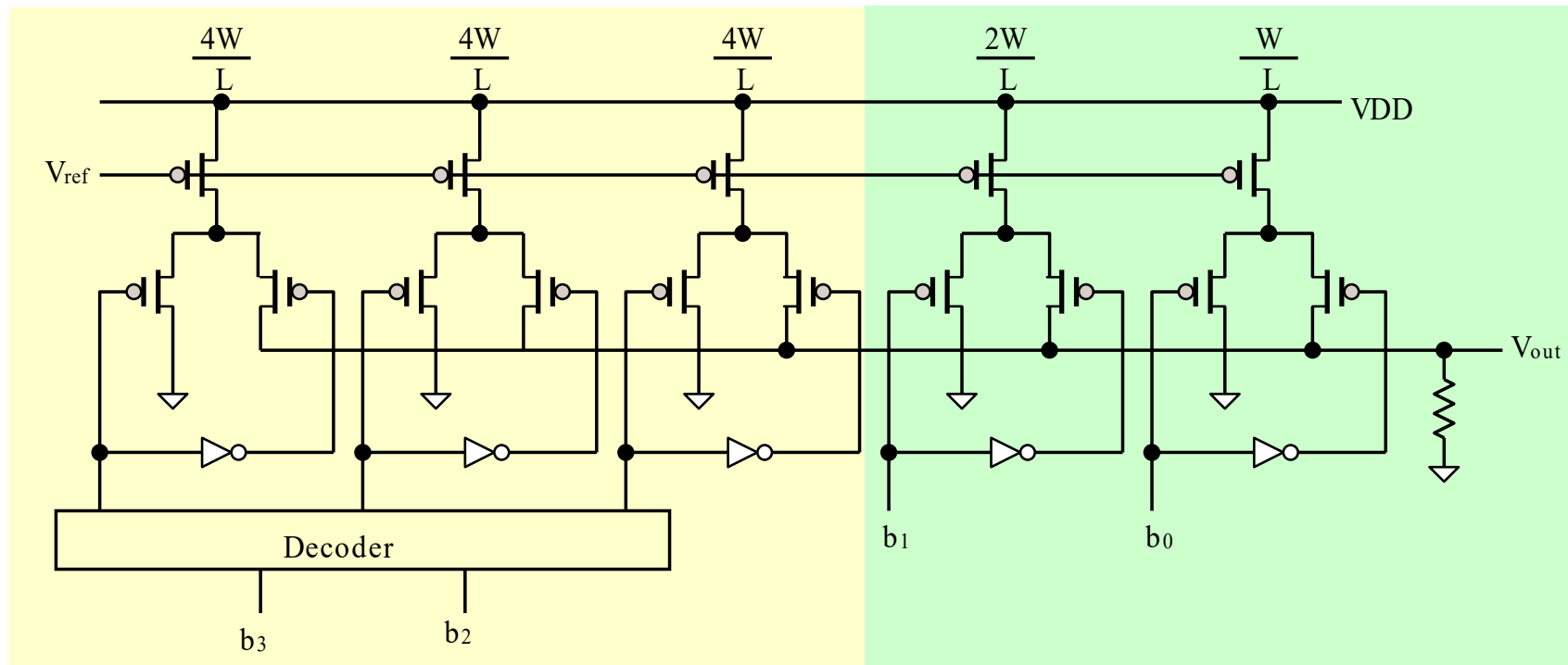
4. Data converters 2

(Nyquist-rate converters)

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Microelectronics Research Lab.
Akio Kitagawa

4.1 Current steering DAC (High speed and no glitch)

Basic circuit

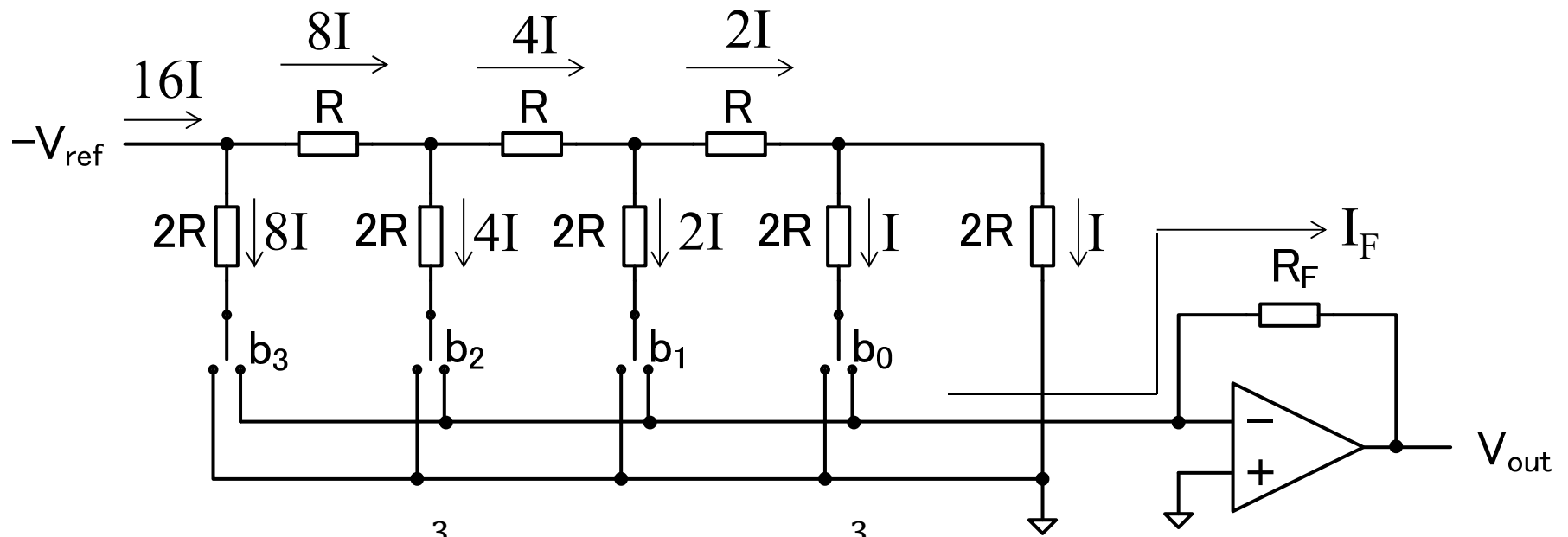


Thermometer code for high-order bits

Binary code for low-order bits

4.2 Current mode R-2R DAC (Small size)

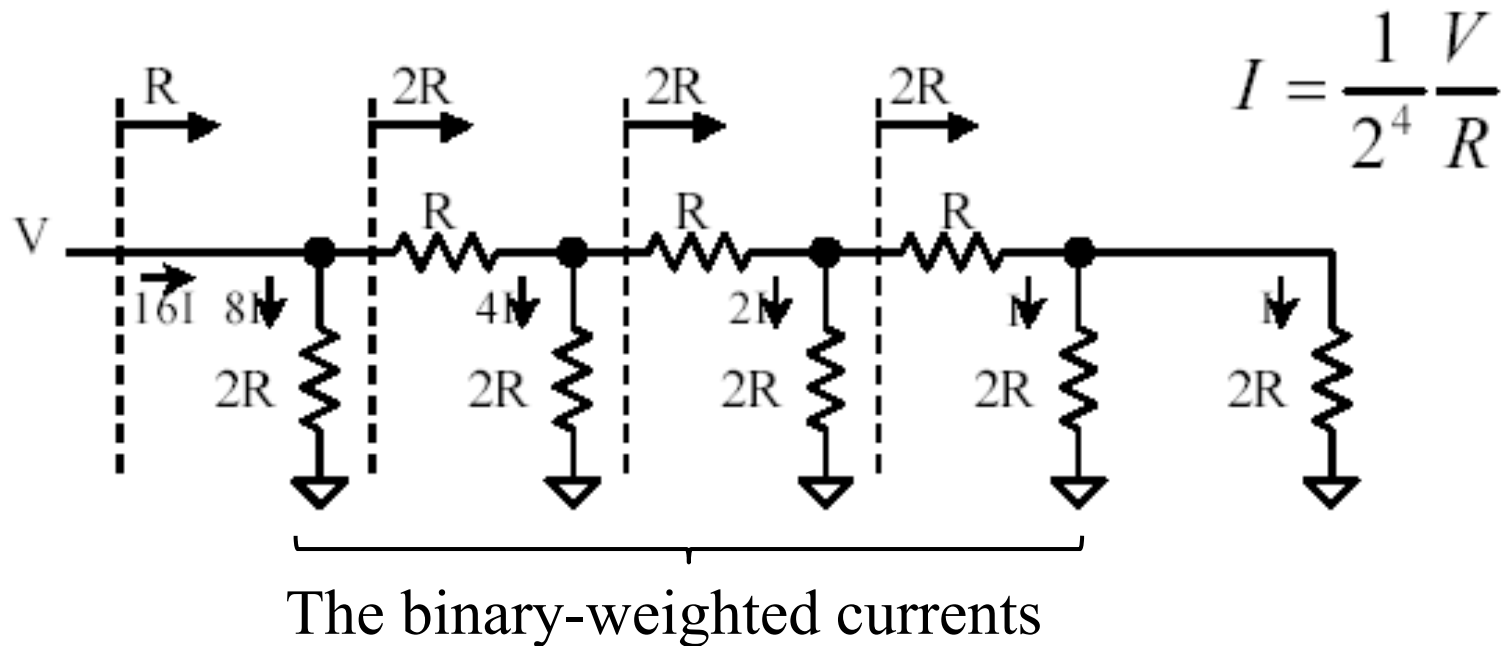
Basic circuit



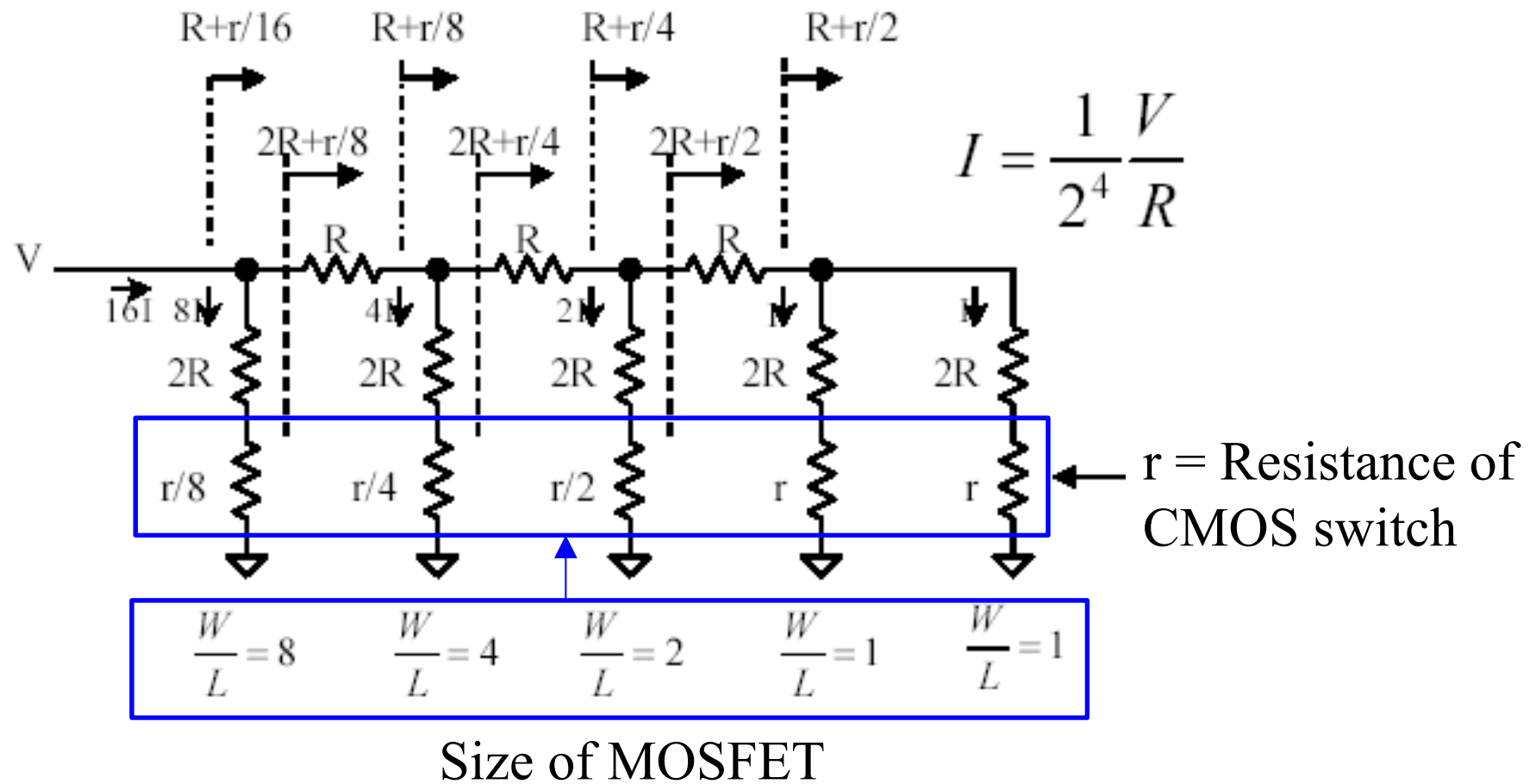
$$I_F = I \sum_{n=0}^3 2^n b_n = -\frac{1}{2^3} \frac{V_{ref}}{R} \sum_{n=0}^3 2^n b_n$$

$$V_{out} = -R_F I_F$$

Principle of operation



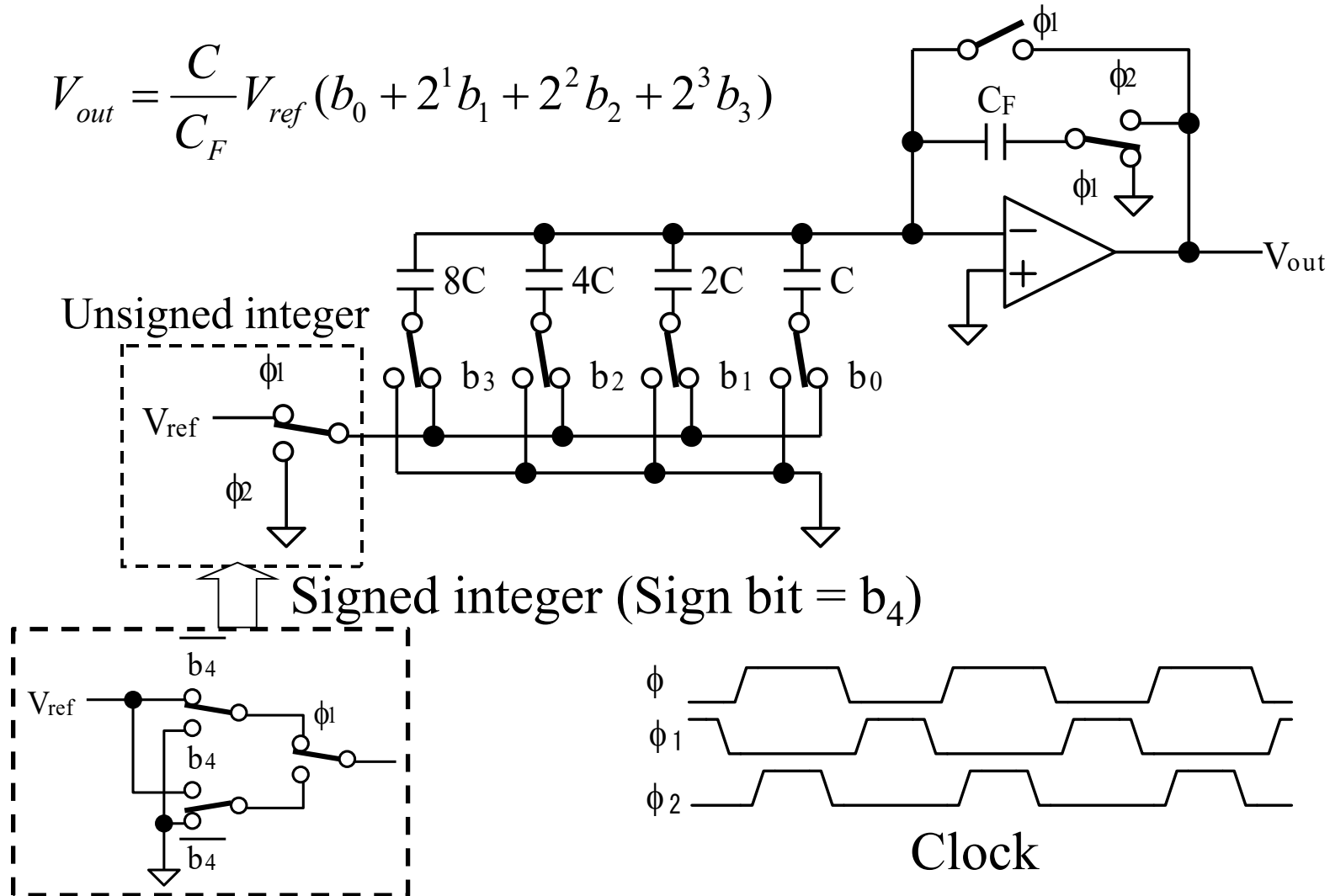
Error reduction



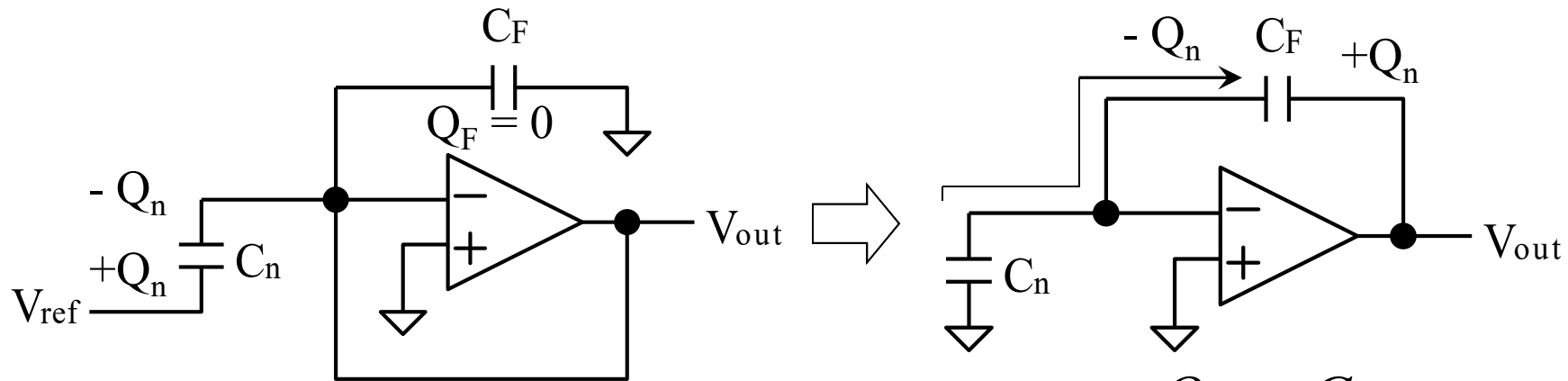
4.3 Charge scaling DAC (High precision and low power consumption)

Basic circuit

$$V_{out} = \frac{C}{C_F} V_{ref} (b_0 + 2^1 b_1 + 2^2 b_2 + 2^3 b_3)$$



Principle of operation



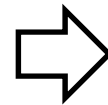
$$V_{ref} = \frac{Q_n}{C_n}$$

$$V_{out} = \frac{Q_n}{C_F} = \frac{C_n}{C_F} V_{ref}$$

$$\text{Conversion gain} = \frac{C_n}{C_F}$$

Phase ϕ_1

- Charge of C_n
- Discharge of C_F

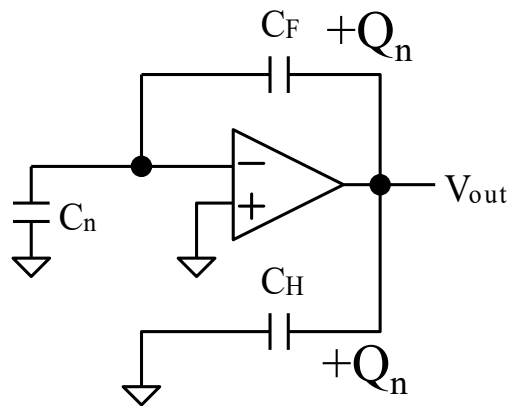
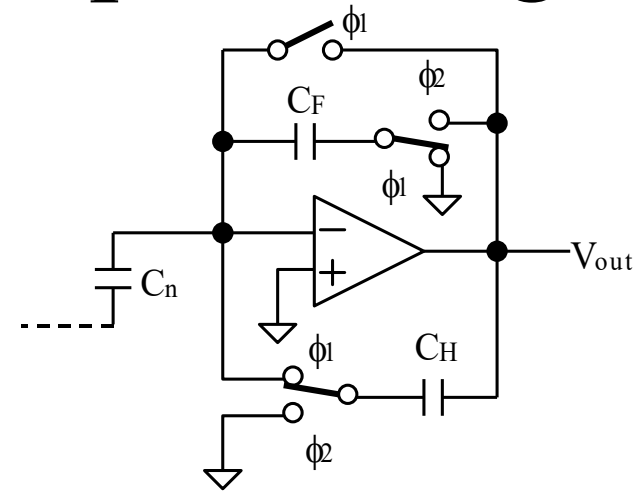


Phase ϕ_2

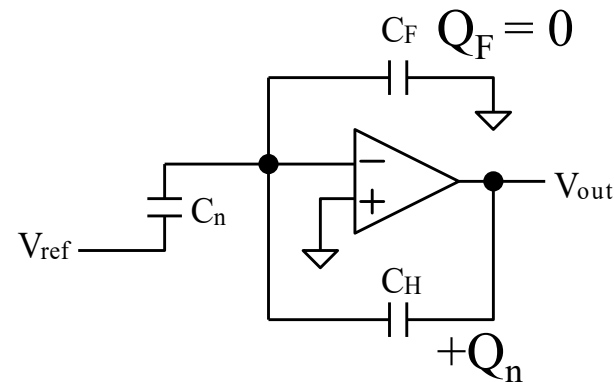
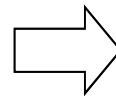
- Charge transfer of $-Q_n$
- Voltage output

Hold circuit of output voltage

The basic DAC circuit outputs the converted voltage only for ϕ_2 phase. The hold circuit is added to hold the output for ϕ_1 phase.



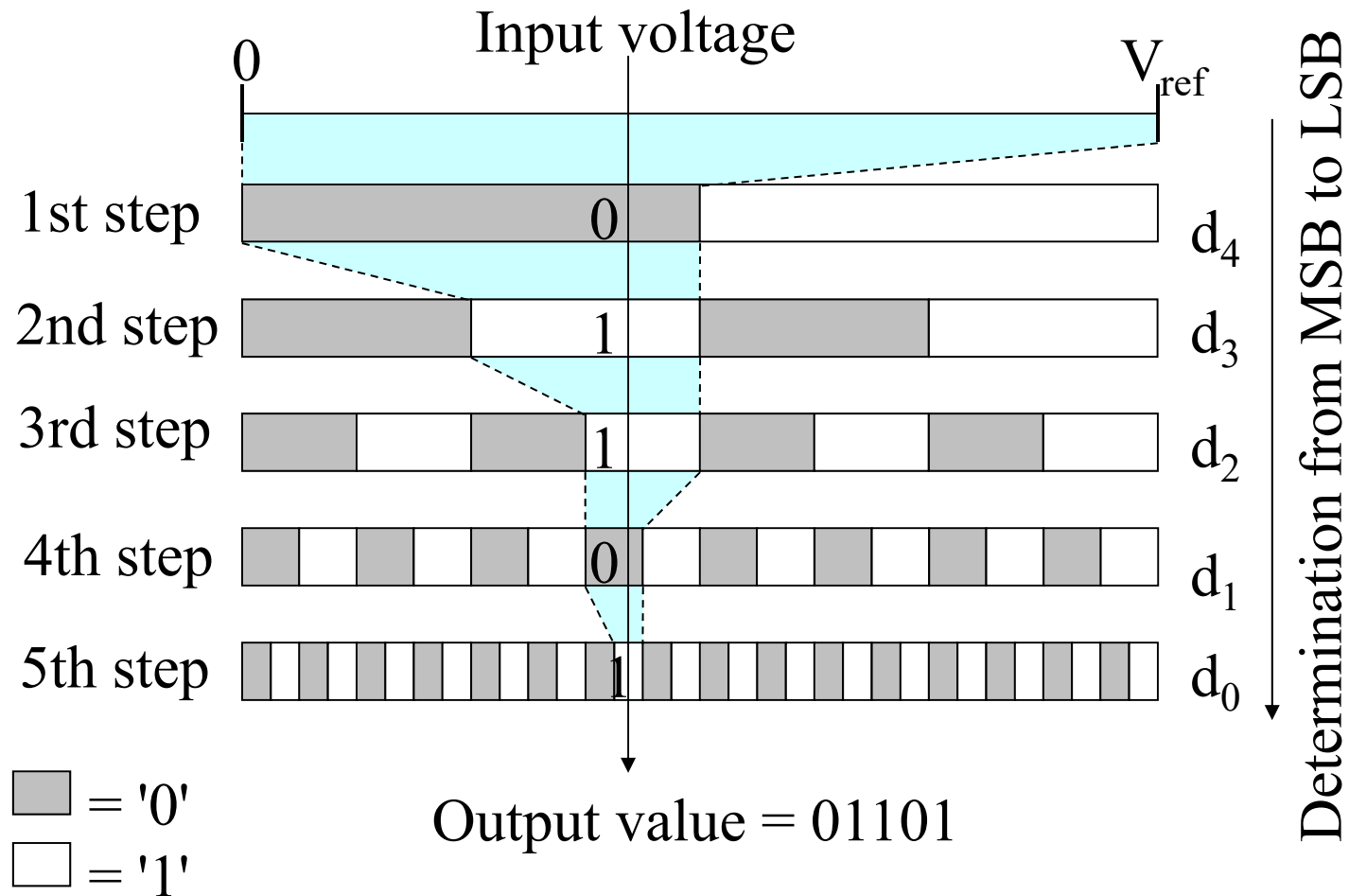
Sample mode in the phase ϕ_2



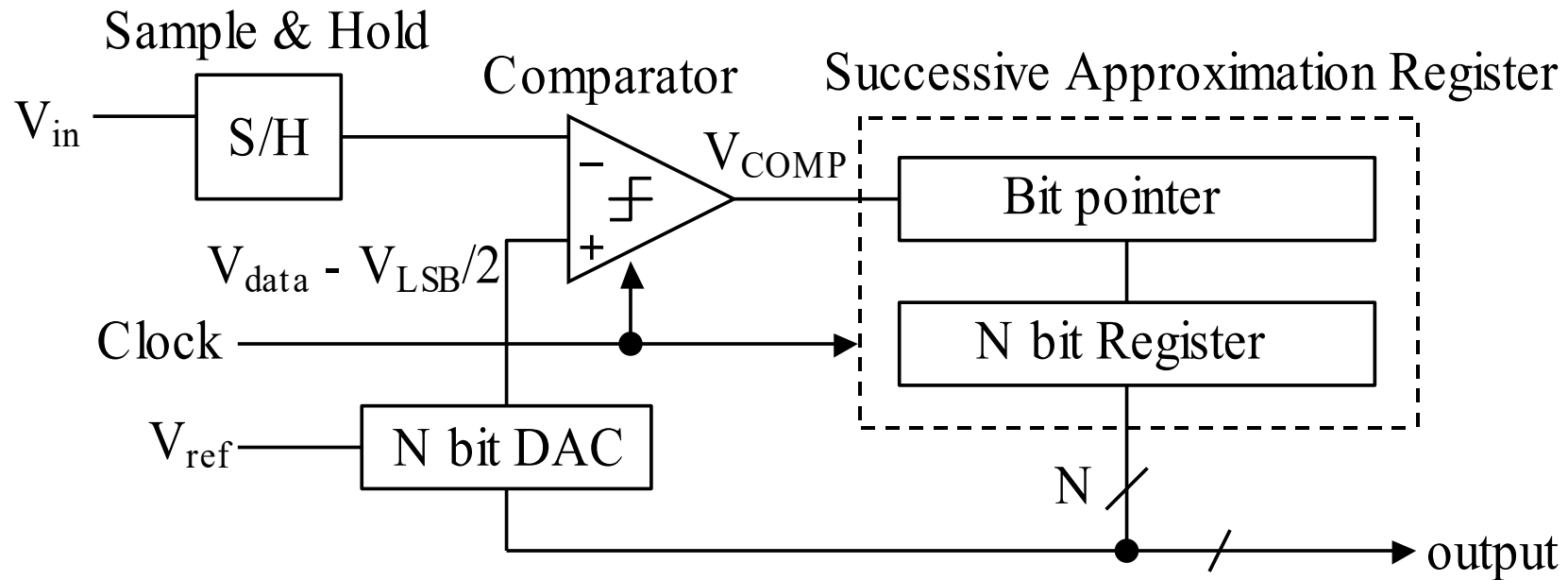
Hold mode in phase ϕ_1

4.4 Successive Approximation Register (SAR) ADC (High precision and low power consumption)

Principle of operation

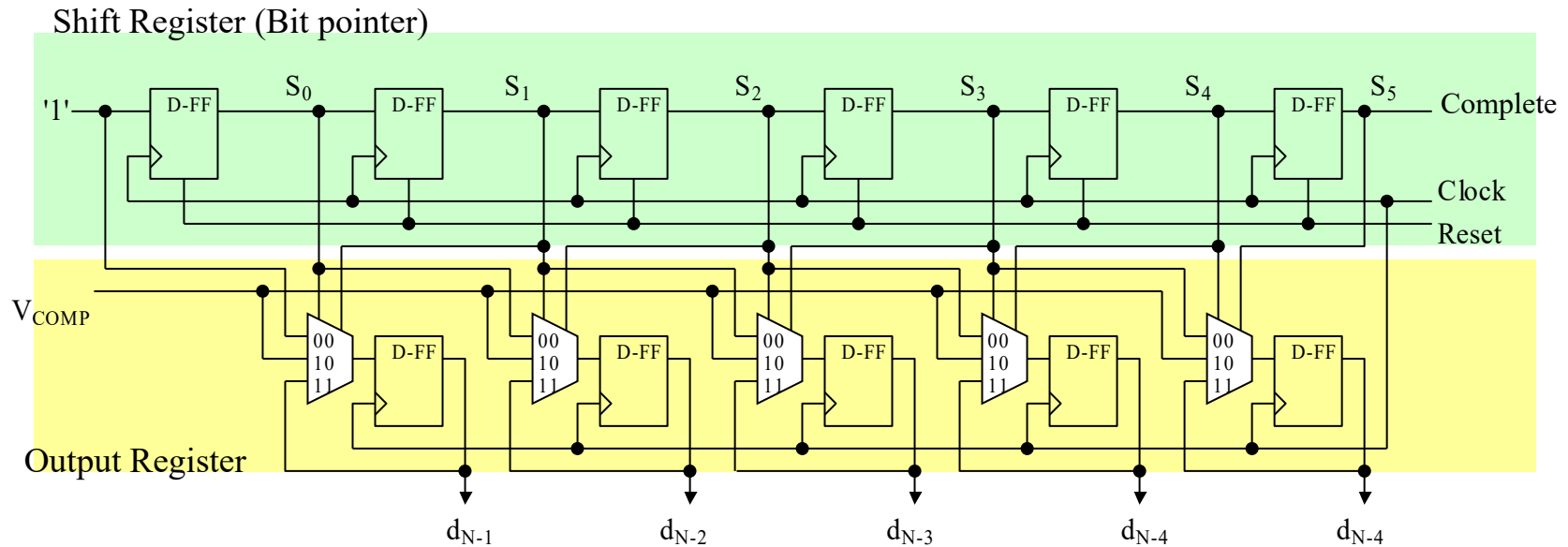


Block diagram of SAR-ADC



The SAR (Successive Approximation Register) controls holds the decided value and controls the output of DAC.

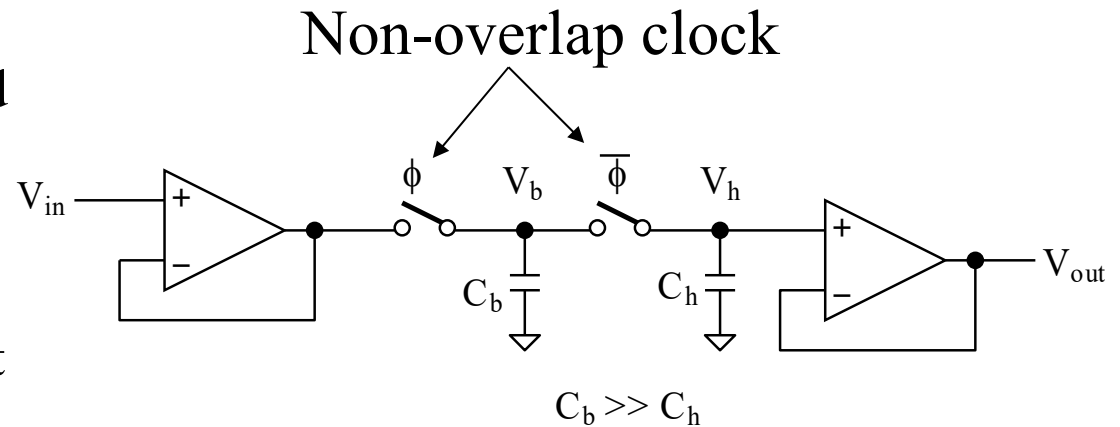
Circuit of SAR



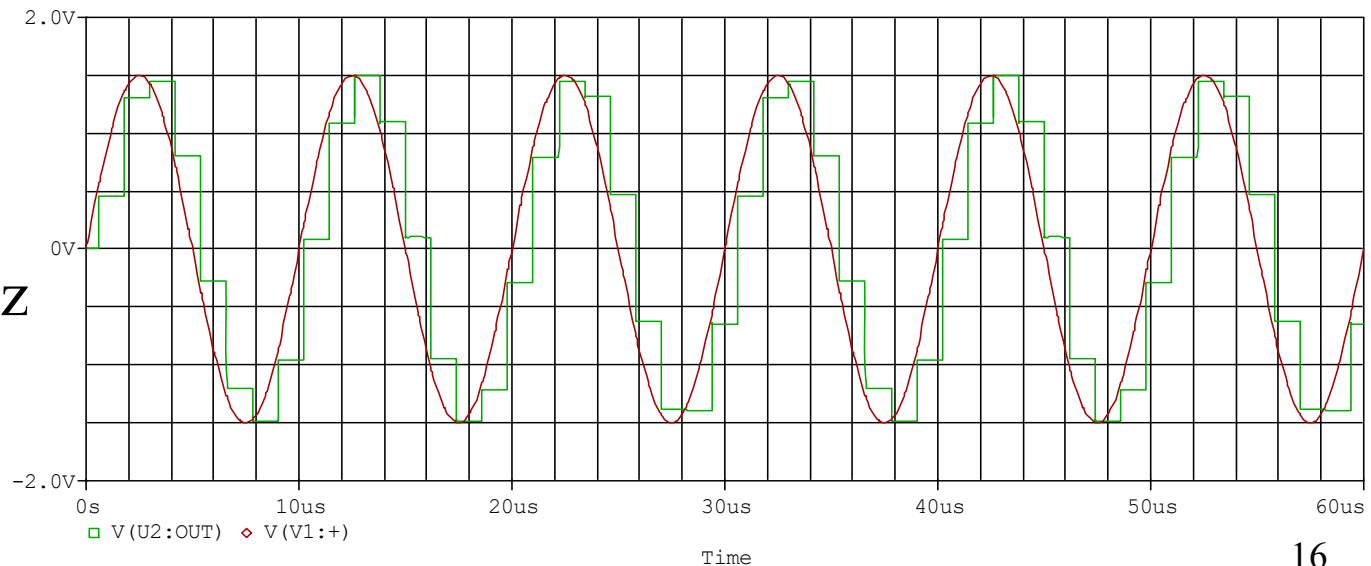
Reset	0	0	0	0	0
1	1	0	0	0	0
2	d_{N-1}	1	0	0	0
3	d_{N-1}	d_{N-2}	1	0	0
4	d_{N-1}	d_{N-2}	d_{N-3}	1	0
5	d_{N-1}	d_{N-2}	d_{N-3}	d_{N-4}	1
6	d_{N-1}	d_{N-2}	d_{N-3}	d_{N-4}	d_{N-5}

Sample and Hold circuit (S/H)

- The input voltage of SAR-ADC have to hold for the conversion to prevent the conversion error.
- SAR-DAC requires an S/H circuit for the input stage.



Simulation
 $f_{in} = 100\text{kHz}$
 $C_b = 10\text{pF}$
 $C_h = 100\text{fF}$

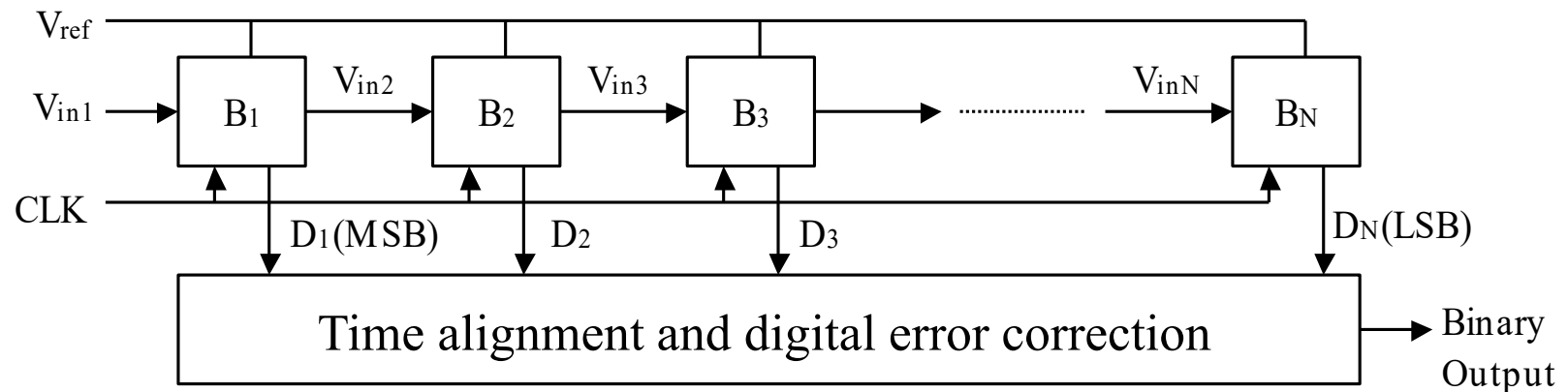


4.5 Pipeline ADC

(High precision and high speed)

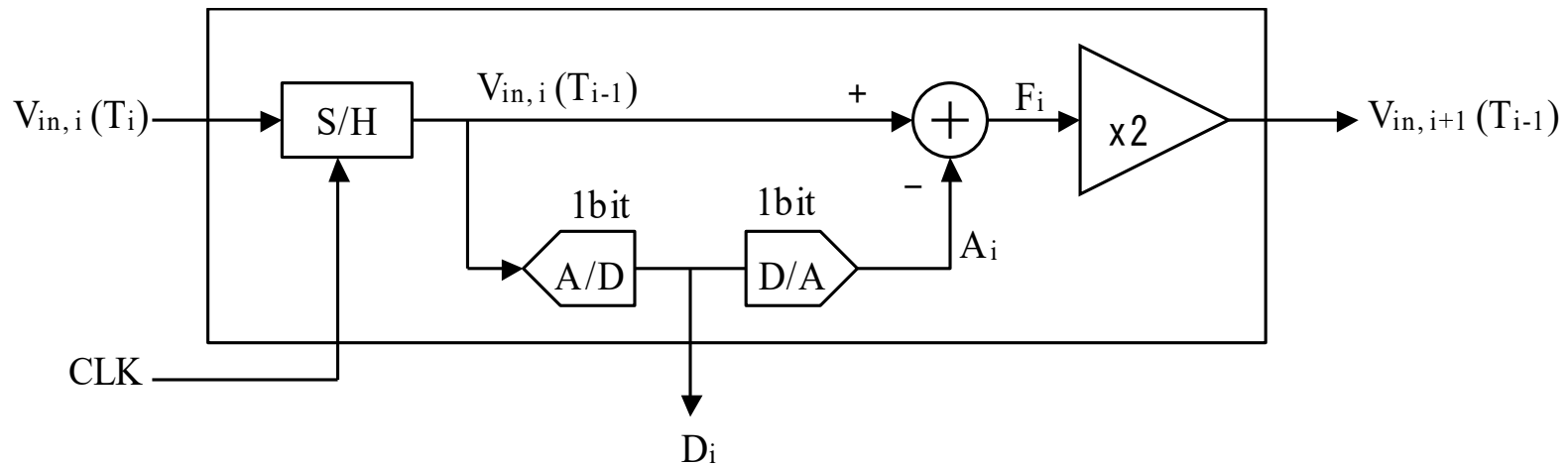
Block diagram of pipeline ADC

Instead of cycling the analog output of the 1-bit/stage section back to the input, the error output of the stage is fed into the subsequent stage, that is, this ADC is an open loop architecture.



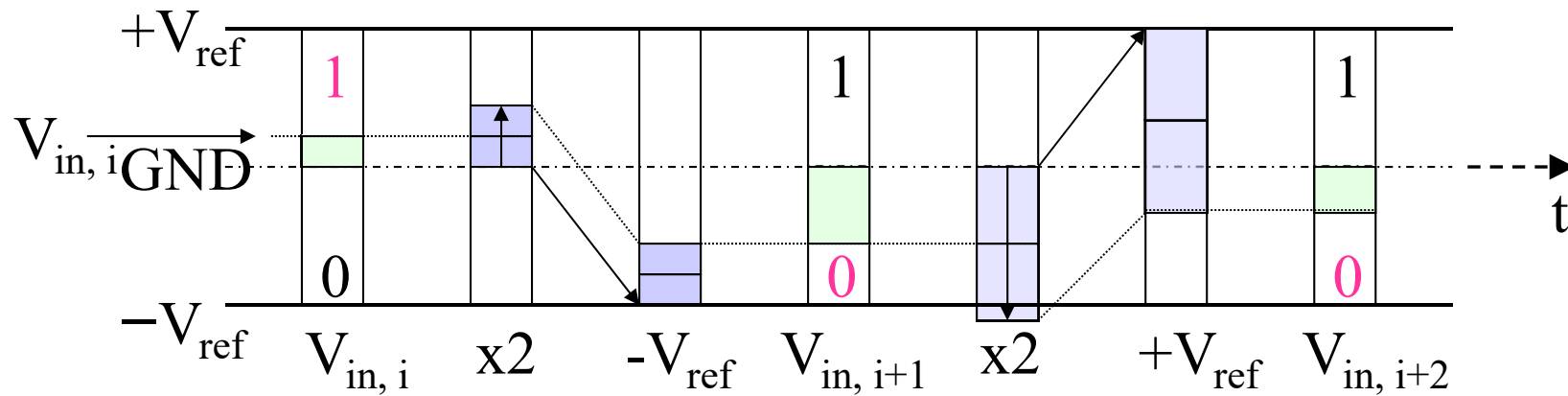
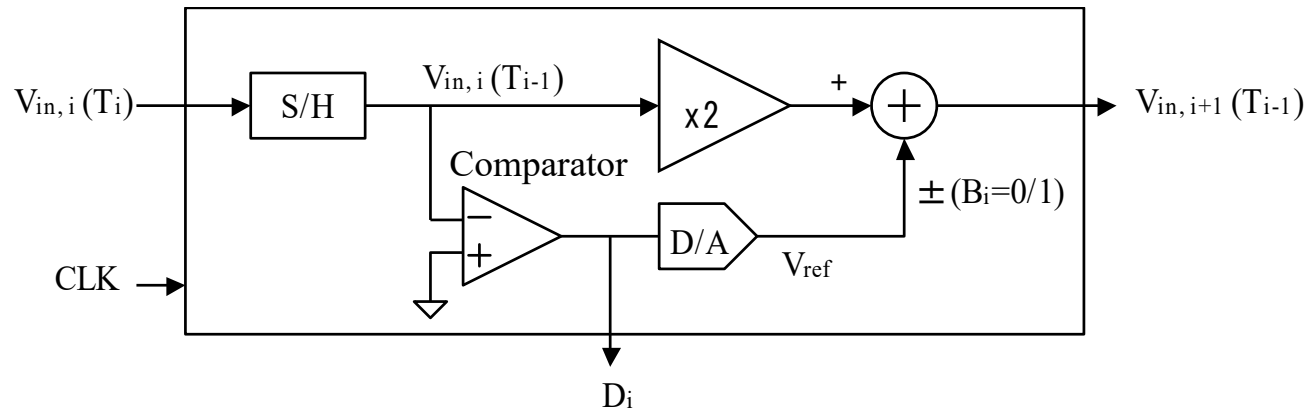
Each stage of $B_{1,2, \dots, N}$ has the digital output and the analog output of the quantization error. Each bit is determined for one clock cycle and N -bit conversion requires the N -clock cycles. The throughput of the conversion is 1-word per clock cycle through the pipeline processing.

Basic operation in 1-bit/stage section

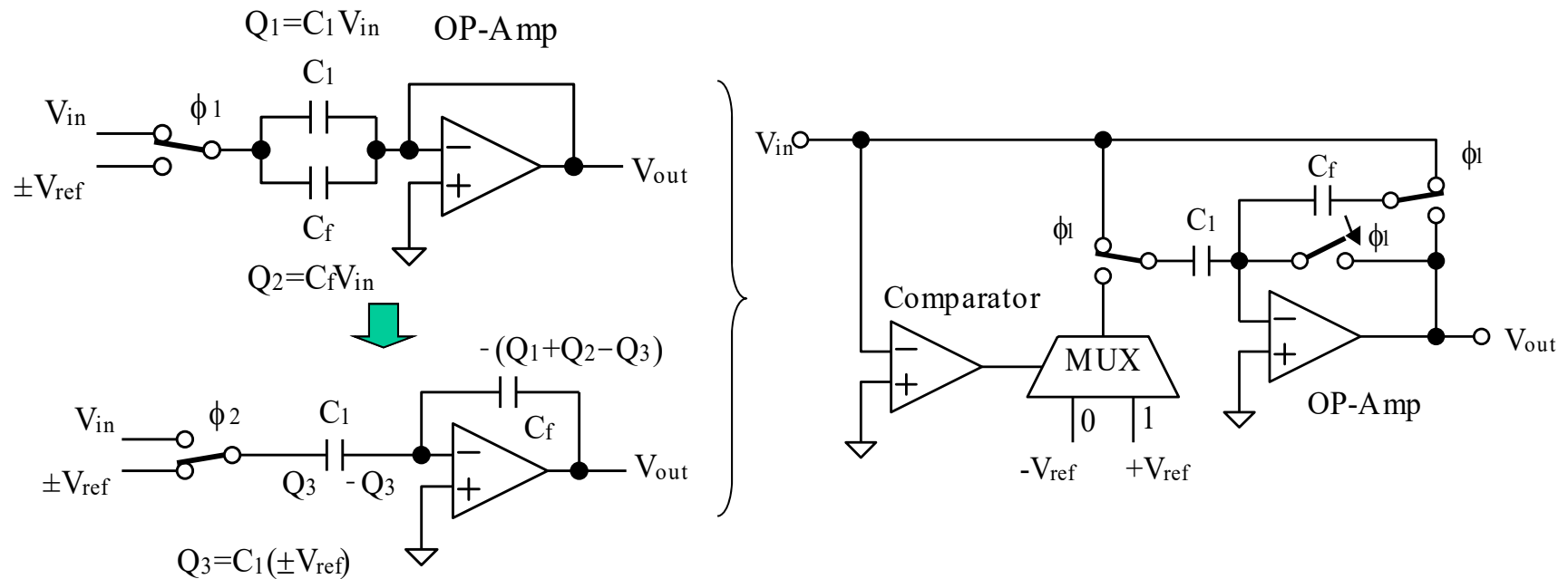


1. Sampling and holding analog signal $V_{in,i}$ with S/H circuit
2. Converting the analog signal into the 1 bit digital output D_i
3. Converting D_i into analog value A_i
4. Calculating the residual analog value $F_i = V_{in,i} - A_i$
5. Scaling the residual analog value F_i and sending it to the next stage

Practical implementation for double ended input



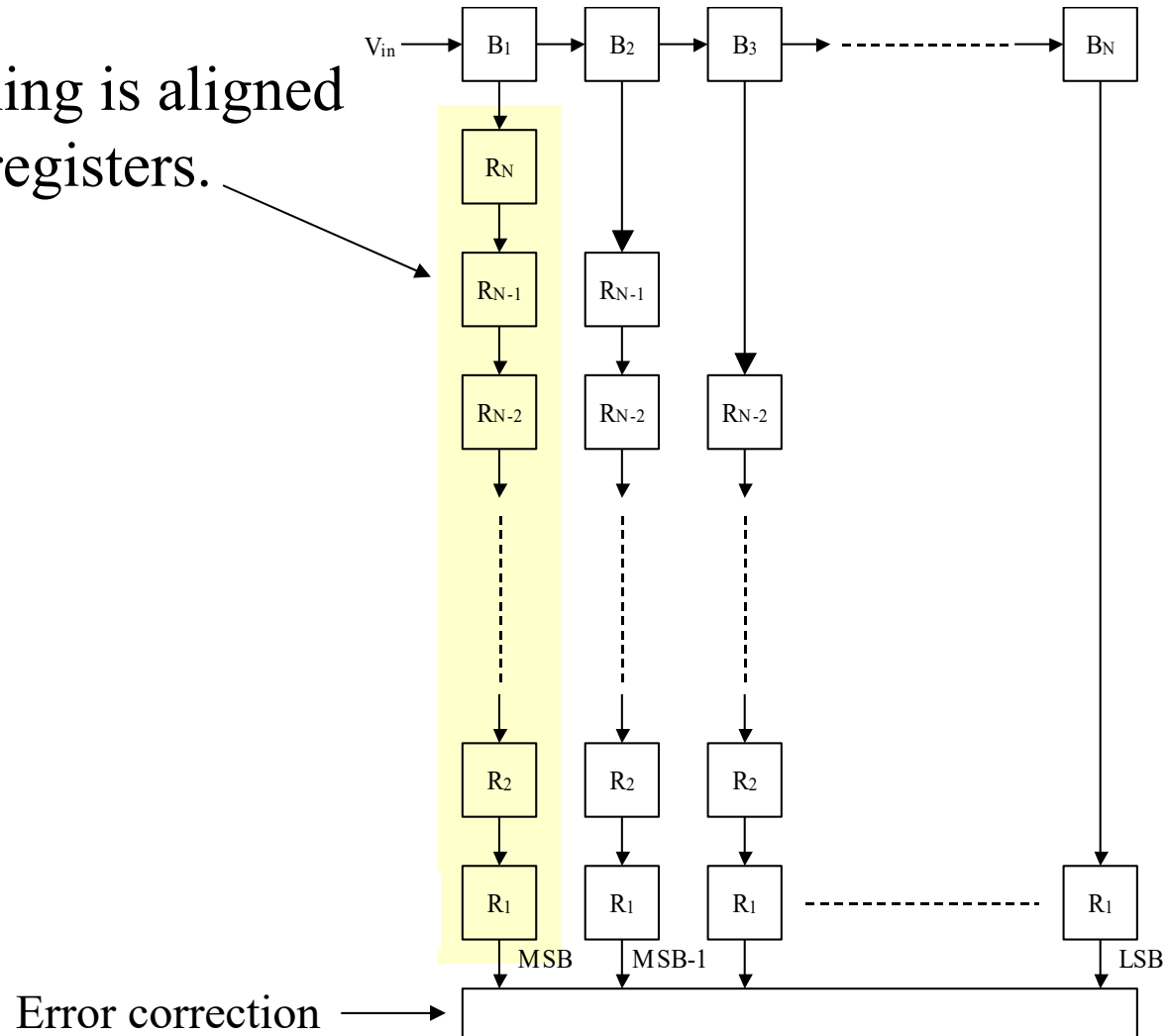
Design example of 1-bit/stage section



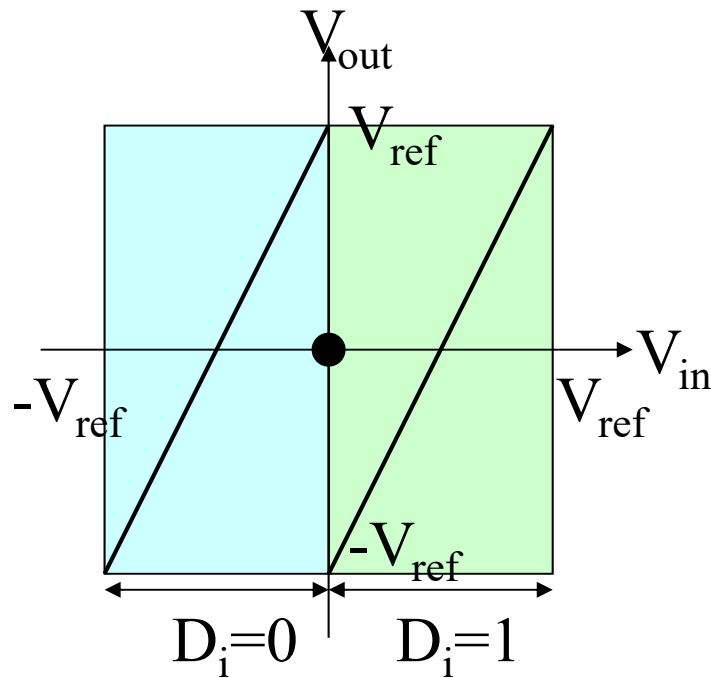
$$\begin{aligned}
 V_{out} &= \frac{1}{C_f} (Q_1 + Q_2 - Q_3) = \frac{1}{C_f} \{ (C_1 + C_f) \cdot V_{in} - C_1 (\pm V_{ref}) \} = \frac{C_1 + C_f}{C_f} V_{in} \mp \frac{C_1}{C_f} V_{ref} \\
 &= 2V_{in} \mp V_{ref} \quad (\text{if } C_1 = C_f)
 \end{aligned}$$

Time alignment

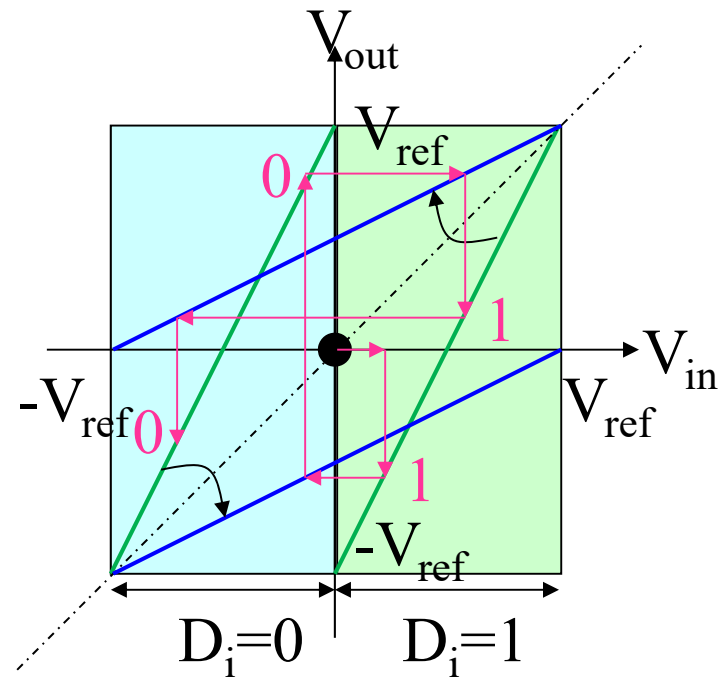
The output timing is aligned with the shift-registers.



Transfer characteristic of 1-stage



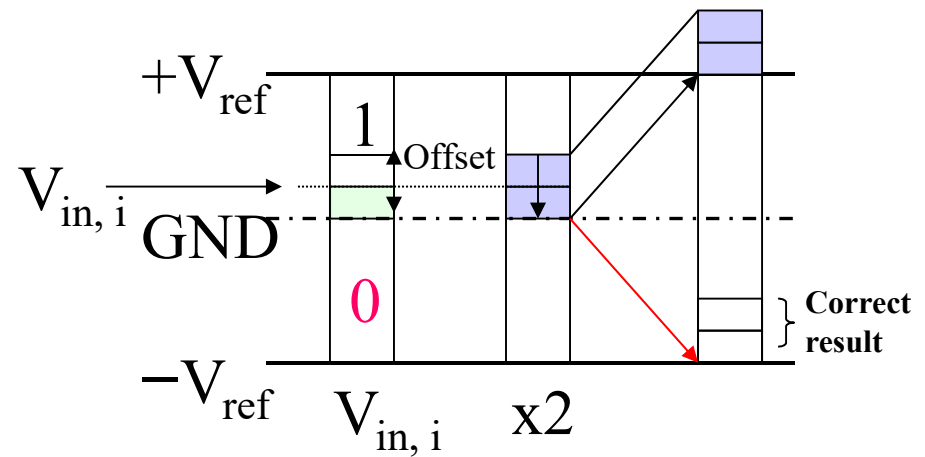
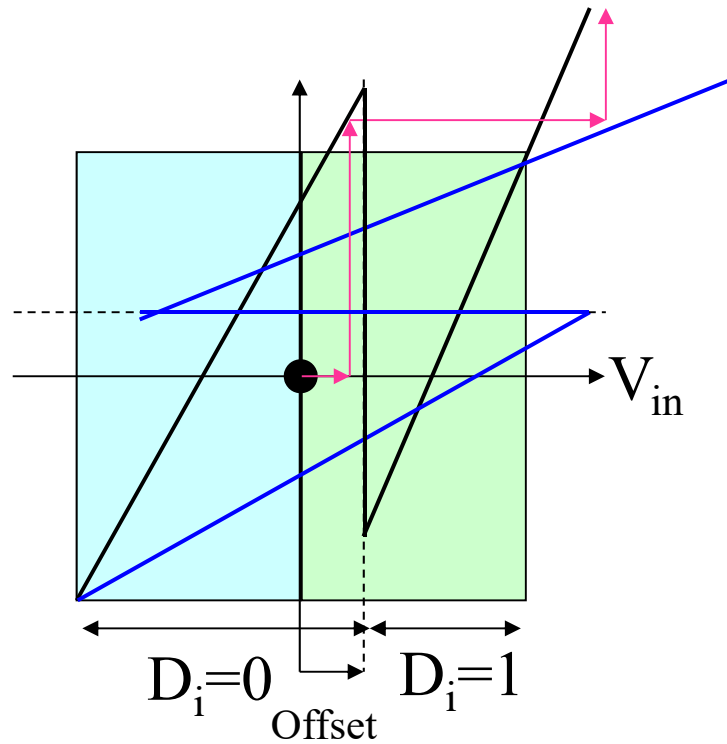
Transfer curve



Transfer curve of B_n (Green)
and B_{n+1} (Blue)

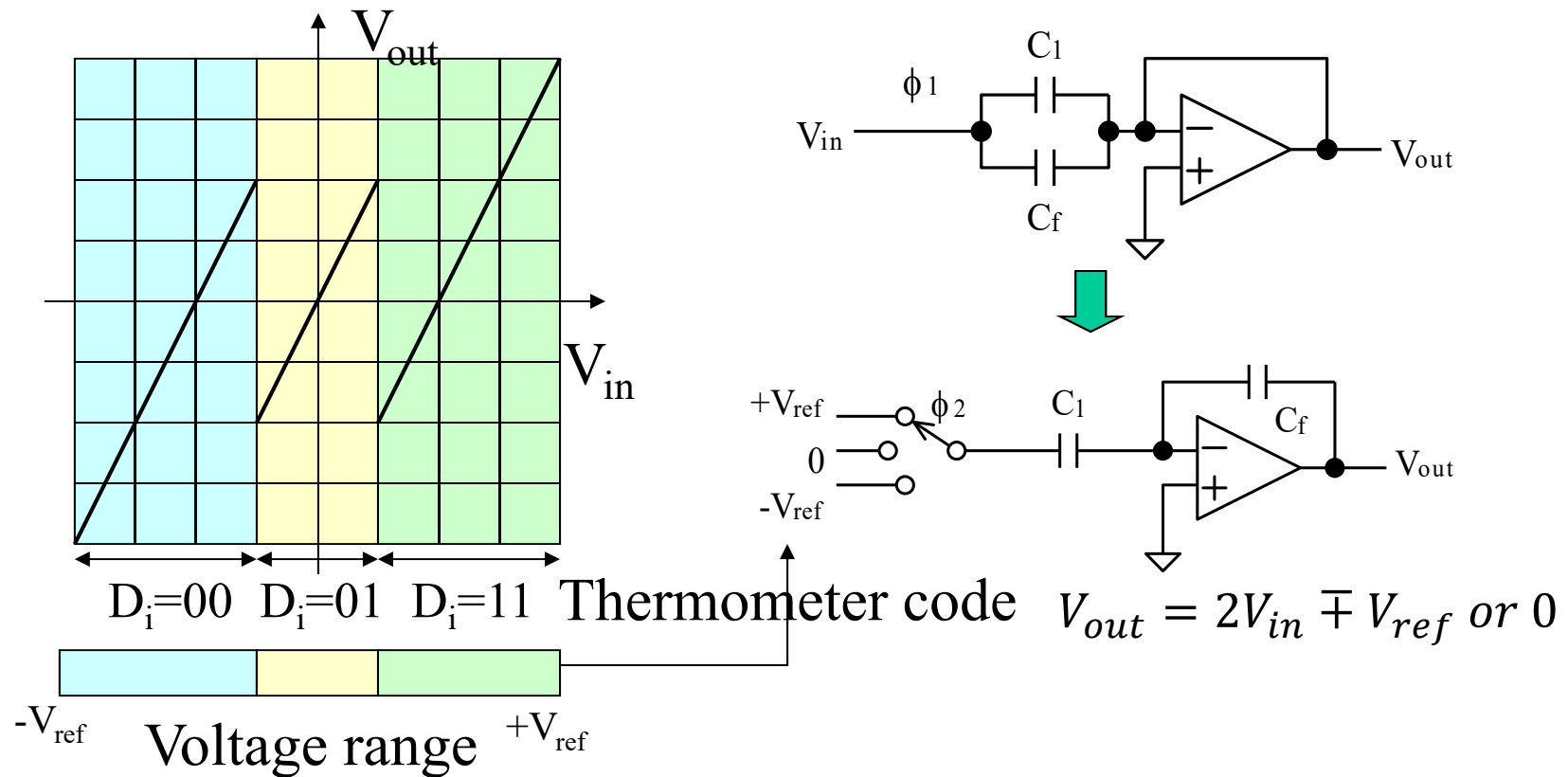
Error propagation

Transfer characteristic considering the comparator offset

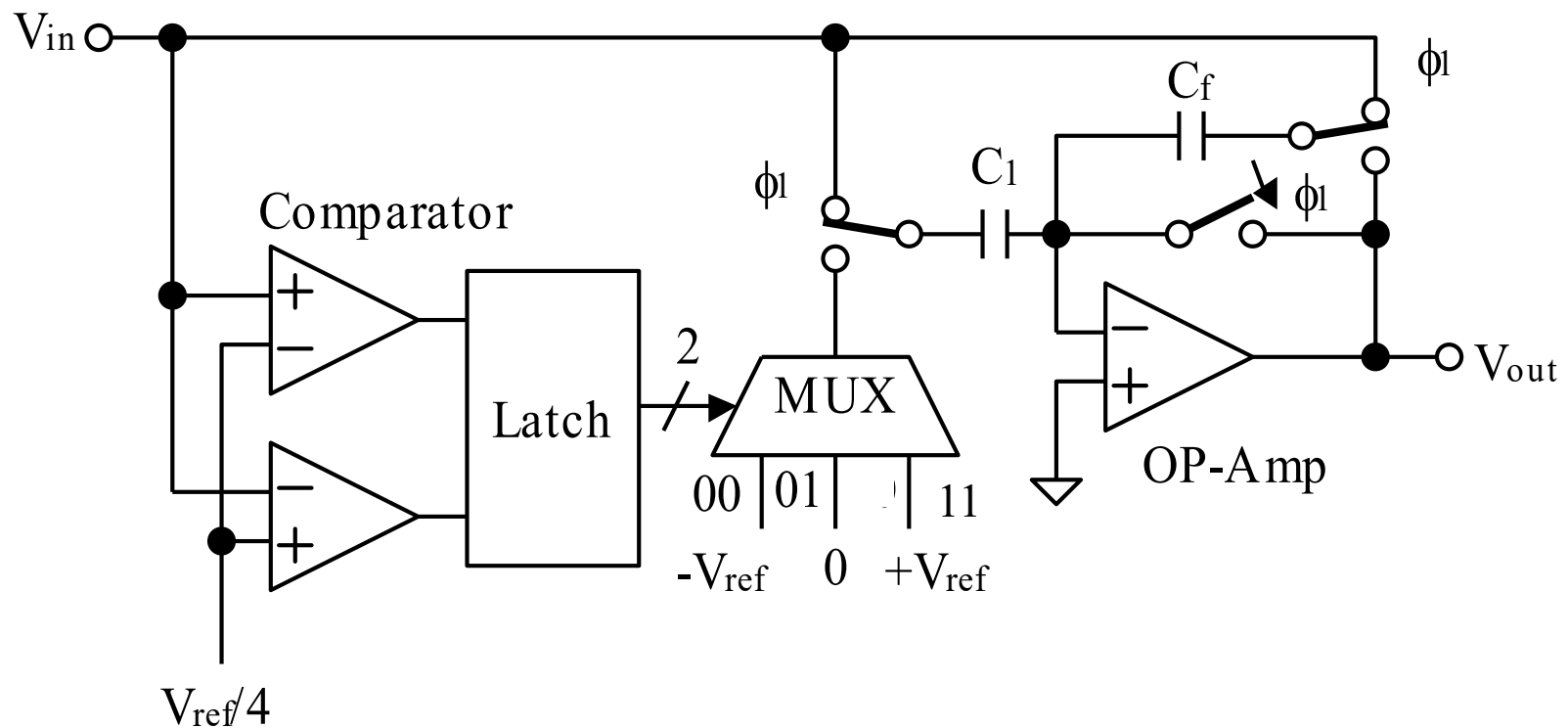


The comparator offset disturbs the convergence of the conversion result.

Transfer characteristic of 1.5 bit/stage

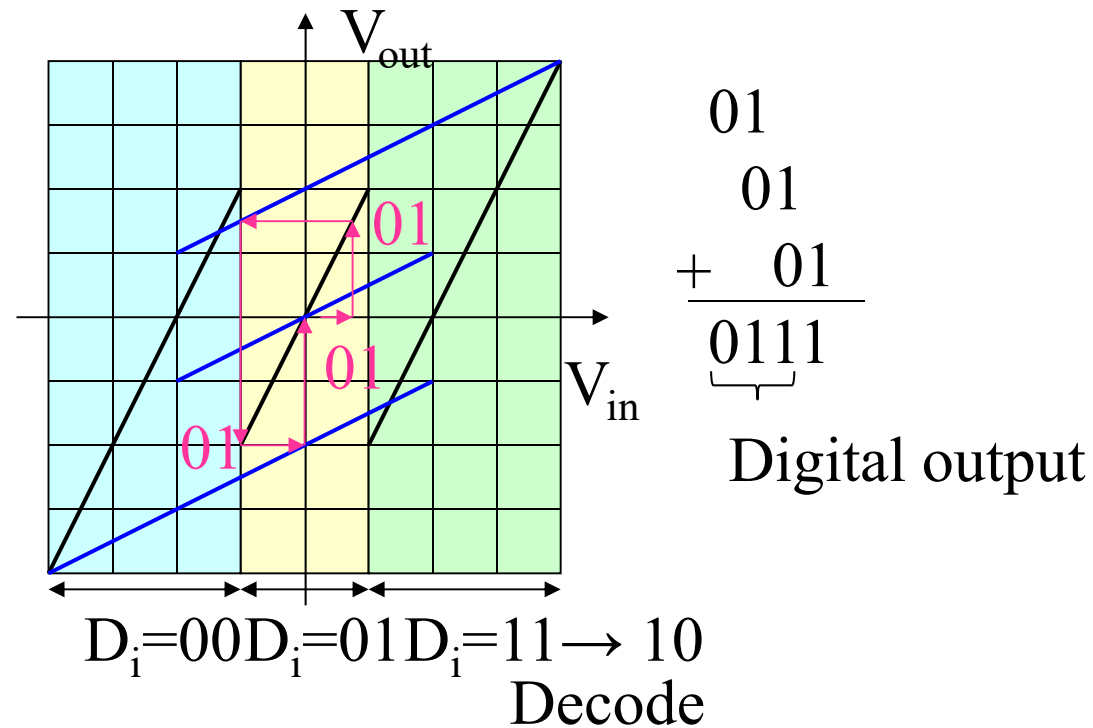


Design example of 1.5-bit/stage



Error compensation by 1.5bit stage

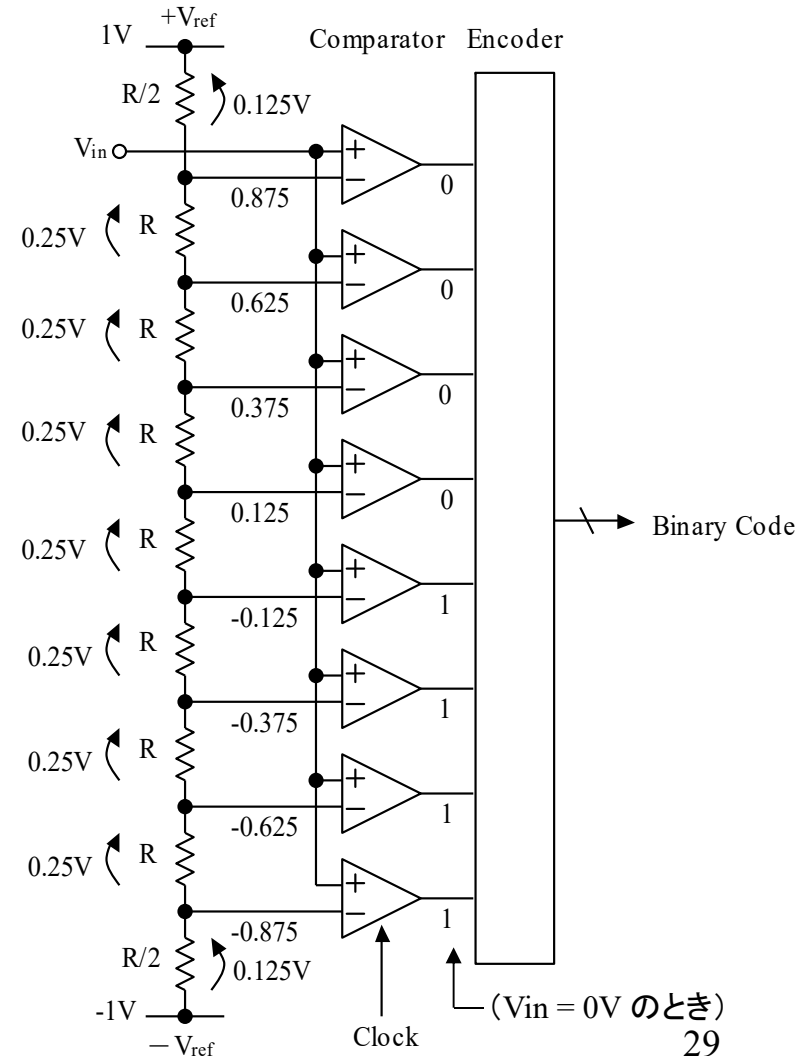
The comparator offset V_{off} temporarily makes the conversion error, however, the error is compensated by adding the conversion result of the previous stage, under the condition with $|V_{\text{off}}| < V_{\text{ref}}/4$.



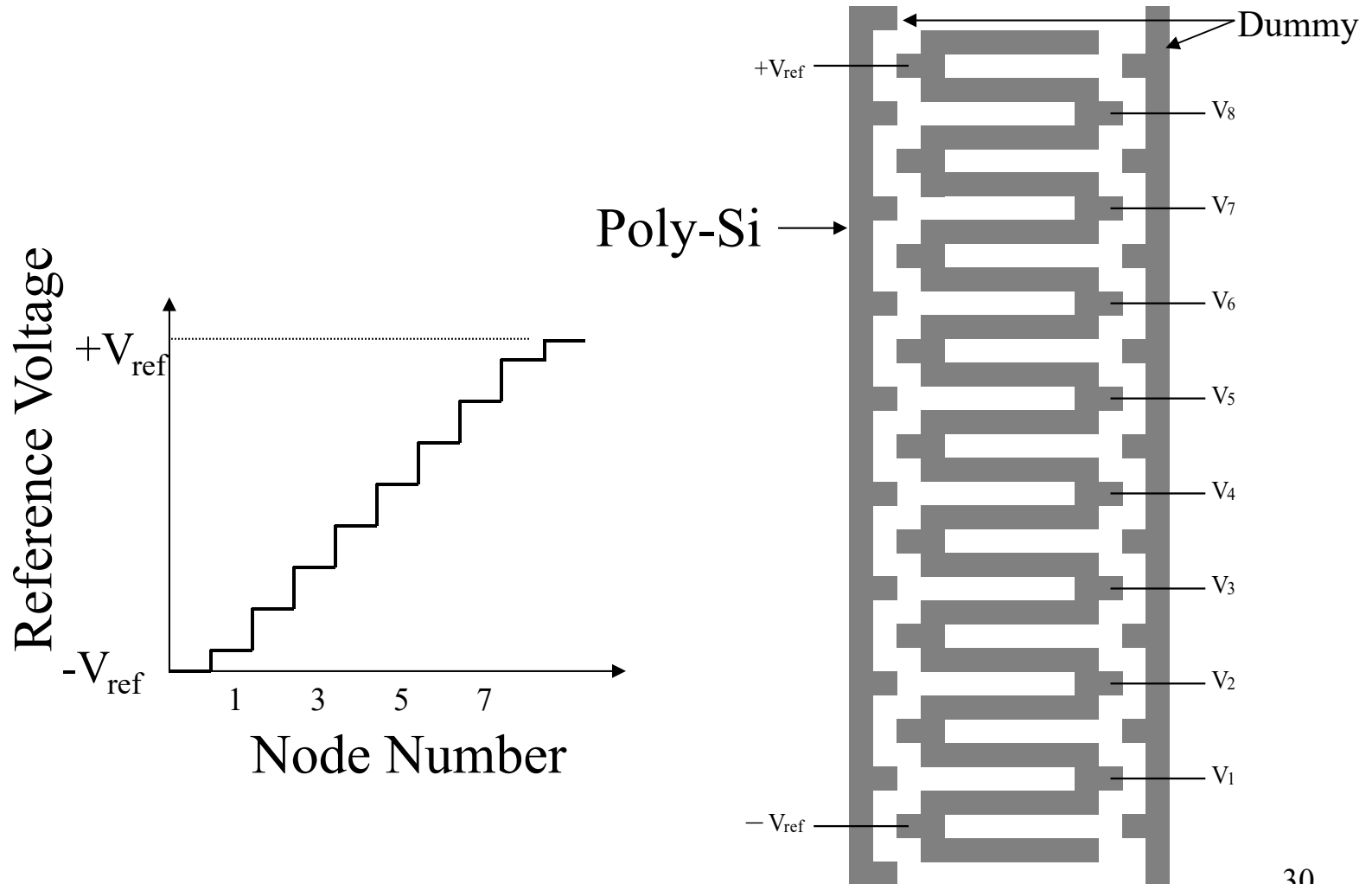
4.6 Flash and ADC (Very high speed and low latency)

Basic circuit

- The input voltage is compared with the 2^N voltages generated by dividing equally the reference voltage.
 - The result is output during one clock cycle.
 - The 2^N comparator is required for N-bit ADC.
 - The circuit scale and the power consumption are large.



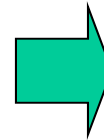
Reference voltage



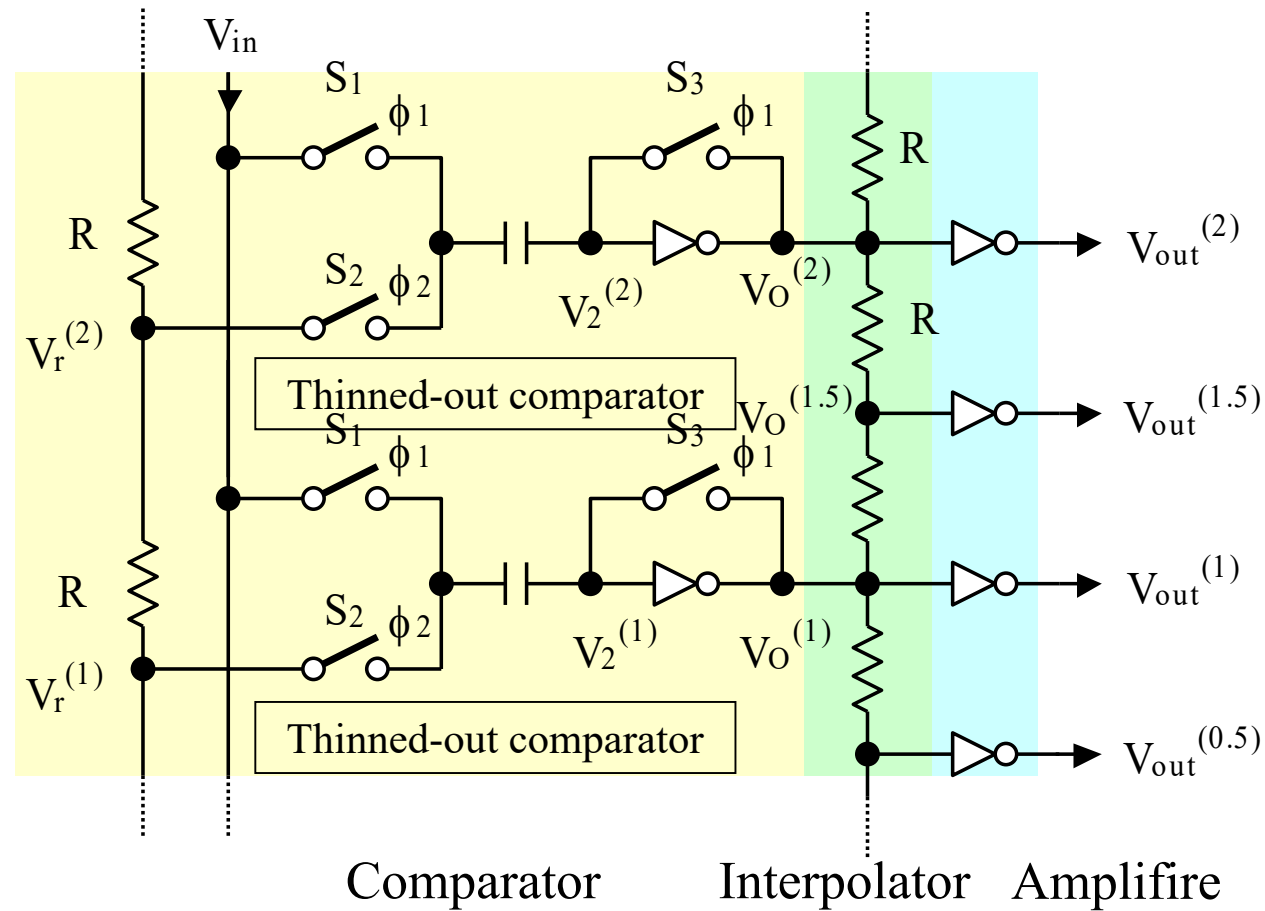
Thermometer encoder

V _{in} (V) (V _{ref} = 1V)	Thermometer Code (Comparator Output)	Binary Code (Encoder Output)
~ -0.875	0 0 0 0	0 0 0
-0.875 ~ -0.625	0 0 0 0	0 0 1
-0.625 ~ -0.375	0 0 0 0	0 1 0
-0.375 ~ -0.125	0 0 0 0	0 1 1
-0.125 ~ 0.125	0 0 0 0	1 0 0
0.125 ~ 0.375	0 0 0 1	1 0 1
0.375 ~ 0.625	0 0 1 1	1 1 0
0.625 ~ 0.875	0 1 1 1	1 1 1
0.875 ~	1 1 1 1	(1) 0 0 0

Encode



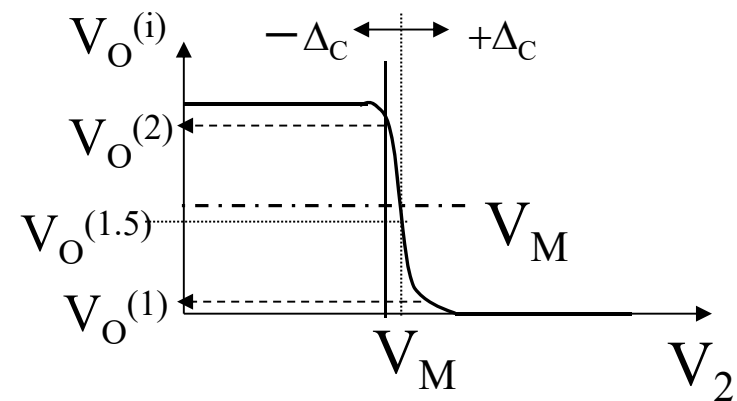
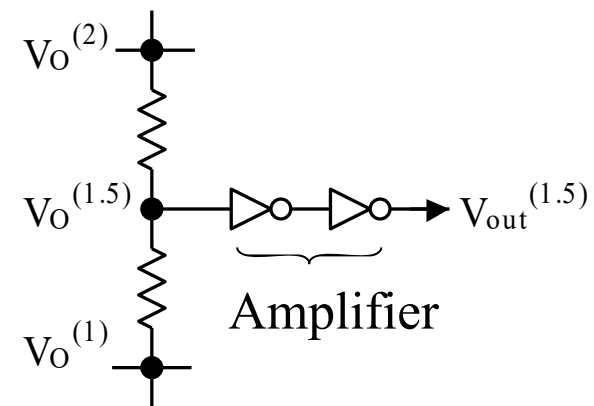
Reduction of the number of comparators



Interpolation methods of comparator

$V_O^{(1)}$	$V_O^{(2)}$	$V_{out}^{(1.5)}$
H	H	H
H	L	Error
L	H	Interpolation
L	L	L

When $V_r^{(2)} < V_{in} < V_r^{(1)}$, $V_O^{(1.5)} = (V_O^{(1)} + V_O^{(2)})/2$ is compared with the threshold voltage V_M of the subsequent inverter.

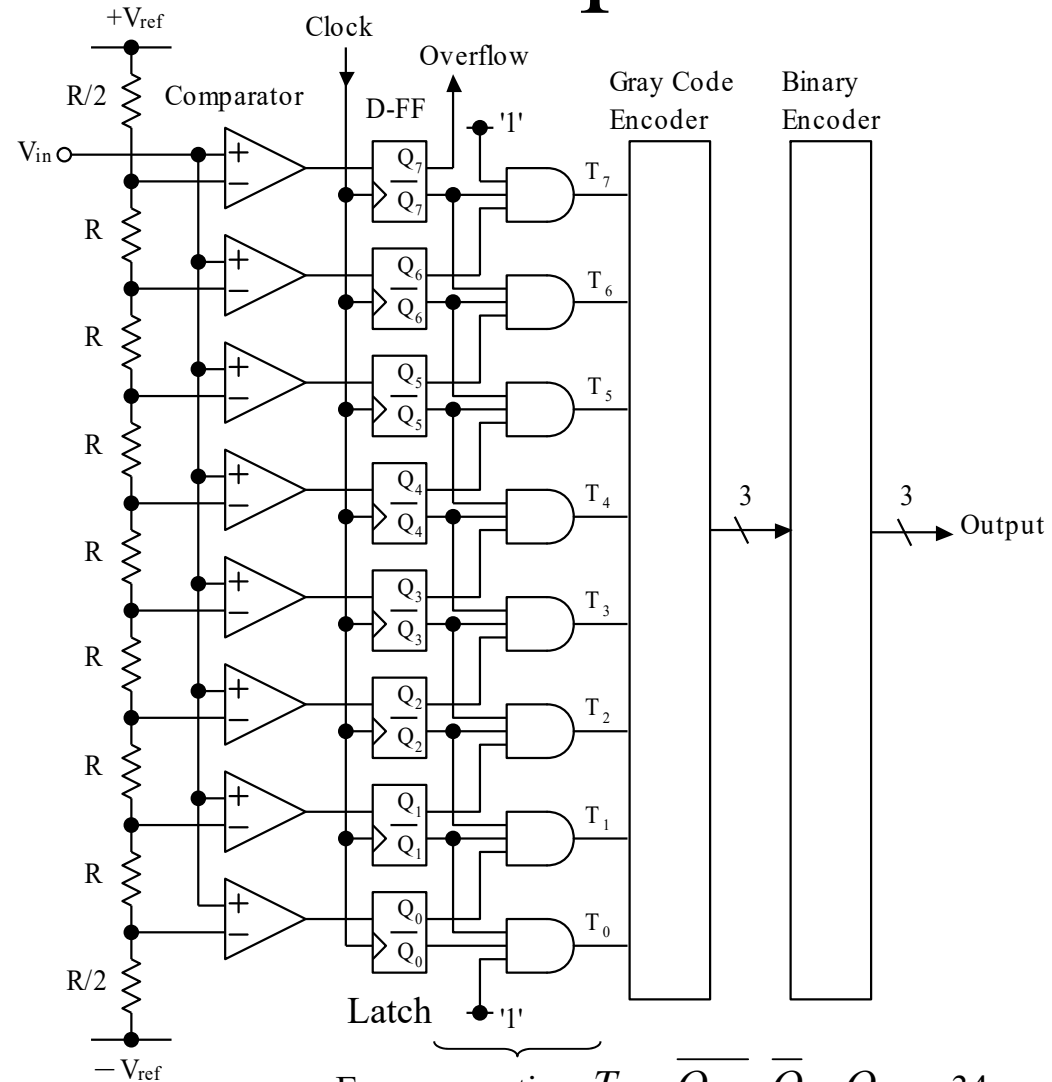


Error correction of comparator

The error correction circuit corrects the bit inversion in the thermometer code.

Gray code encoder converts the adjacent 1-bit error into the error of LSB.

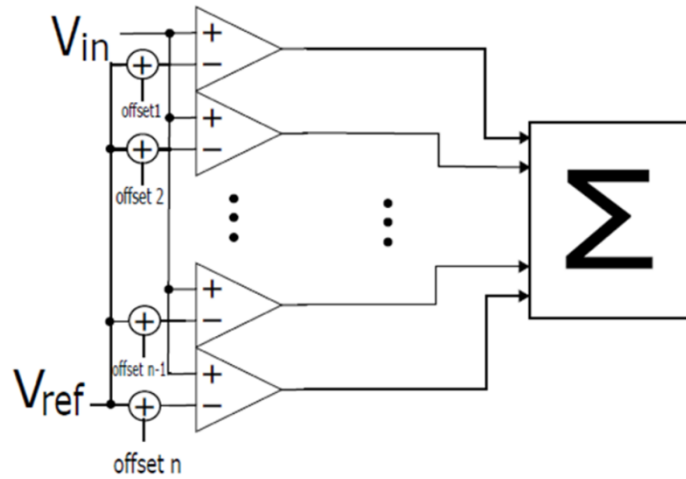
Q_{n+1}	Q_n	Q_{n-1}	T_n
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



Error correction $T_n = \overline{Q_{n+1}} \cdot \overline{Q_n} \cdot Q_{n-1}$ 34

4.7 Stochastic ADC (Very high precision)

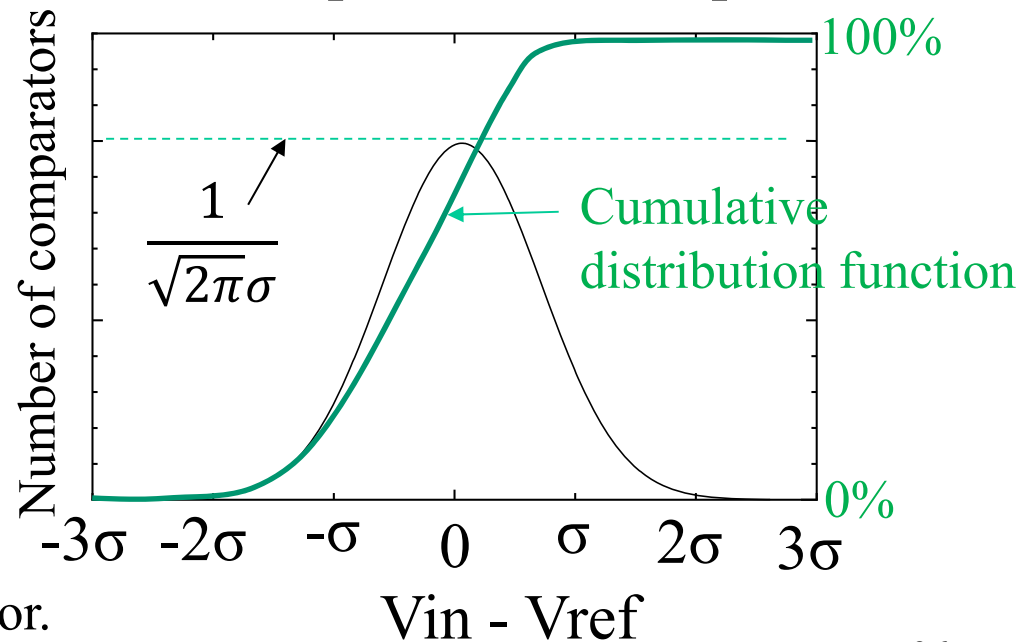
Principle of operation



$$N_{ENOB}(\text{bit}) = \log_4 \frac{N_{comparators}}{2}$$

Digital output

Statistical dispersion of comparators

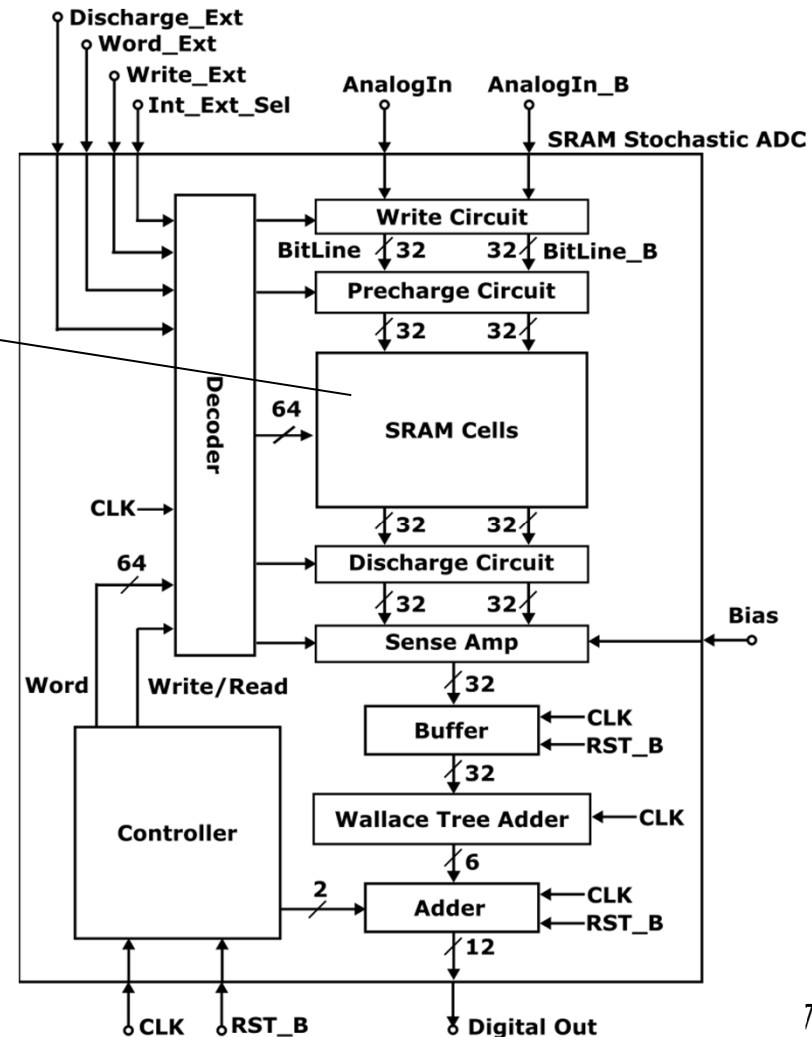
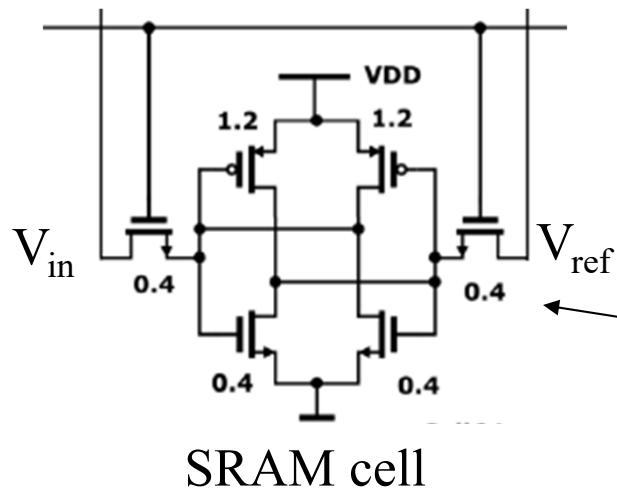


NOTE: The effective number of bits does not depend on the operational precision of the comparators, but it depends on the number of comparators.



A latch can be used as a comparator.

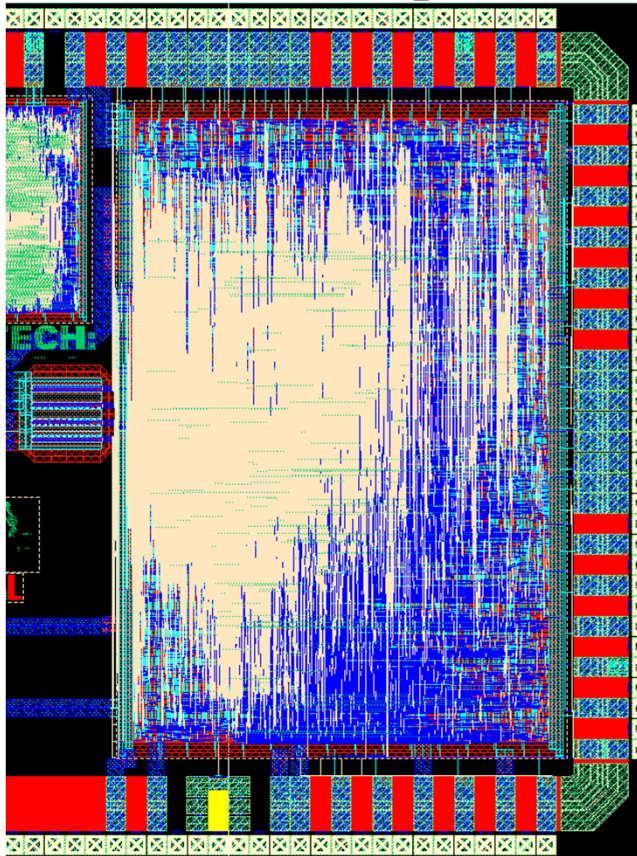
Block diagram of stochastic ADC



The design example of stochastic ADC. The SRAM array is used as 64 x 64 comparator array. The circuit is synthesizable, because it can be composed of digital circuit.

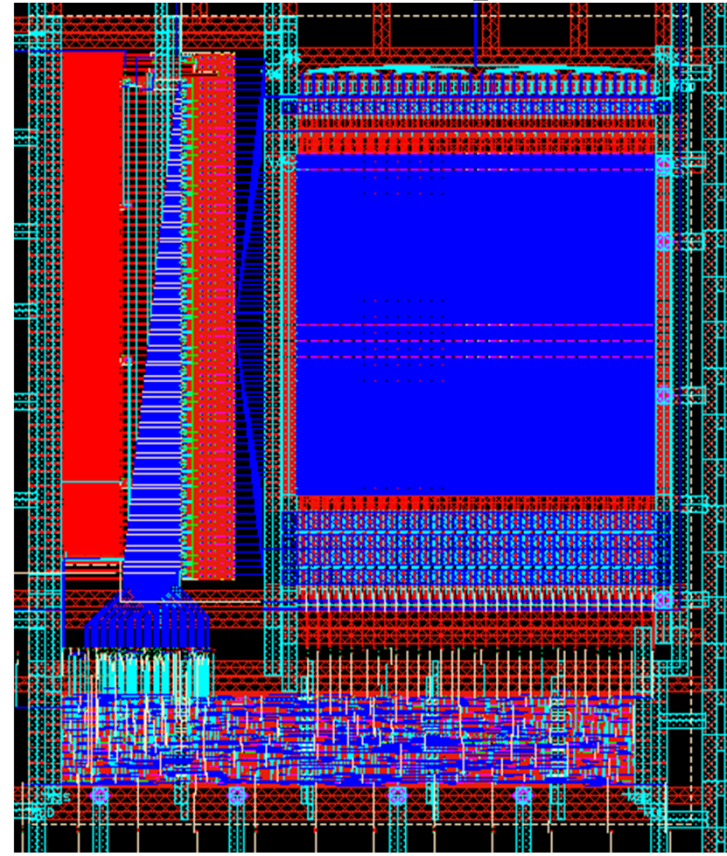
Design example of 2 step stochastic ADC

4-inverter-comparators



CMOS 65nm, 1930 um x 1315 um

6T-SRAM-comparators



CMOS 180nm, 525 um x 430 um