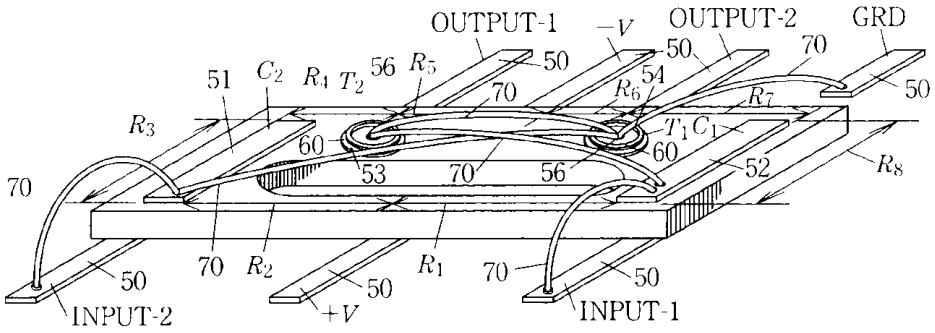
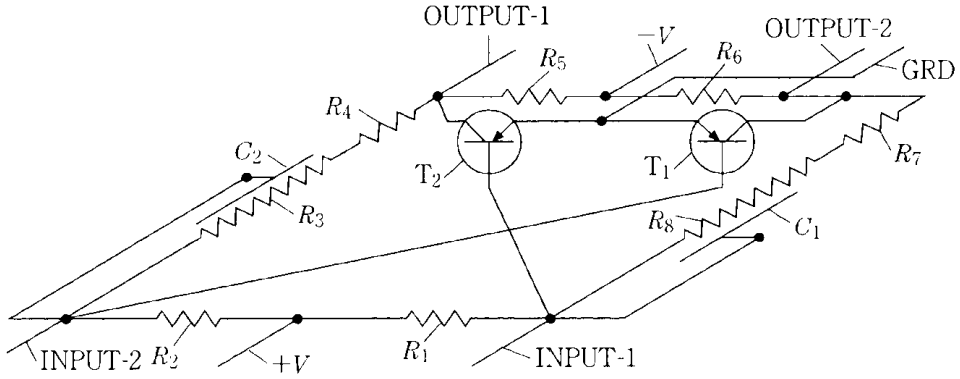
1.1 Technology trends

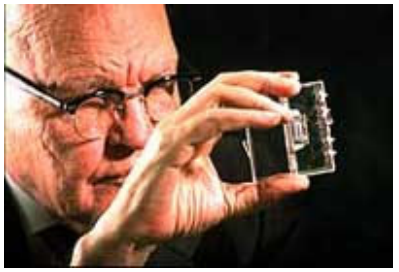
Historical background of microelectronics

1.1.1 Origin of LSI

Patent of J. Kilby (1959)



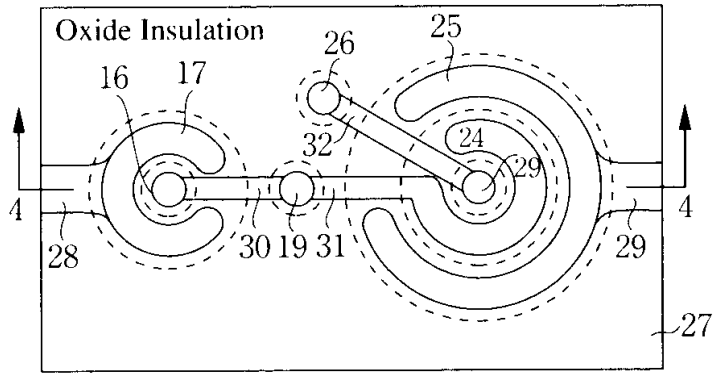


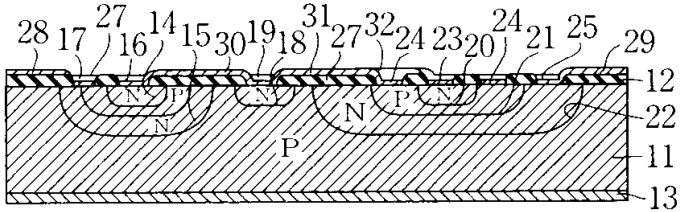


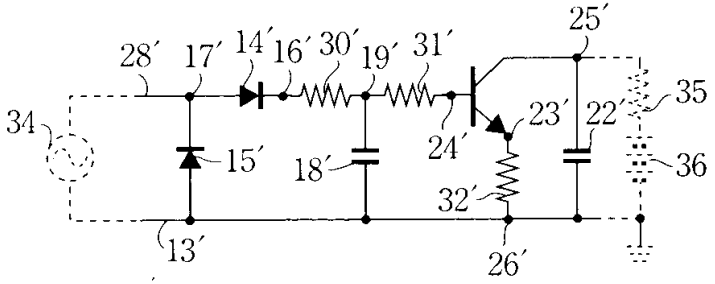
Jack S. Kilby,
Texas Instruments Inc.,
2000 Nobel Prize winner
Source: TI Inc.

US Patent
No. 2 138 743, 1964

Patent of R. Noyce (1959)







Robert Noyce,
Fairchild Semiconductor International, Inc.
Source: Innopedia

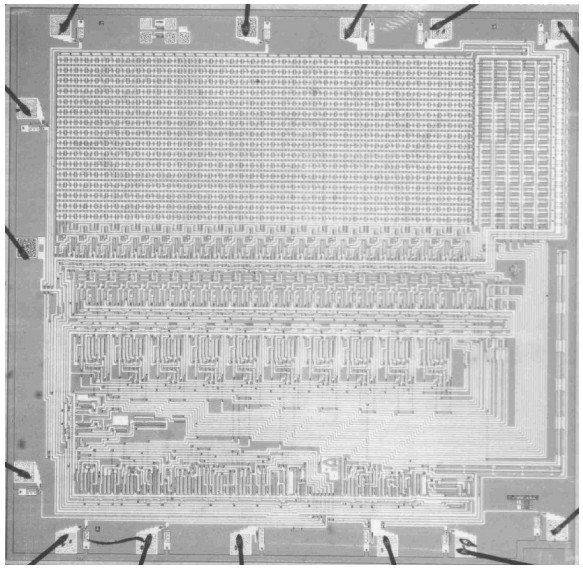
US Patent
No. 2 981 877, 1961

Technological innovations

Year	Innovation	Inventor
1959	Patent application of Solid State Circuit	TI, J. Kilby (Registration: 1964)
	Patent application of Unitary Circuit	Fairchild Semiconductor International, R. Noyce (Registration: 1961)
1961	IC (Integrated Circuit) made in Japan	Mitsubishi Electric Corporation (Renesas Electronics Corporation)
1962	Start of mass production of logic family	Fairchild, TI
1965	IC calculator	Sharp Corporation
	Moore's Law	Gordon Moore (Intel Corporation)
1970	Chipset of MP944	Garrett AiResearch Corp., American Microsystems, Inc. (Official announcement 1998)
1971	Microprocessor 4004	嶋正利(Busicom corp.), Marcian Edward Hoff Jr., Federico Faggin (Intel Corp.)
1974	Microprocessor TMS1000 （US Pat.：3,757,306, 4074351, 1973）	TI, Gary Boone and Michael Cochran (Microcontroller with RAM and IO)

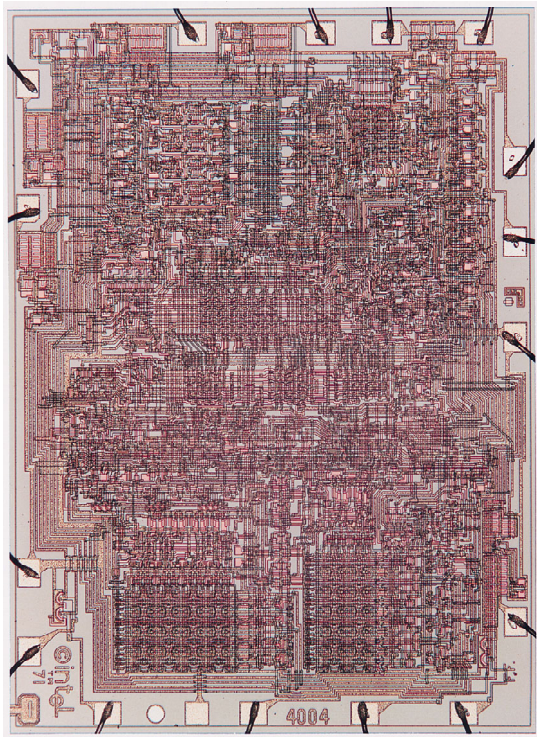
The world's first microprocessor

Garrett AiResearch MP944
p-MOS technology,
Data 20bit, f_{CLK} = 375kHz



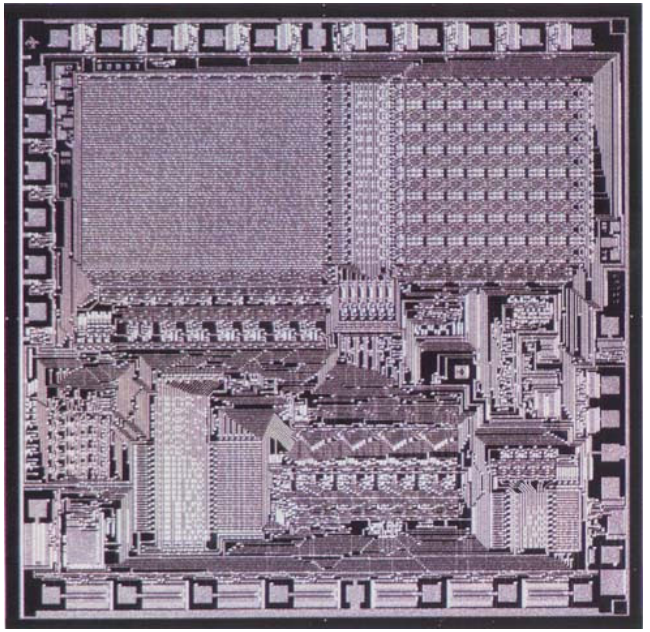
Source: http://firstmicroprocessor.com/

Intel 4004
10um p-MOS technology,
2,250 transistors,
f_{CLK} = 500k-740kHz
Data 4bit, 48 instructions,



Source: http://www.4004.com/

TI TMS1000
8um p-MOS technology,
8,000 transistors,
f_{CLK} = 100k-400kHz
Data 4bit, 43 instructions,
256bit RAM, 1kbit ROM



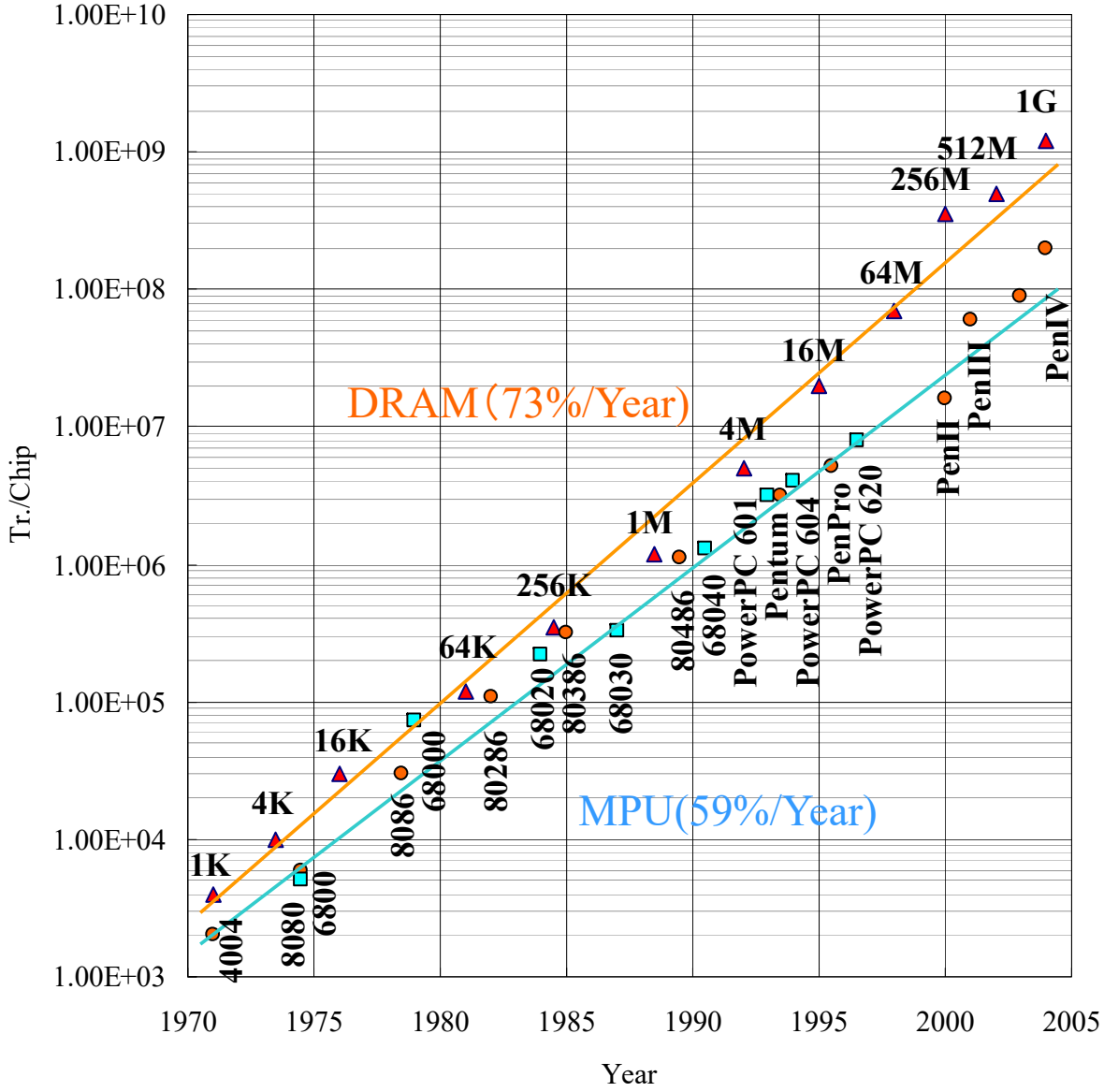
Source: National Museum of American History

1.1.2 Trends of process technology

Index of integration

- Logic LSI
  - Number of transistors per chip
  - Number of gates per chip (based on 2-input NAND conversion)
- Memory
  - Number of bits (Not Byte)
- Mixed signal LSI (including analog circuits)
  - The performance does not depend on the integration, but the figure of merit is defined to compare the circuit performance.

Moore's low (1965)



Gordon Moore's Law

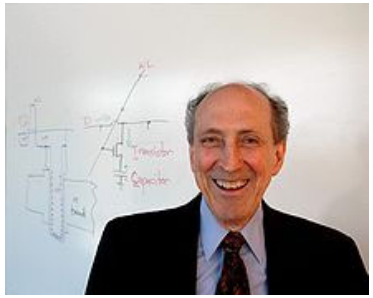
Annual growth rate
= 41% = 2times/2years

Gordon Moore

Source: Intel Corporation

Dennard's scaling law (1974)

- The reduction of the transistor size leads to both performance and integration.
- The length, width and height are scaled down as the same ratio k.



Robert H. Dennard,
1968, Inventor of DRAM
Source: Wikipedia

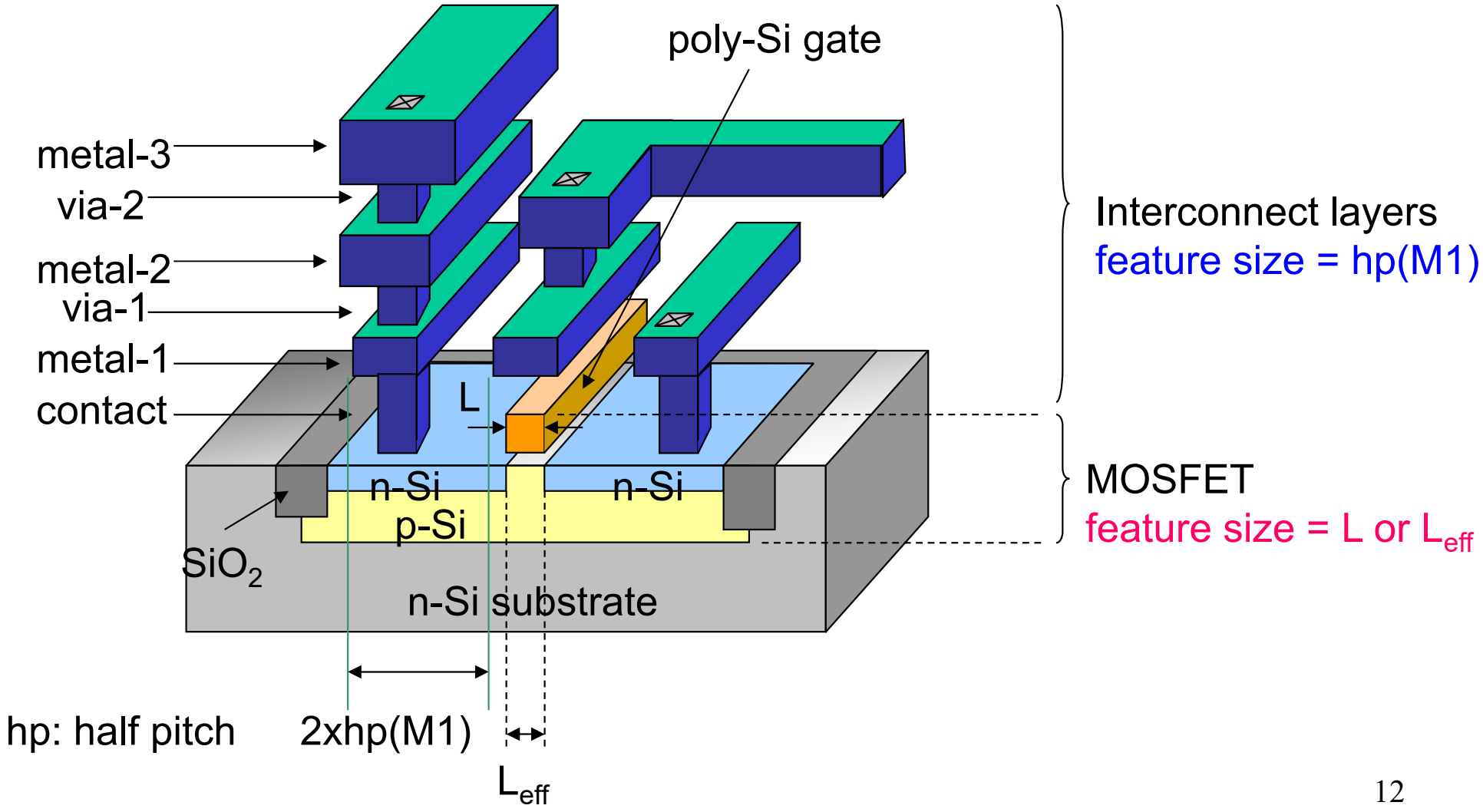
Effects of scaling (Theoretical estimation is discussed in Chapter 6.)

	Integration	**Speed**	**Power consumption /Transistor**	**Power consumption /area**
Scaling factor k	$1/k^2$	$1/k$	k^2	1
k = 0.7	2	1.4	0.5	1

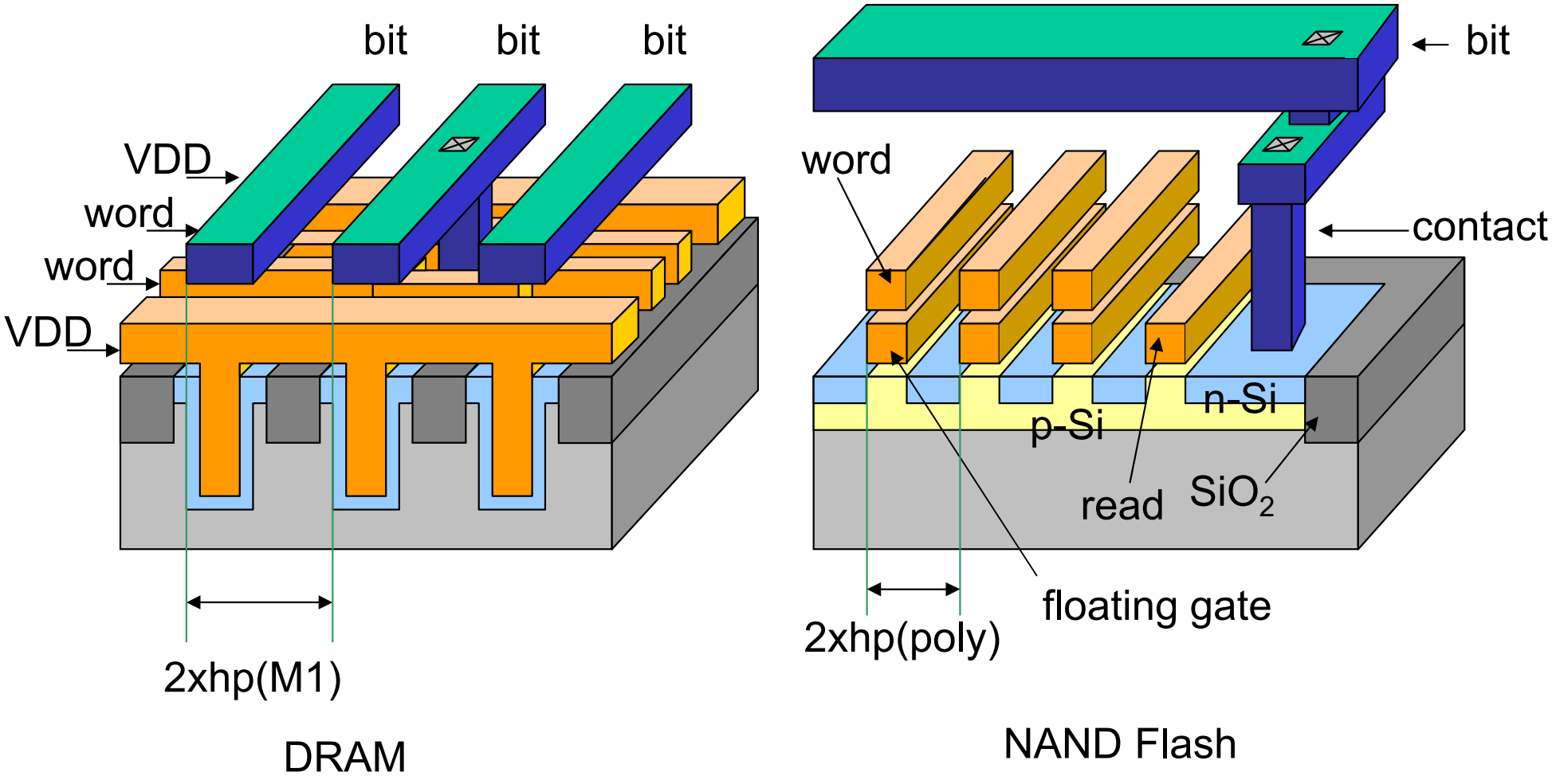
Driving force of microfabrication technology

- Dennard's scaling law is a basis of the development in the microfabrication technology.
- Industrial advantages of scaling
  1. Reduction of the manufacturing cost (material, energy, and transportation)
  2. Performance improvement of the LSI
  3. Reduction of the power consumption of LSI
- Contribution to Sustainable Development Goals (SDGs)
  1. Compatibility between the performance and manufacturing cost.
  2. The semiconductor industry is typical knowledge-intensive industries and have not declined for over 70 years.

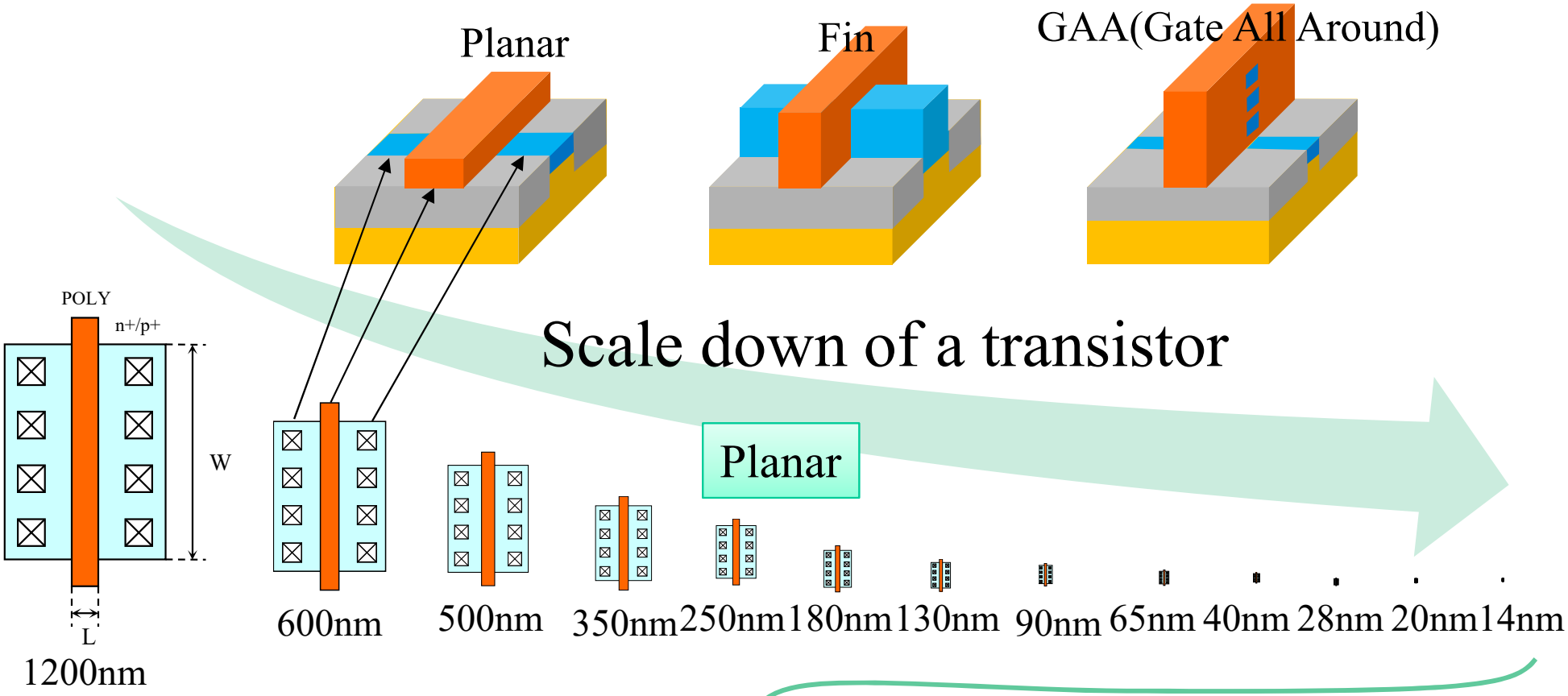
Structure of MOSFET (Transistor)



Structure of DRAM and Flash memory

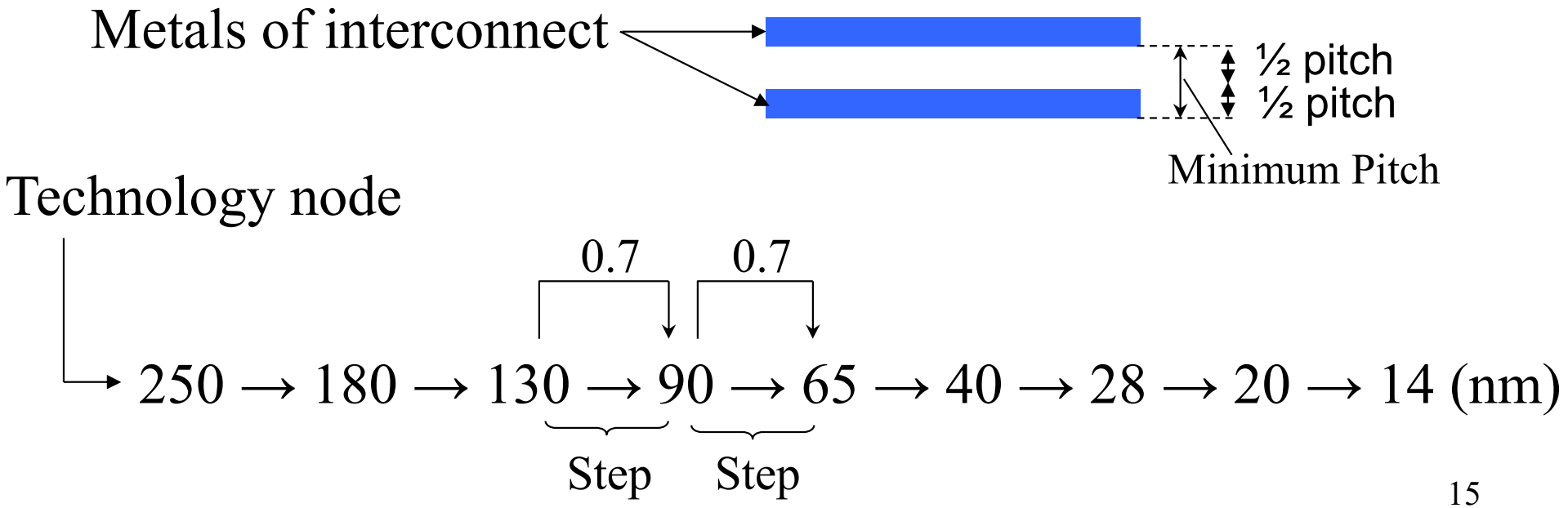


Scaling of MOSFET (Transistor)



Technology node

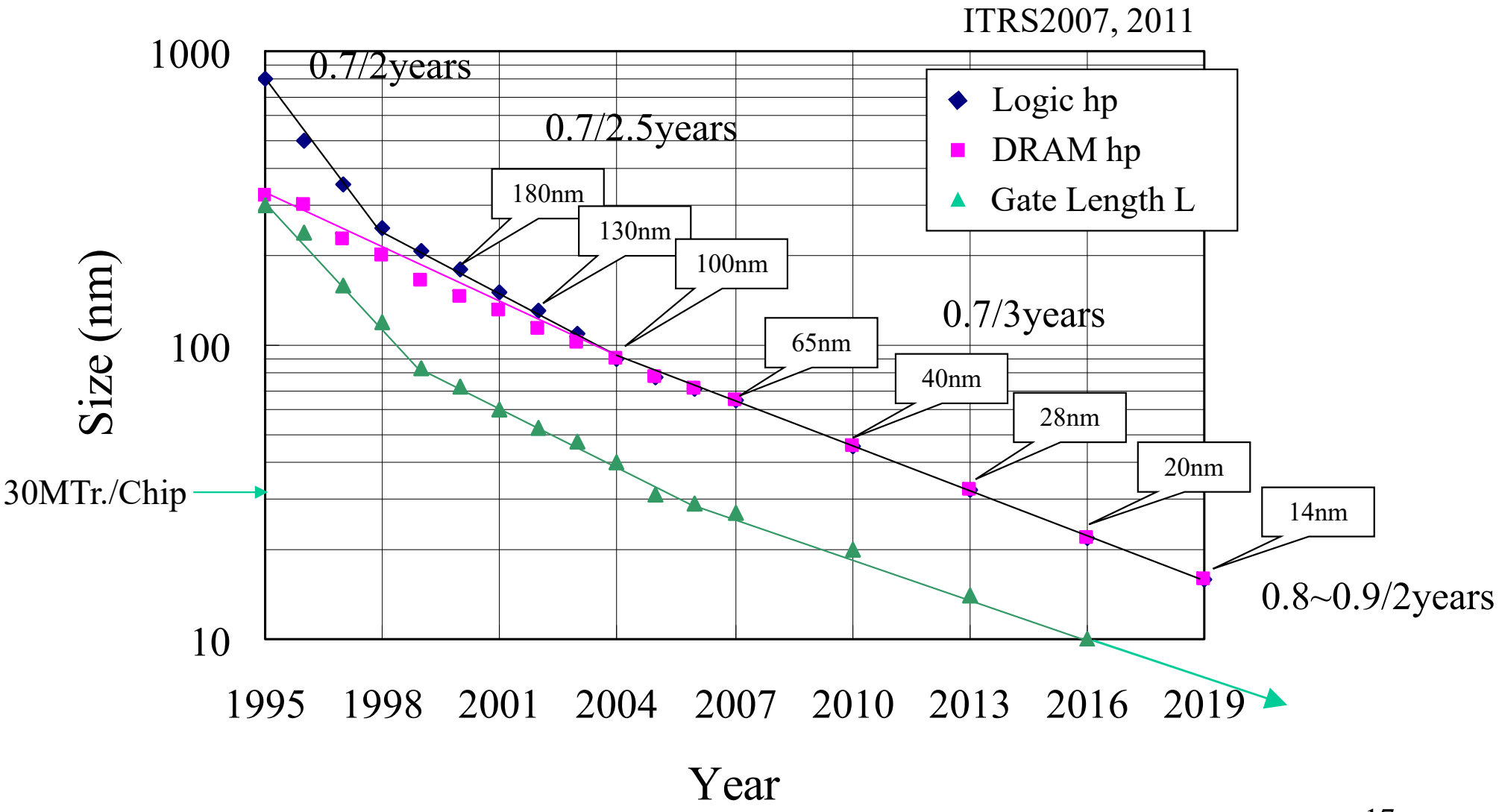
- Feature size or technology node was represented by 1/2 pitch (hp) between interconnects. However, the physical scale of the hp and the gate length diverges from the technology node In recent years.
- The technology cycle (rate of the advancing) has been progressing at 1-step per about 3years.



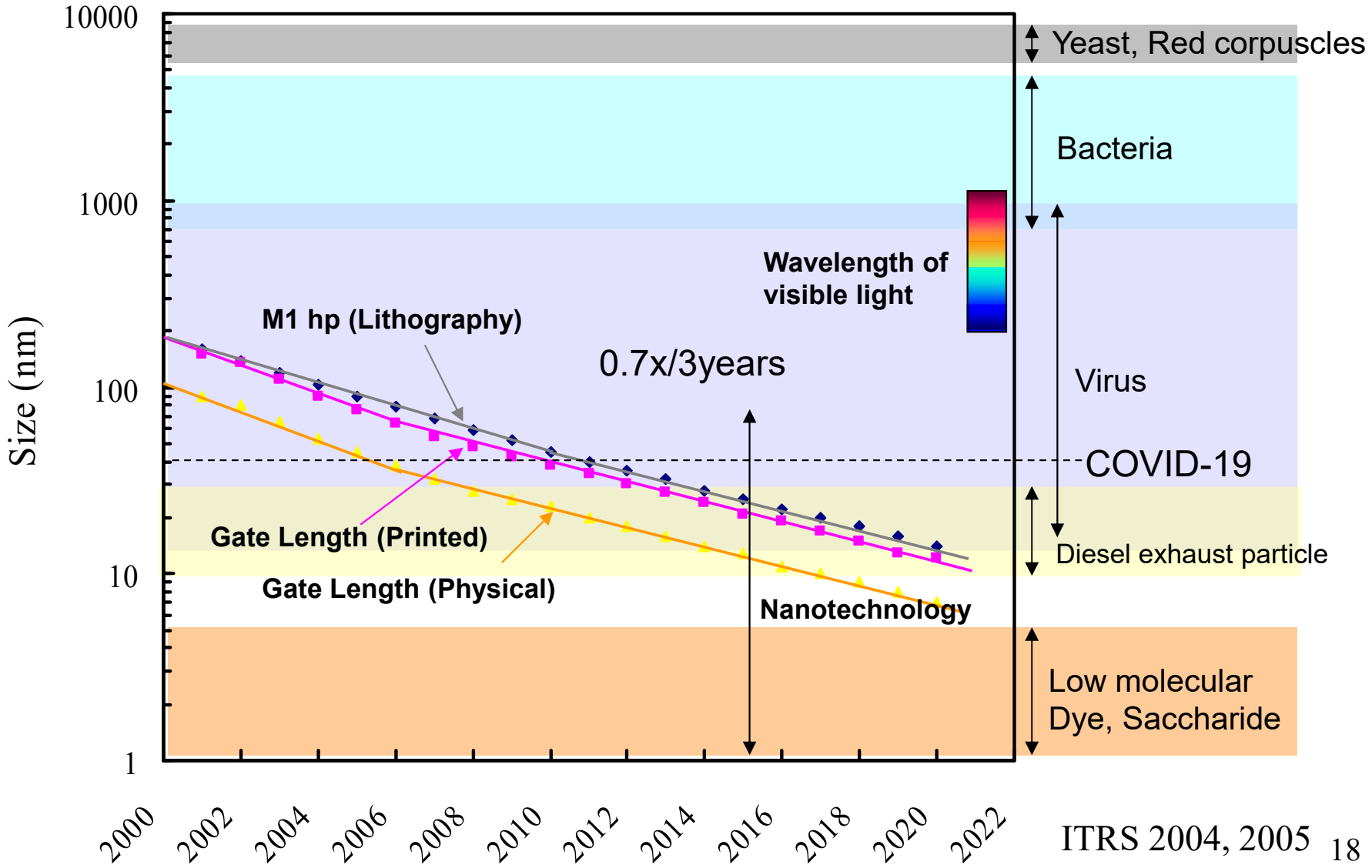
Terminology

- Process
  - means the manufacturing methods. This term focuses on the type of integrated devices.
- Technology
  - means the manufacturing methods. This term focuses on the feature size.
- Examples
  - "CMOS process" is a fabrication technology to integrate p-ch MOSFETs and n-ch MOSFETs.
  - "CMOS 7nm technology" is a CMOS process to microfabricate 7nm structure.

Scaling trends

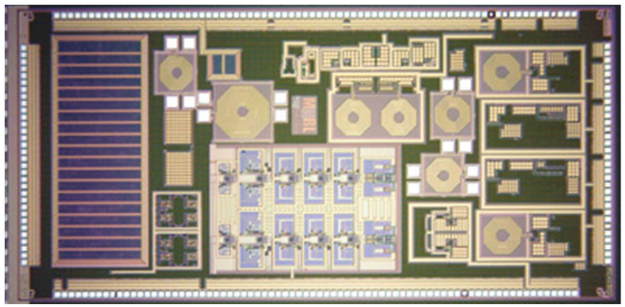


Comparison in size



ITRS 2004, 2005

Trends of operating frequency



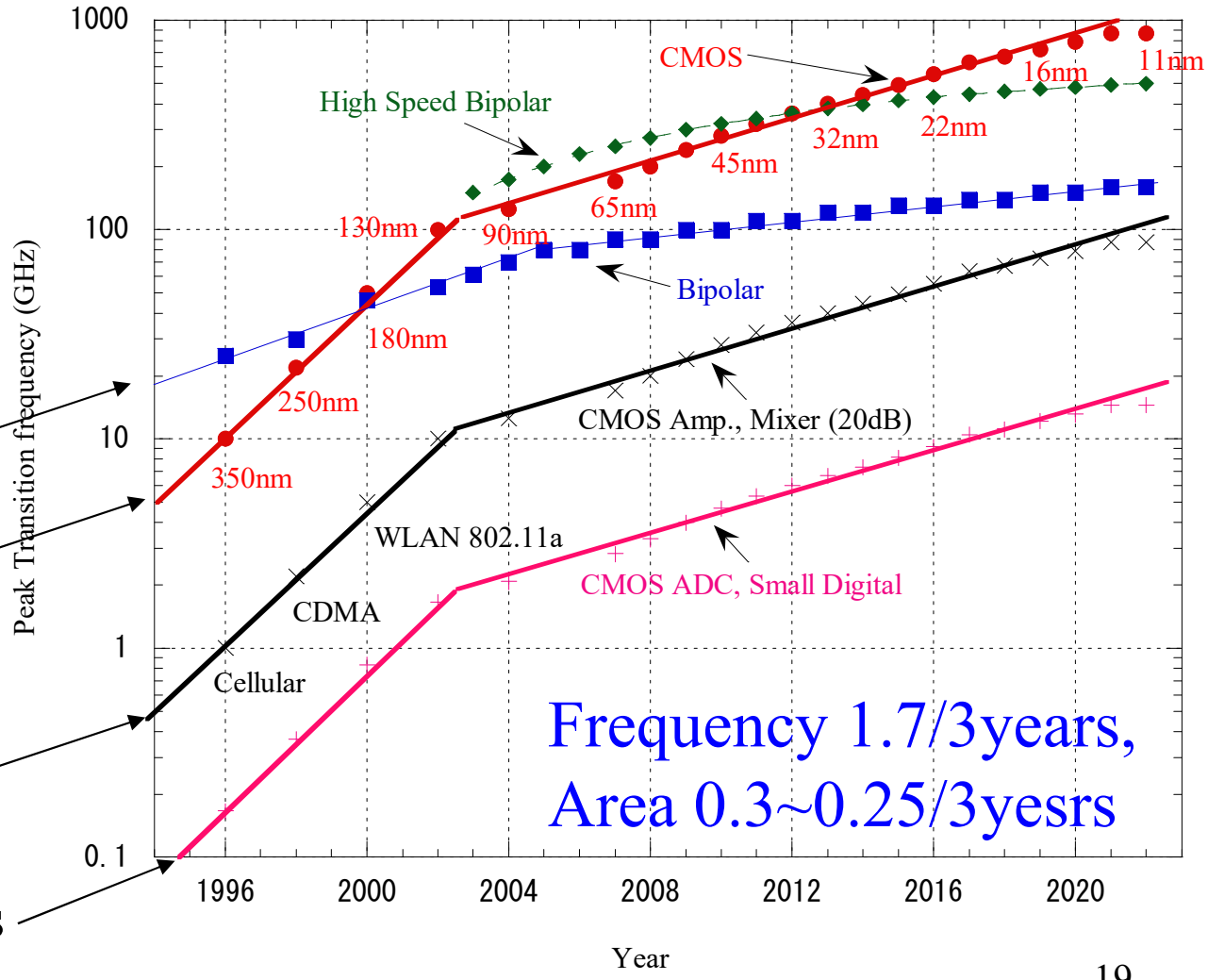
RF-LSI (developed by MeRL)

Bipolar transistor

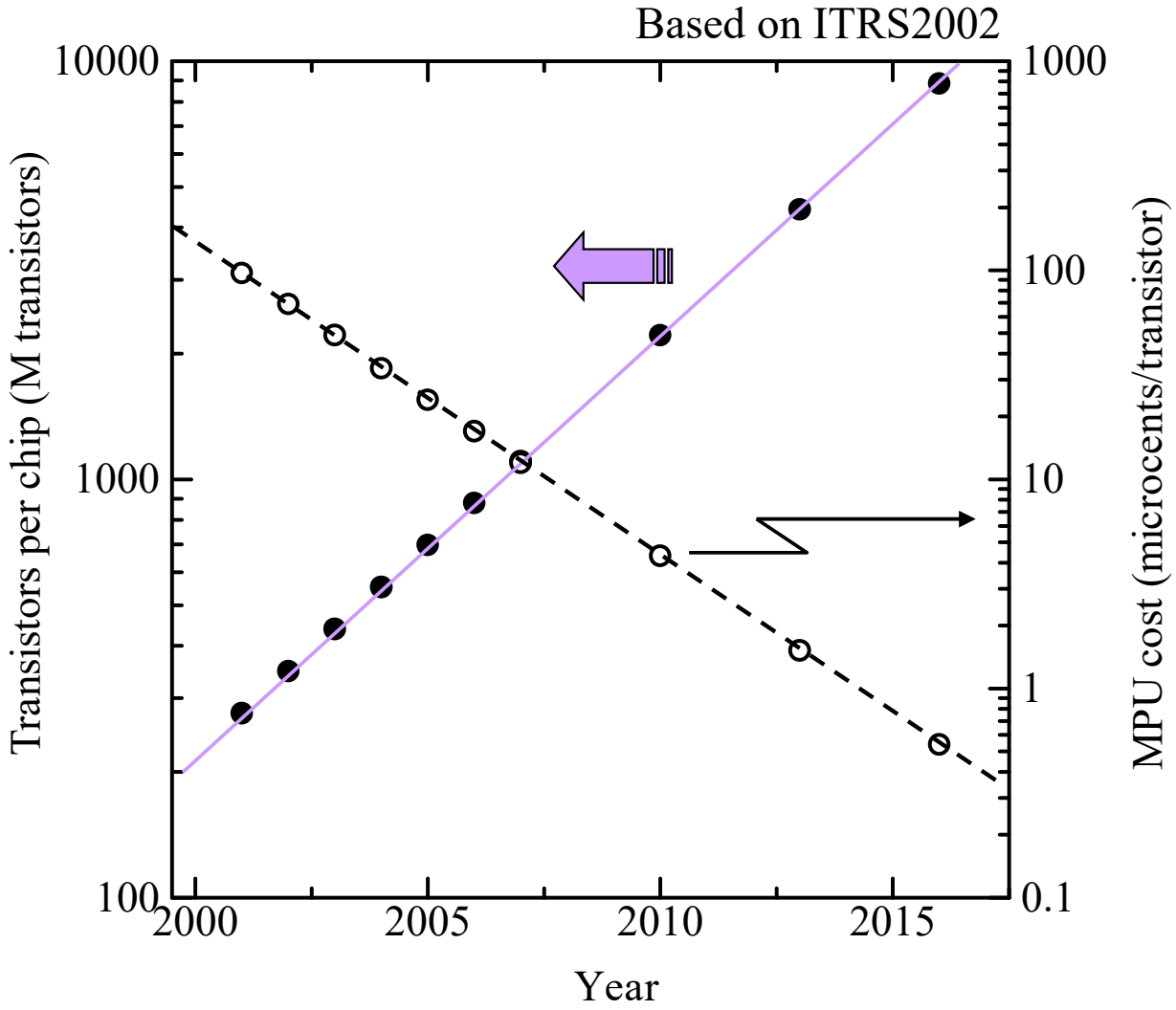
MOSFET

Analog circuits

Digital circuits

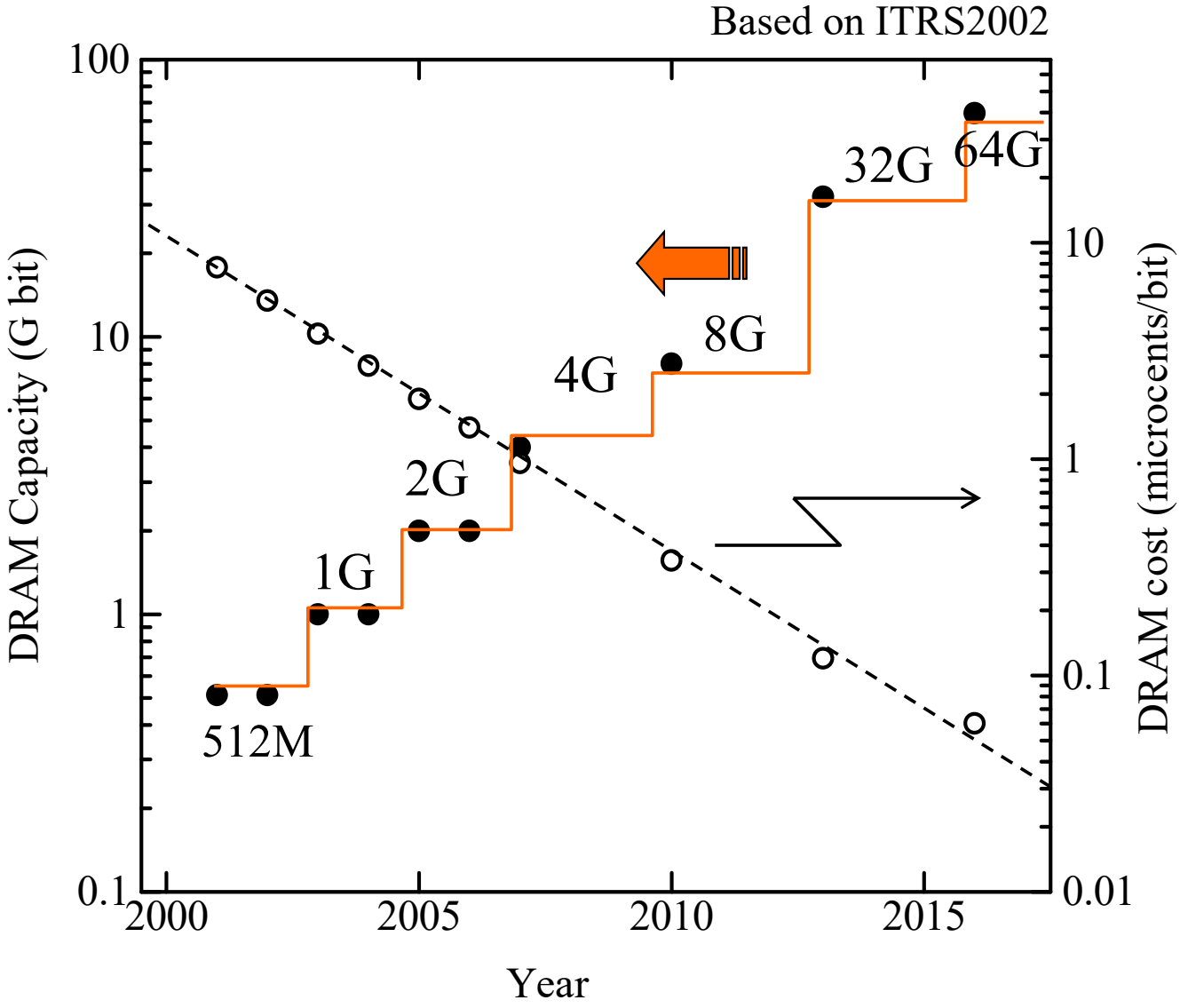


Trends of logic LSI cost



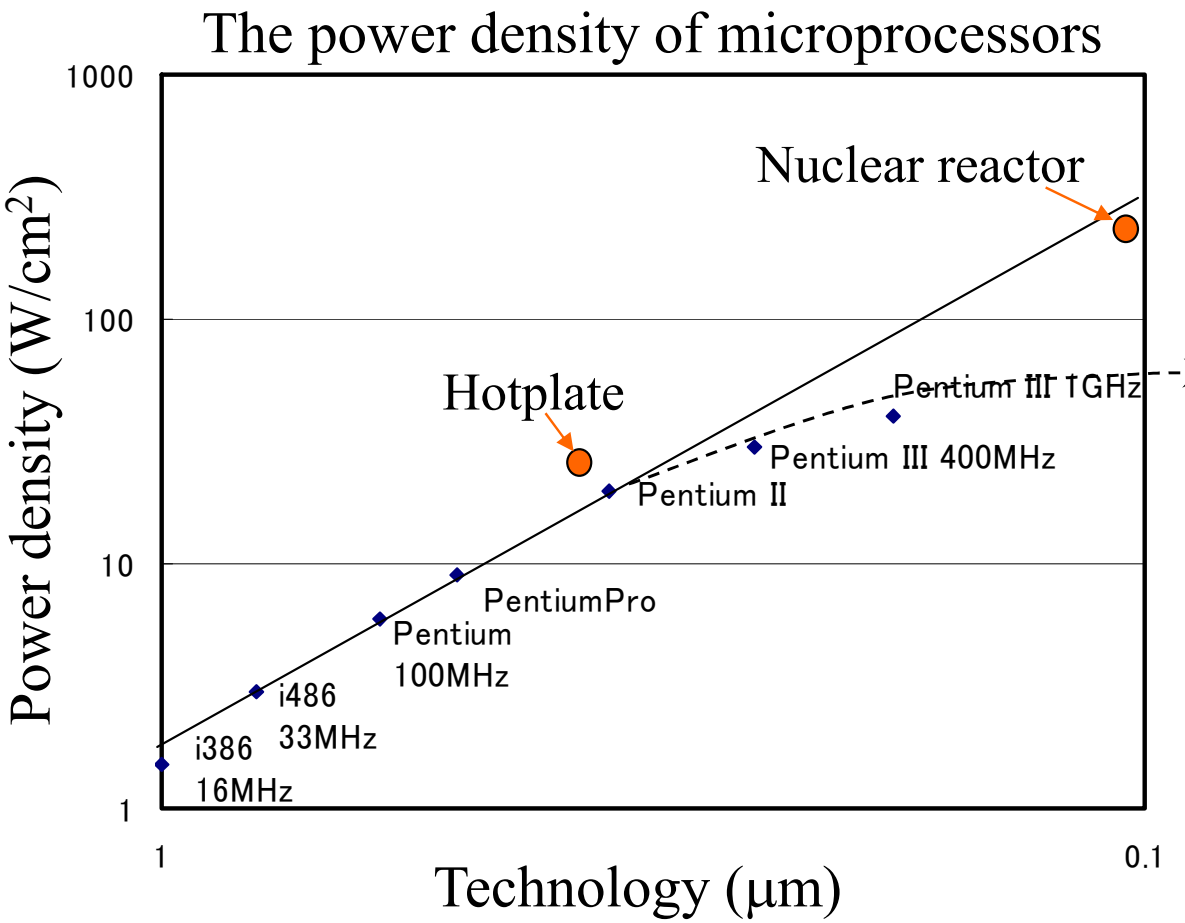
Cost of high-performance logic LSI having SRAM

Trends of DRAM cost



Exothermic density issue

The power consumption is proportional to the operating speed (clock frequency).



Multicore processor, Quantum computer

The performance of microprocessor is evaluated by power density/operating speed.

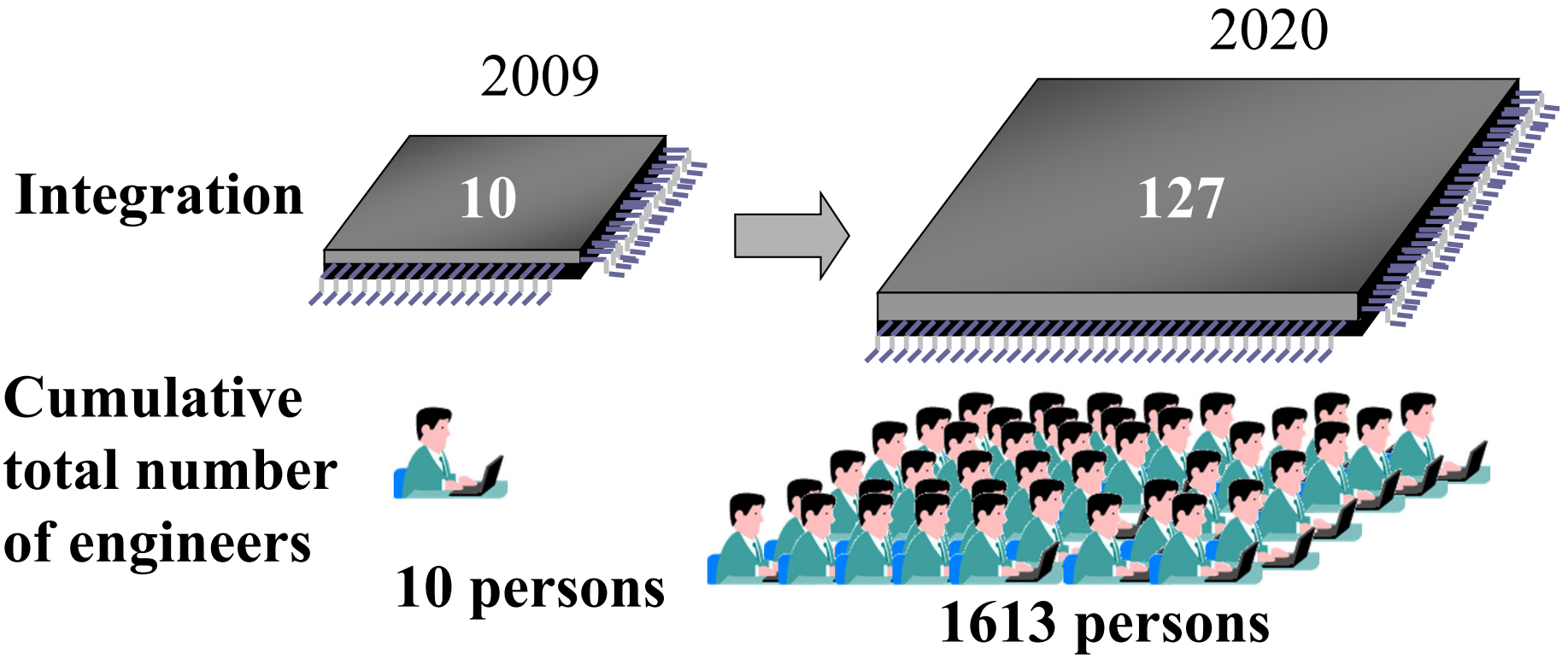
[参考] 半導体の微細化限界

- 最終的な限界 ⇒ 技術進歩の必要性に依存
- 物理的限界（材料）、技術的限界（微細加工）、経済合理性(ビジネスとして成り立つかどうか)では限界が決まらない
  - 多くの微細化限界説が提唱されたが、その度に新しい解決策も提案されてきた
  - 時代は、そこで生活する人々が創るものであり、時代を支える技術は必要性によって生み出されていることを、LSI技術の歴史が示している

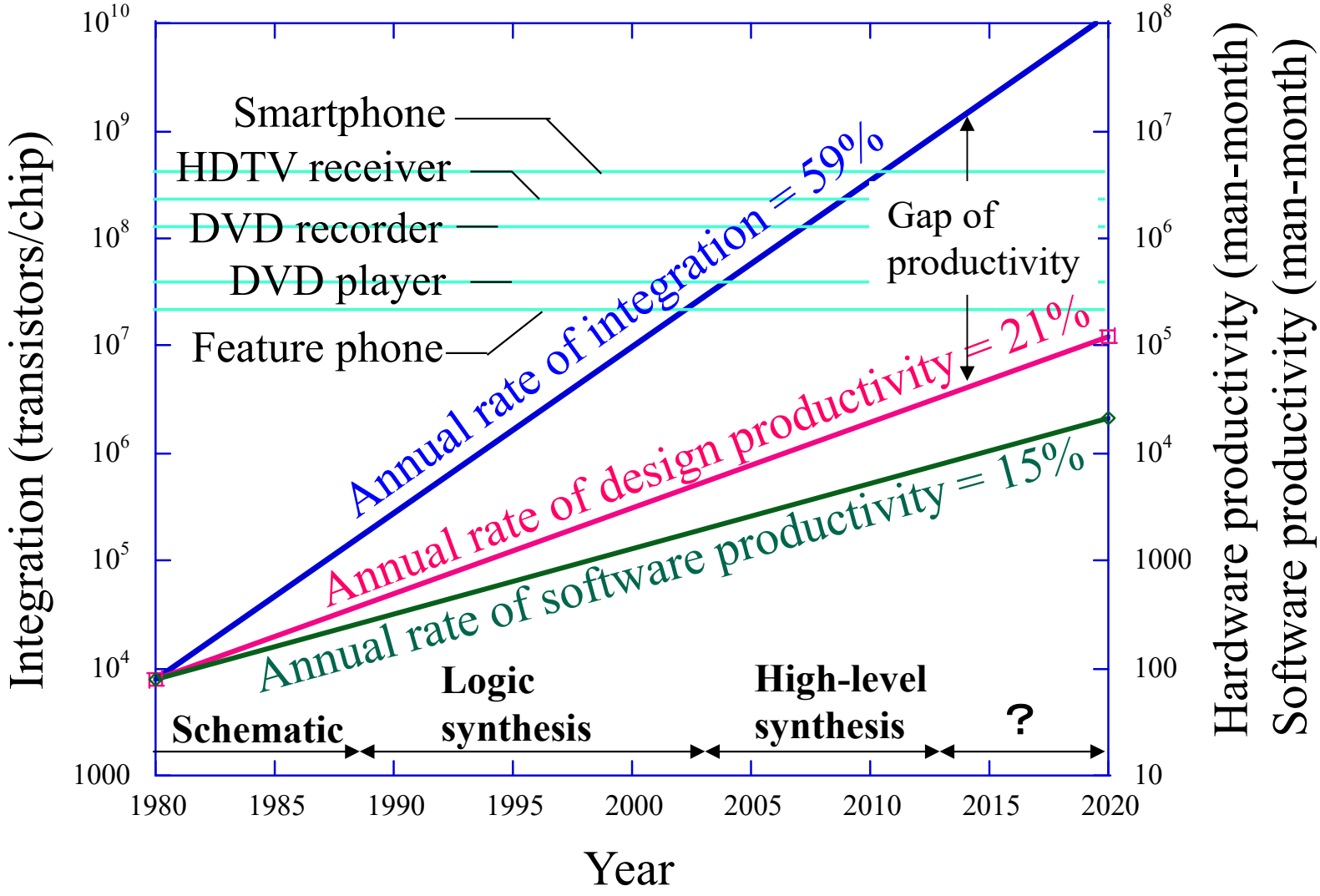
1.1.3 Trends of design technology

Explosive increase in design workload

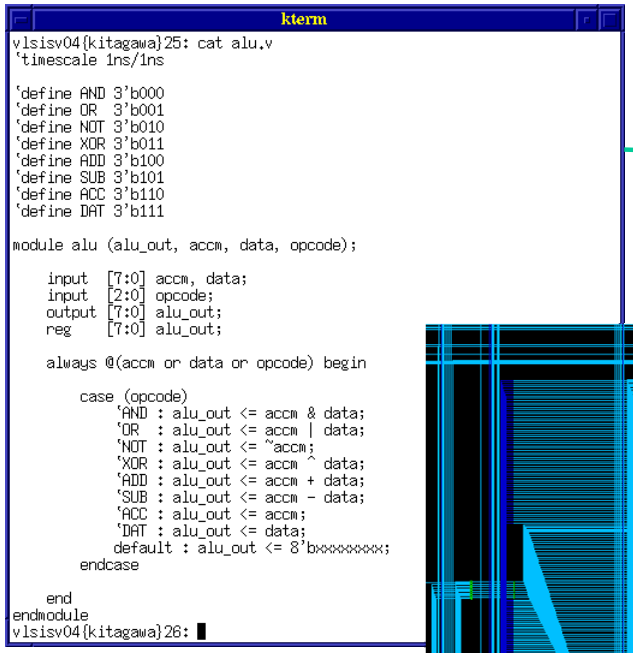
The workload of the LSI design is increasing fourfold with increasing twofold the circuit scale.



Productivity of LSI design

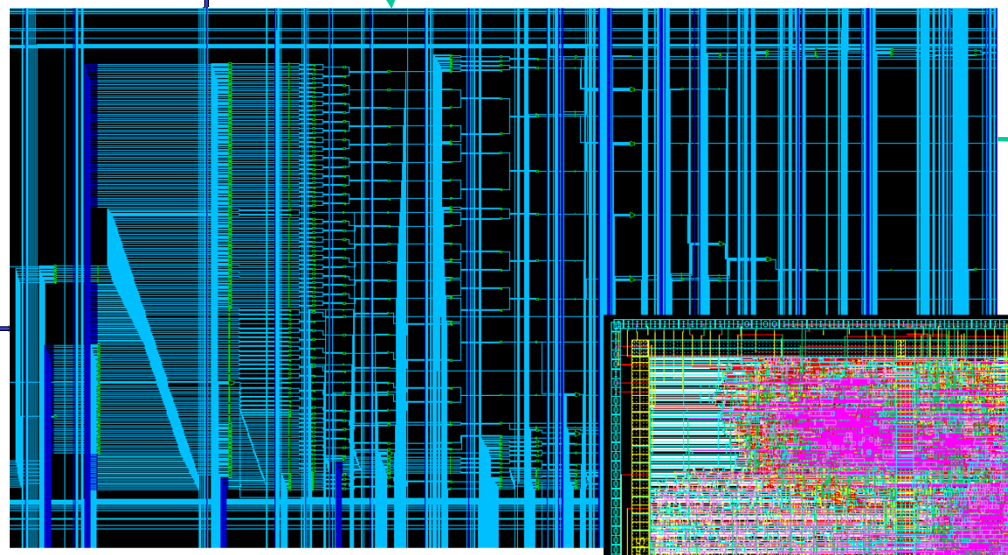


EDA (Electronic design automation)



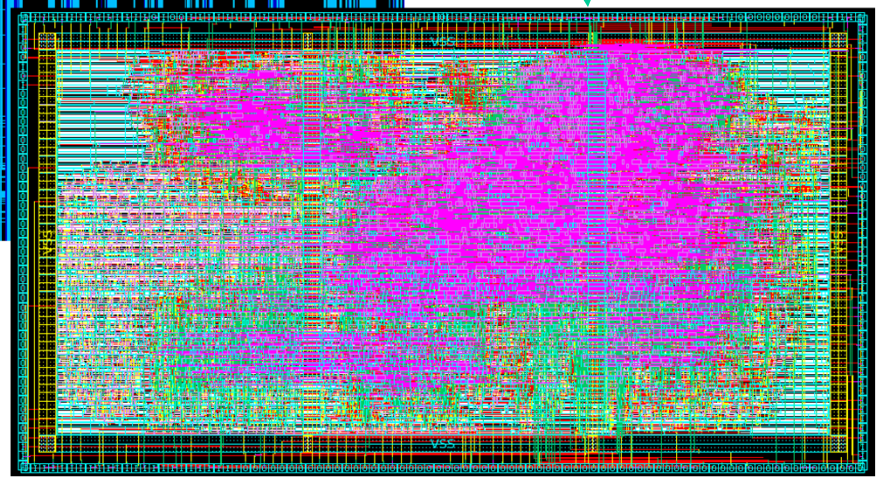
HDL code

Logic synthesis



Schematic

Place & route



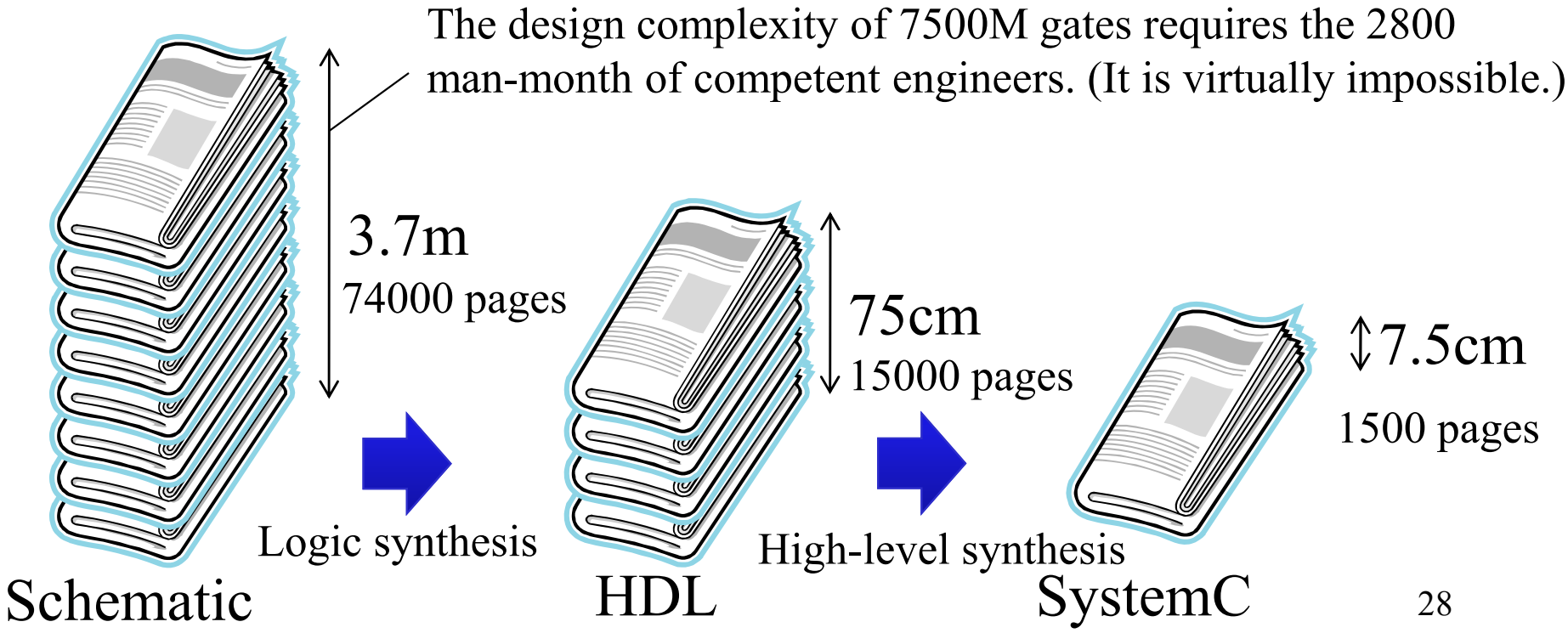
Layout

HDL: Hardware Description Language

Enhancement of productivity

A high-level abstraction reduces the quantity of the code.

The technology that automatically generates low-level descriptions from high-level abstraction is required to design LSI.



Design verification

- Simulator
  - Circuit simulator
  - Logic simulator (HDL simulator)
  - High level synthesis tool (*)
- Emulator
  - A development of SoC (System on a chip) requires the hardware emulation system which perform a high-speed simulation of the LSI behavior by the hardware accelerator.
  - The emulator system provides the virtual transaction from the peripherals.

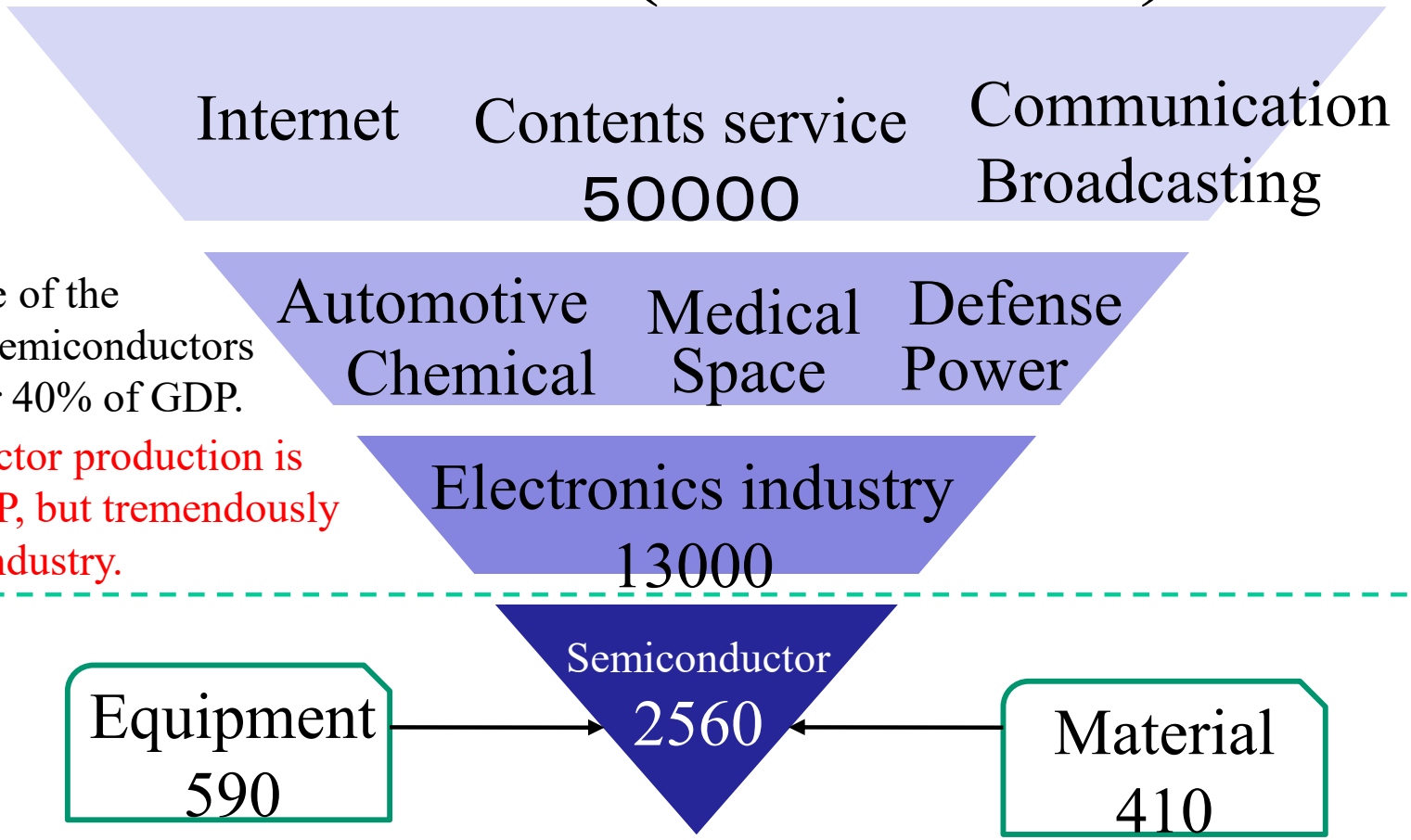
7200M gates emulator
@Kanazawa University

600M gates emulator
@Kanazawa University

* High level synthesis tool = CAD which compile a code written in high-level language into HDL.

1.1.4 Industrial structure

Industrial structure in the post-Cold War (産業の米)



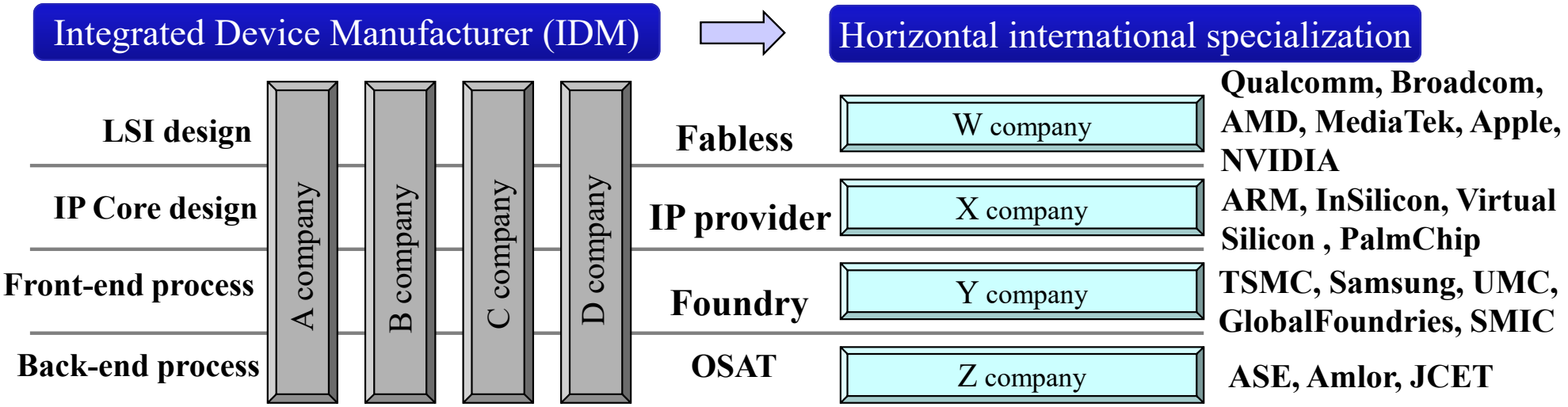
The market size of the application of semiconductors in Japan is over 40% of GDP.

The semiconductor production is only 1% of GDP, but tremendously influences all industry.

Unit: 100M$

Source: F. Huang, Green IT international symposium
IC Handbook, JEITA, 2009.

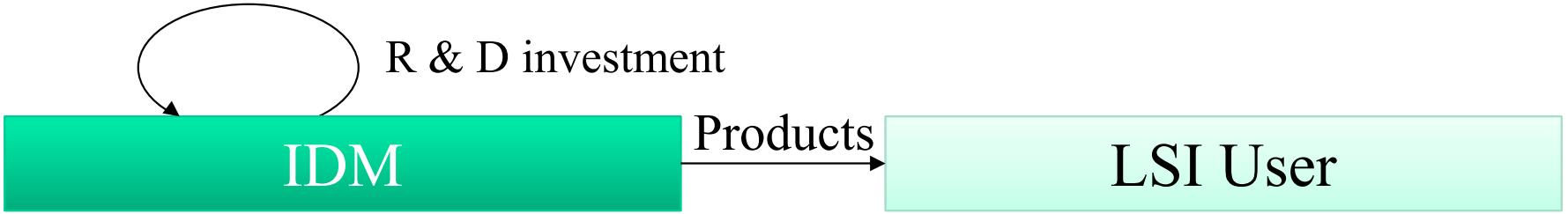
Changes in the industrial structure in 1990s



	IDM	Fabless	IP provider	Foundry	OSAT	University
Design	○	○	○	×	×	○
Front-end process	○	×	×	○	×	×
Back-end process	○	×	×	△	○	×
Test	○	×	×	×	○	○
Own capitalized	○	×	×	×	×	○
OEM supply	○	○	○	○	○	×
Own branded products supply	○	○	×	△	△	×

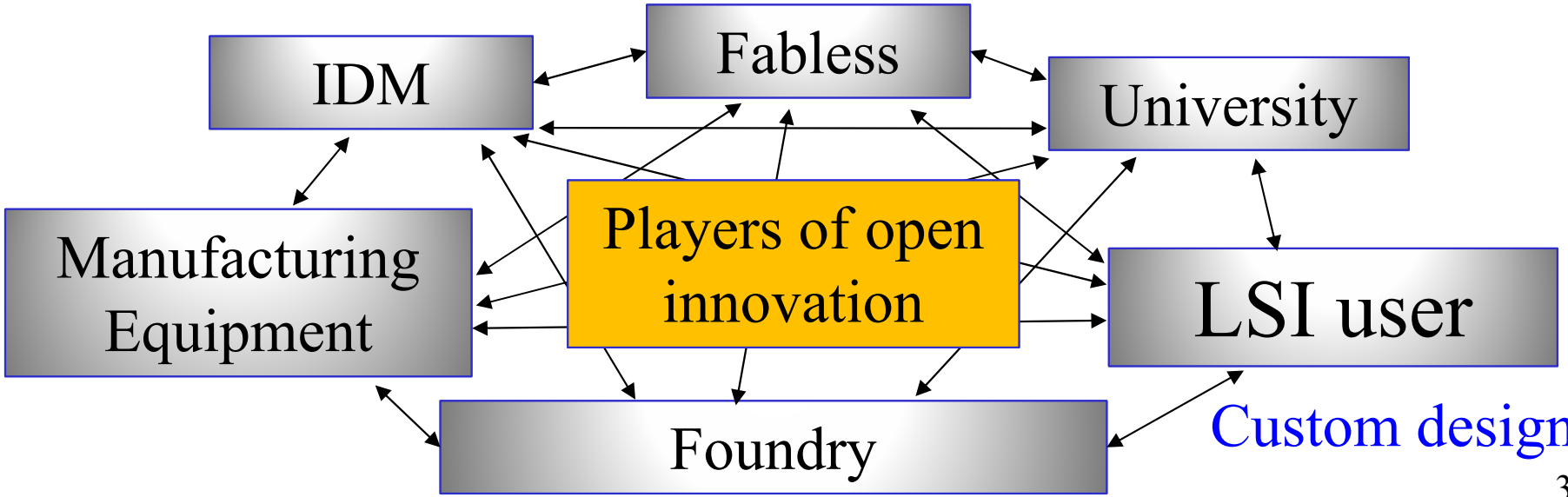
NOTE: IP (Intellectual Property) is a software and hardware assets which can be embedded into LSI.
OSAT: Outsourced Semiconductor Assembly & Test

Advancement of open innovation



Mass production of general-purpose products

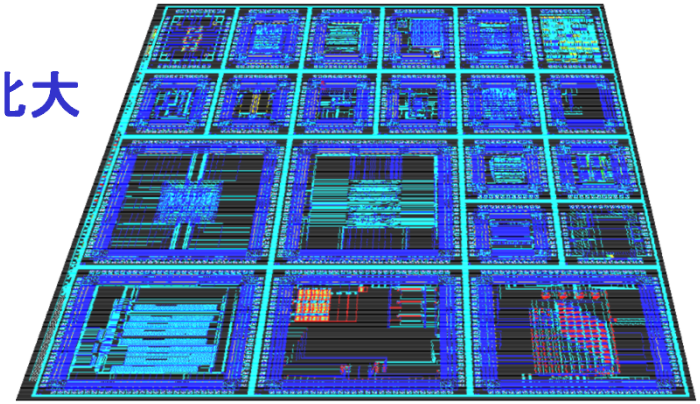
After 2010



Custom design

VLSI Design and Education Center (VDEC) is established in 1996.

Hokuriku VDEC sub-center



Multi-project chip of VDEC

VDEC is a national academic network by10 universities to provide the CAD software license and LSI manufacturing service.

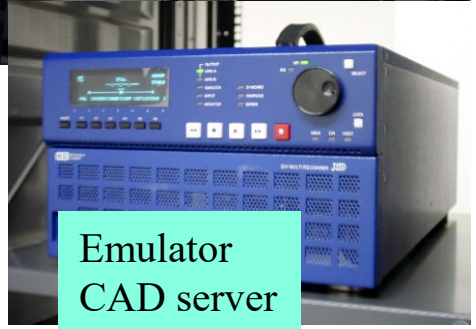
Hokuriku VDEC subcenter in Kanazawa University

Terminals for design practice

VDEC design room

LSI tester
Clean room

VDEC test room



Emulator
CAD server

VDEC server room

要点の日本語解説

- 半導体産業の構造変化
  - 国際的水平分業によりファブレス（LSI製造の外注）が可能になった
  - ユーザを中心とするオープンイノベーションが進行している
  - LSIは買ってくるのではなく、必要なものを自分で設計し、製造外注することが常識になっている
- 量産からカスタム指向への変化
  - 2010年以降、LSI設計者は、半導体メーカではなく、各アプリケーション領域に分散している
  - 新しい技術を使って、「何を作ればよいか」を考え、付加価値を生み出す考え方が必要
  - 情報通信産業の全体像を理解するための基礎としてLSI設計技術の知識が必要