2.2 CMOS static logic gates

The design of primitive logic gates

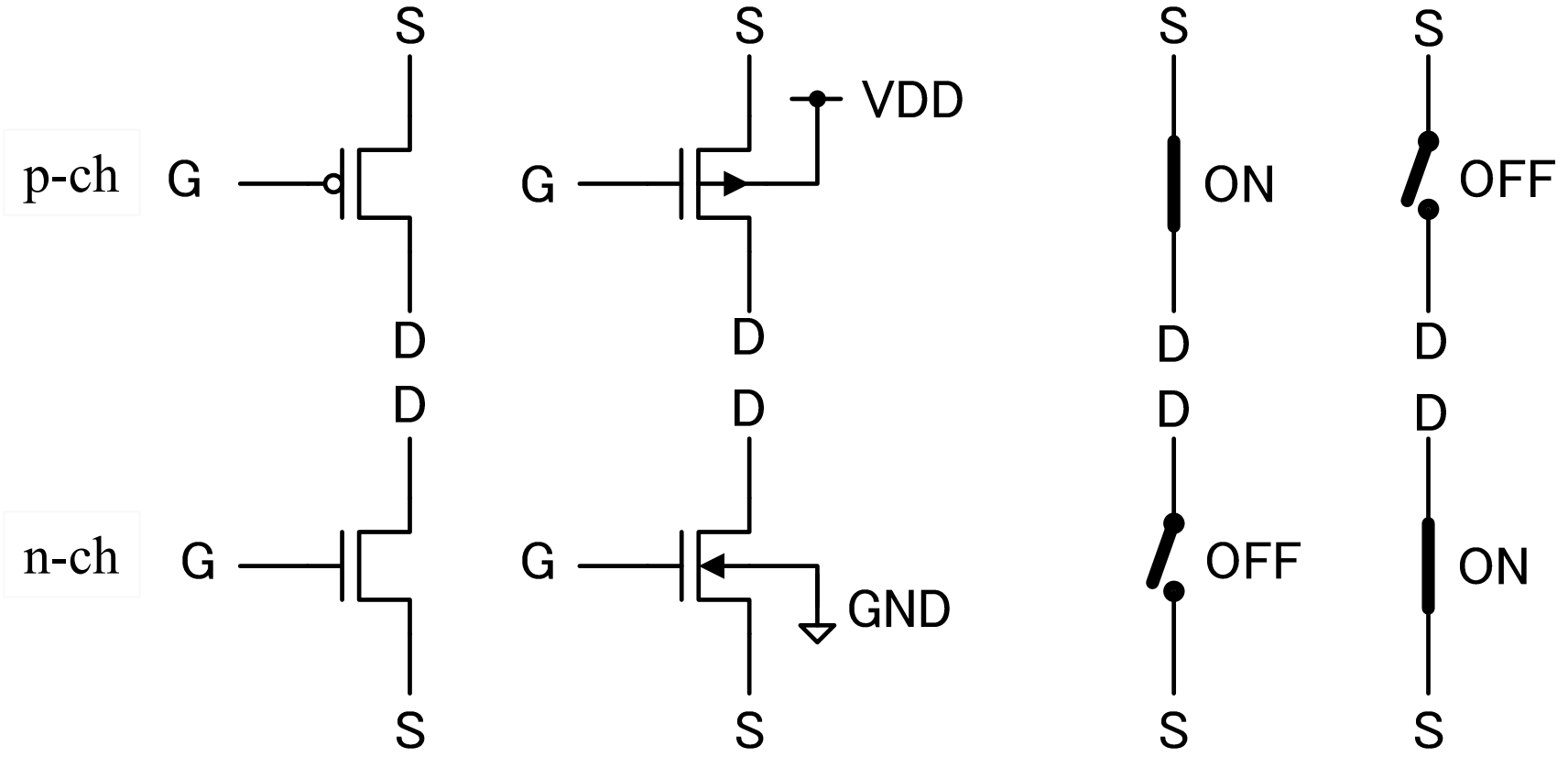
CMOS

CMOS = Complementary MOS

This term has two meanings.

- The process technology to integrate p-ch MOSFETs and n-ch MOSFETs
- The circuit structure with p-ch MOSFETs and n-ch MOSFETs

MOSFET switch

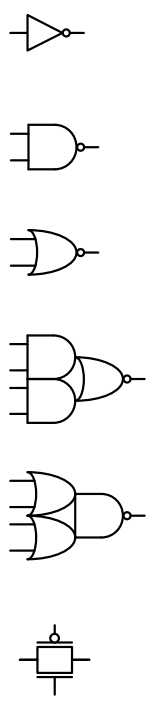
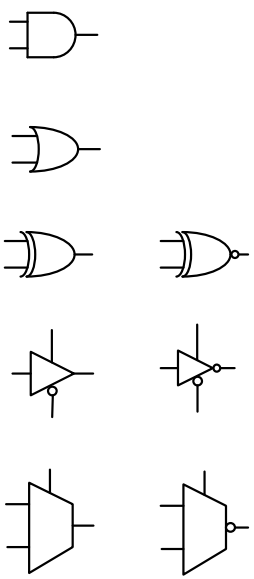
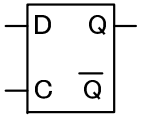
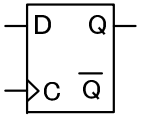


MOSFET symbol with 3 terminals

MOSFET symbol with 4 terminals

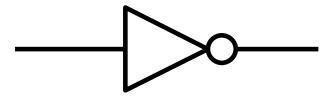
V_G = Low V_G = High
Analogy of switch

Primitive logic gates

Combinational logic		Sequential logic	
1 stage	2 stages	Latch	Flip-flop
			

Inverter

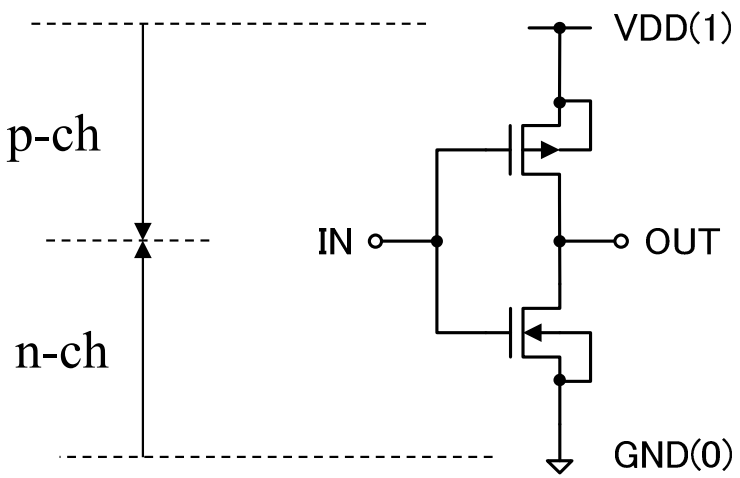
Symbol

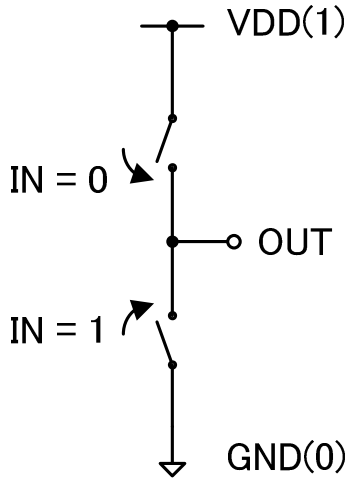


Truth table

IN	OUT
0	1
1	0

Schematic





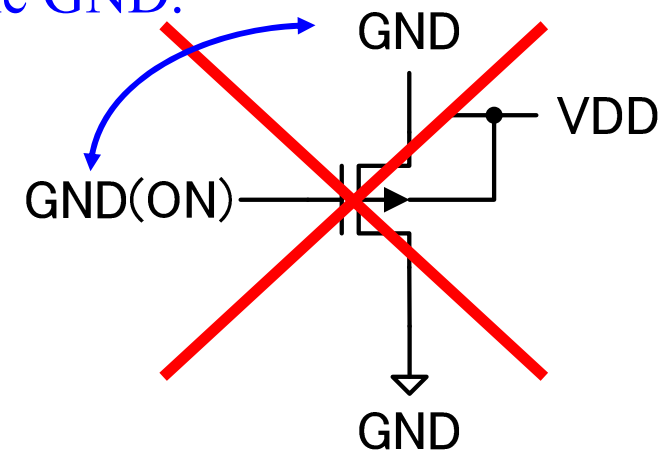
The terminal of OUT is switched to VDD or GND.

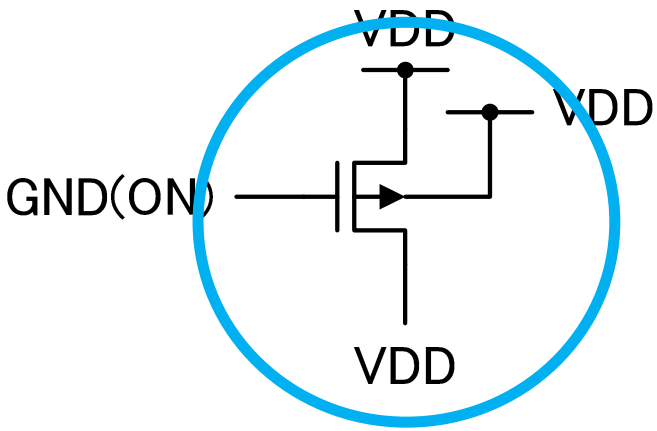
Connection of body terminal

The MOSFET cannot turn on the GND.

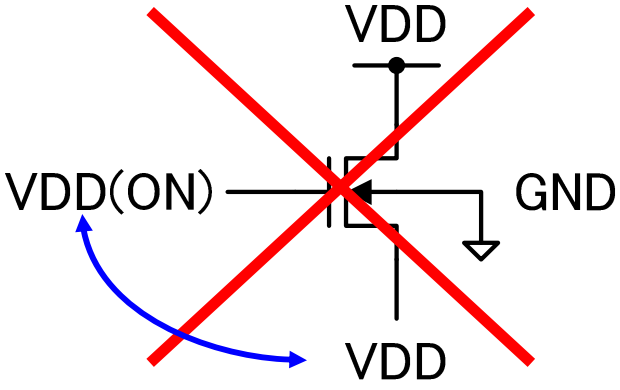
A p-ch MOSFET can output VDD.

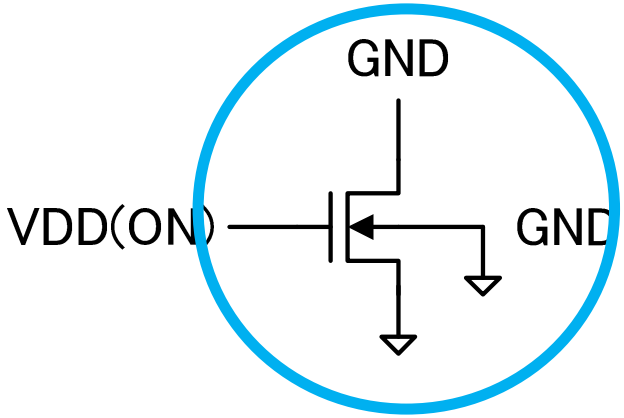
p-ch





n-ch

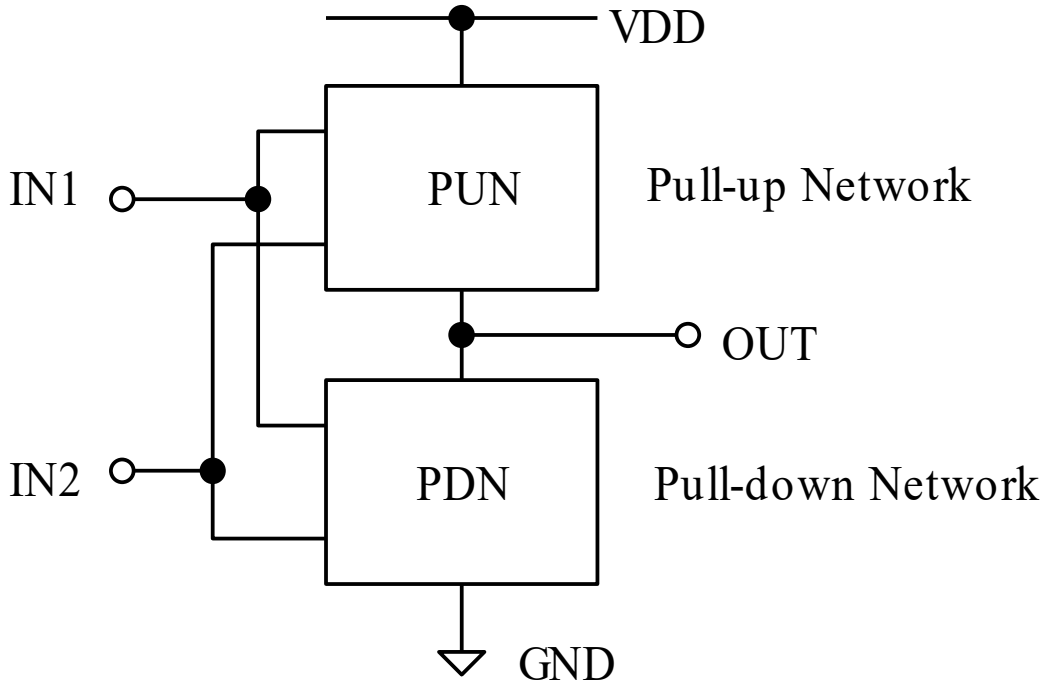




The MOSFET cannot turn on the VDD.

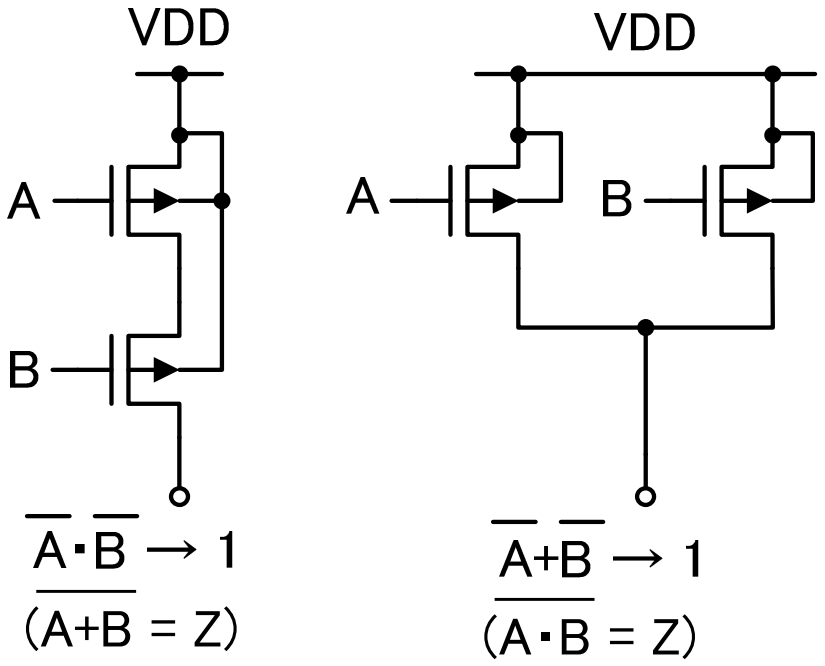
A n-ch MOSFET can output GND.

General form of the static logic



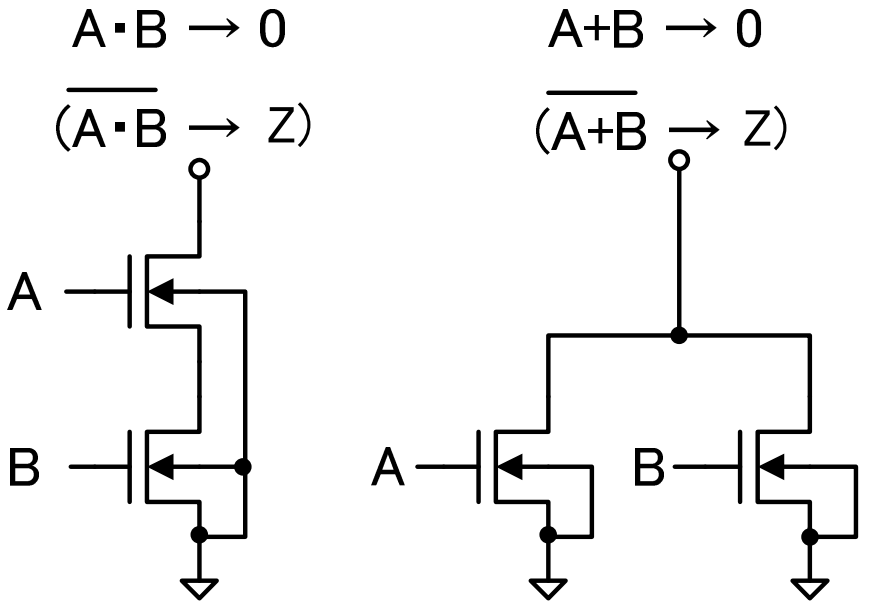
- A pull-up network is a switch network for VDD.
- A pull-down network is a switch network for GND.

2-input switch networks



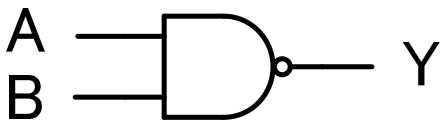
PUN consists of p-ch MOSFETs.

PDN consists of n-ch MOSFETs.



Function of 2-input NAND

Symbol



Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

de Morgan's laws

$$Y = \overline{A} + \overline{B} \longrightarrow \text{p-ch MOSFET network}$$

$$= \overline{A \cdot B} \longrightarrow \text{n-ch MOSFET network}$$

At first, find 2 equivalent Boolean expressions.

(1) The expression of each variable negation
(2) The expression of the total negation

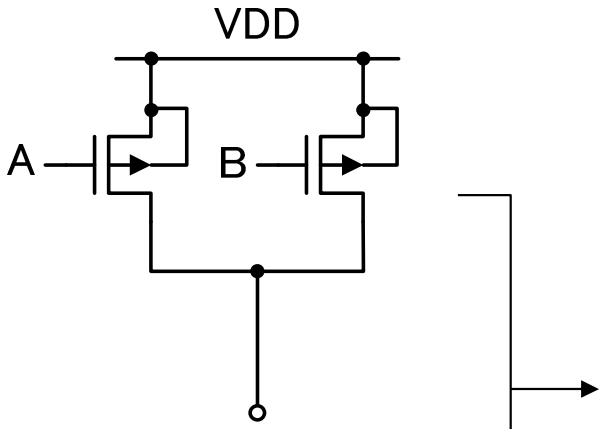
Note: If you cannot find the equivalent Boolean expressions, there is no logic circuit that consists of 1-stage.

Design of 2-input NAND

$$Y = \begin{cases} \overline{A} + \overline{B} \longrightarrow \text{PUN} \\ \overline{A \cdot B} \longrightarrow \text{PDN} \end{cases}$$

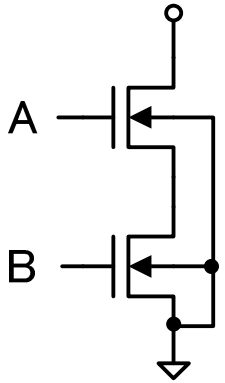
PUN

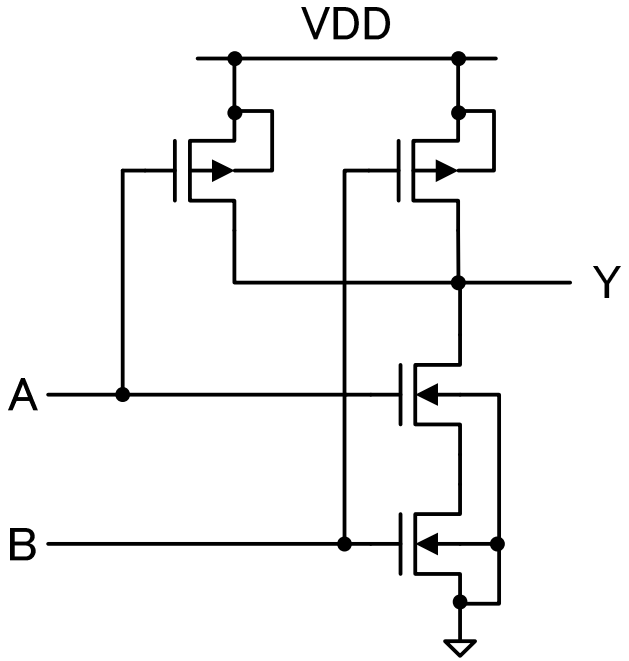
If A=0 OR B=0, then Y=1



PDN

If A=1 AND B=1, then Y=0

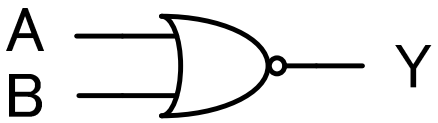




Connection of PUN and PDN

Function of 2-input NOR

Symbol



Truth table

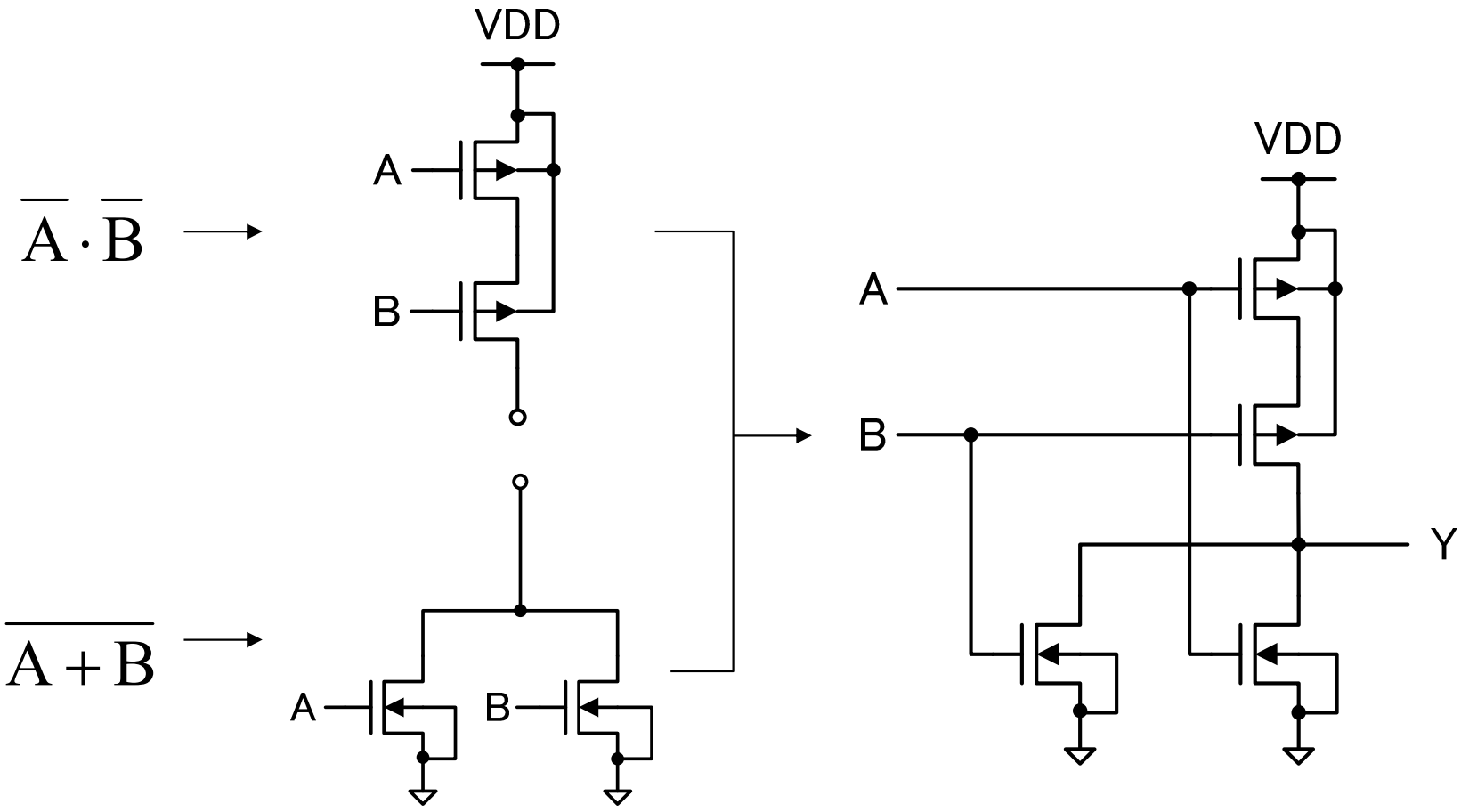
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

de Morgan's laws

$$Y = \overline{A} \cdot \overline{B} \longrightarrow \text{p-ch MOSFET network}$$

$$= \overline{A + B} \longrightarrow \text{n-ch MOSFET network}$$

Design of 2-input NOR



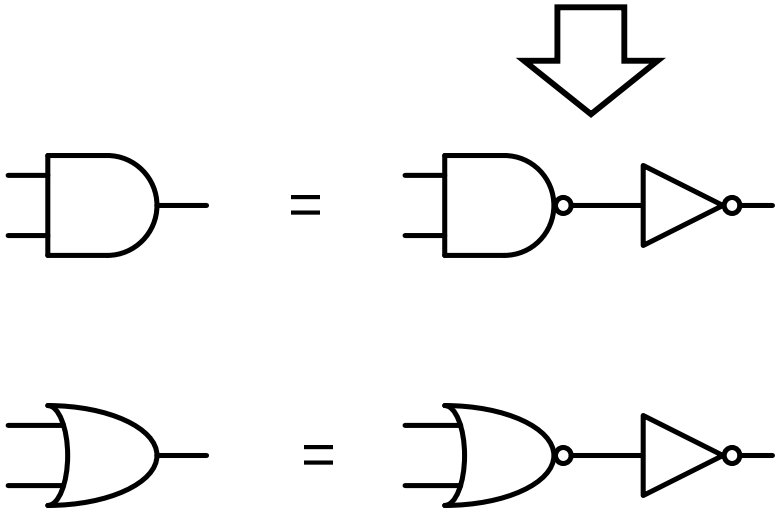
Connection of PUN and PDN

Design of AND, OR

$$\text{AND} \longrightarrow \quad A \cdot B = \overline{\overline{A} + \overline{B}}$$

$$\text{OR} \longrightarrow \quad A + B = \overline{\overline{A} \cdot \overline{B}}$$

PUN and PDN cannot build the operations shown above.

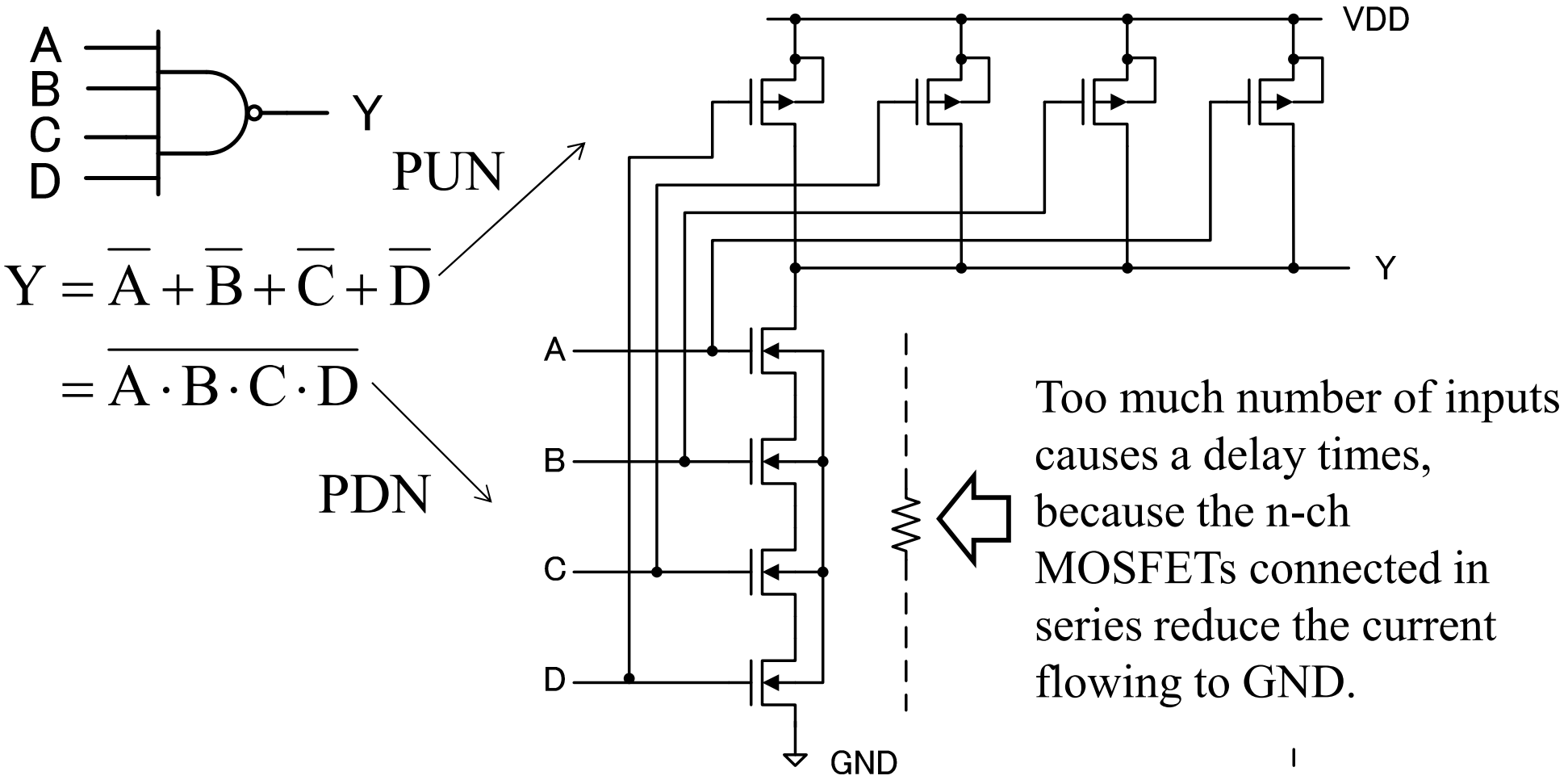


1-stage + 1 stage

AND operation and OR operation require 2 stage(*) logic circuits.

* Stage: 段数

Multi-input gates



DO not over 4-input.

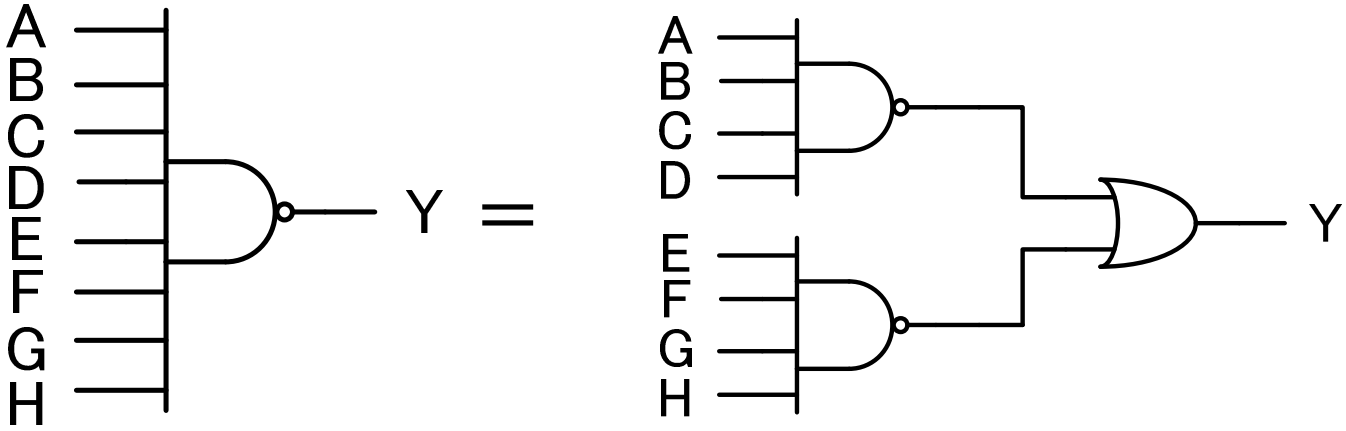
8-input NAND

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

$$= \overline{(A \cdot B \cdot C \cdot D) \cdot (E \cdot F \cdot G \cdot H)}$$

$$= \overline{A \cdot B \cdot C \cdot D} + \overline{E \cdot F \cdot G \cdot H}$$

de Morgan's laws



1 stage + 2 stages

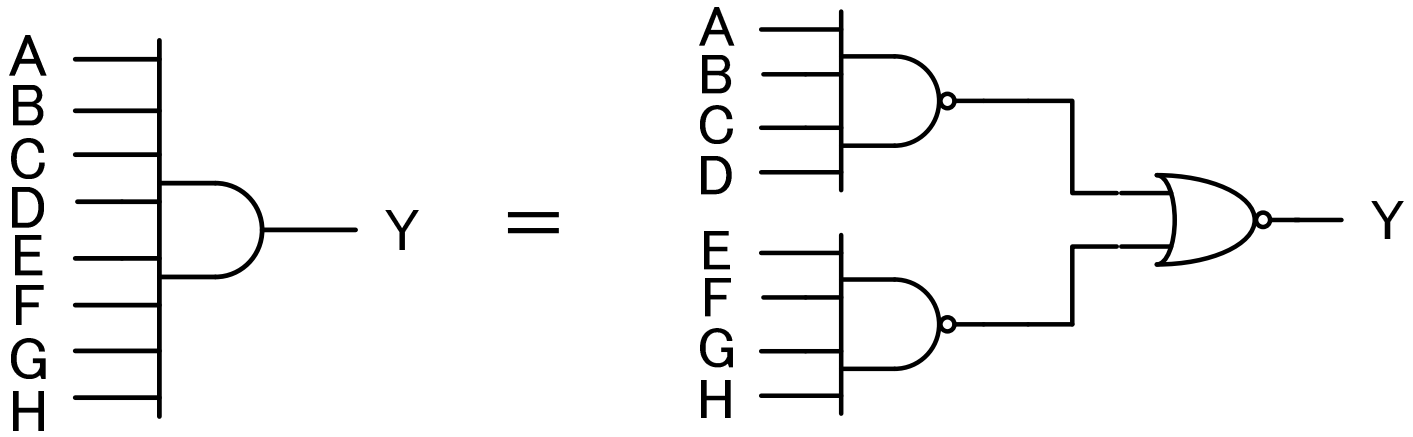
8-input AND

$$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$$

$$= (A \cdot B \cdot C \cdot D) \cdot (E \cdot F \cdot G \cdot H)$$

$$= \overline{\overline{A \cdot B \cdot C \cdot D} + \overline{E \cdot F \cdot G \cdot H}}$$

de Morgan's laws

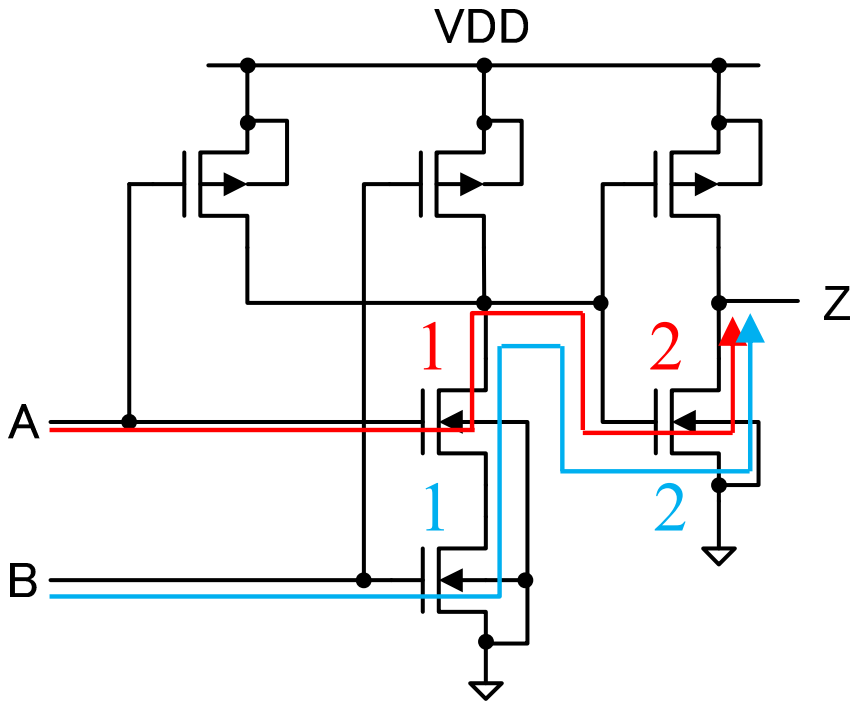


1 stage + 1 stage

Counting method of gate stages

- A number of stages is defined as a maximum number of gate electrodes of MOSFET on the path from an input port to an output port.

Example of 2- stage gate



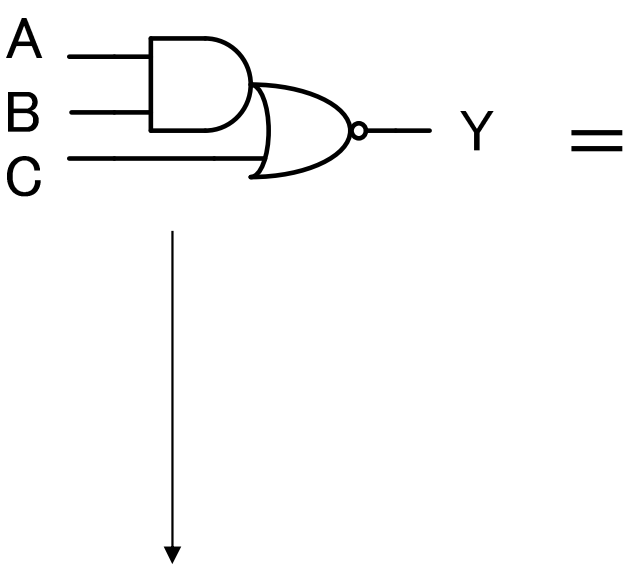
Propagation delay

- A propagation delay (伝搬遅延時間) is defined as a time between 50% points of input and output.
- The propagation delay t_{logic} of the logic circuit is estimated from the number of stages K and the propagation delay t_d of 1-stage gate.

$$t_{logic} = K \cdot t_d$$

3-input AND-NOR gate 1

$$Z = \overline{(A \cdot B) + C}$$



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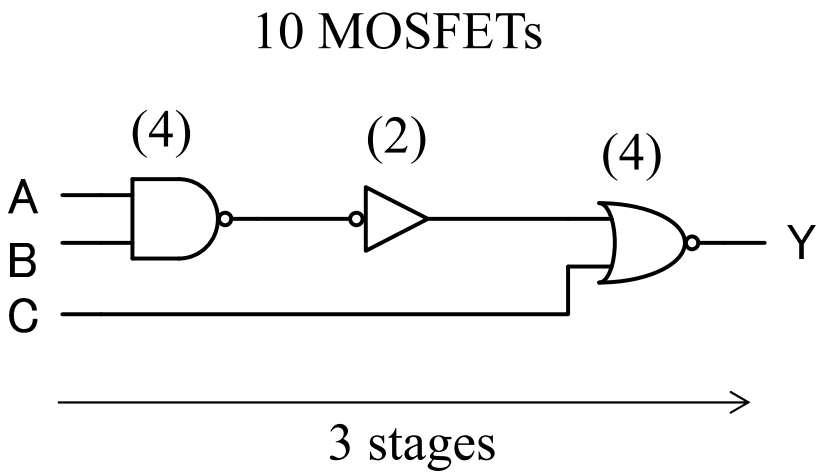


Construction by PUN and PDN

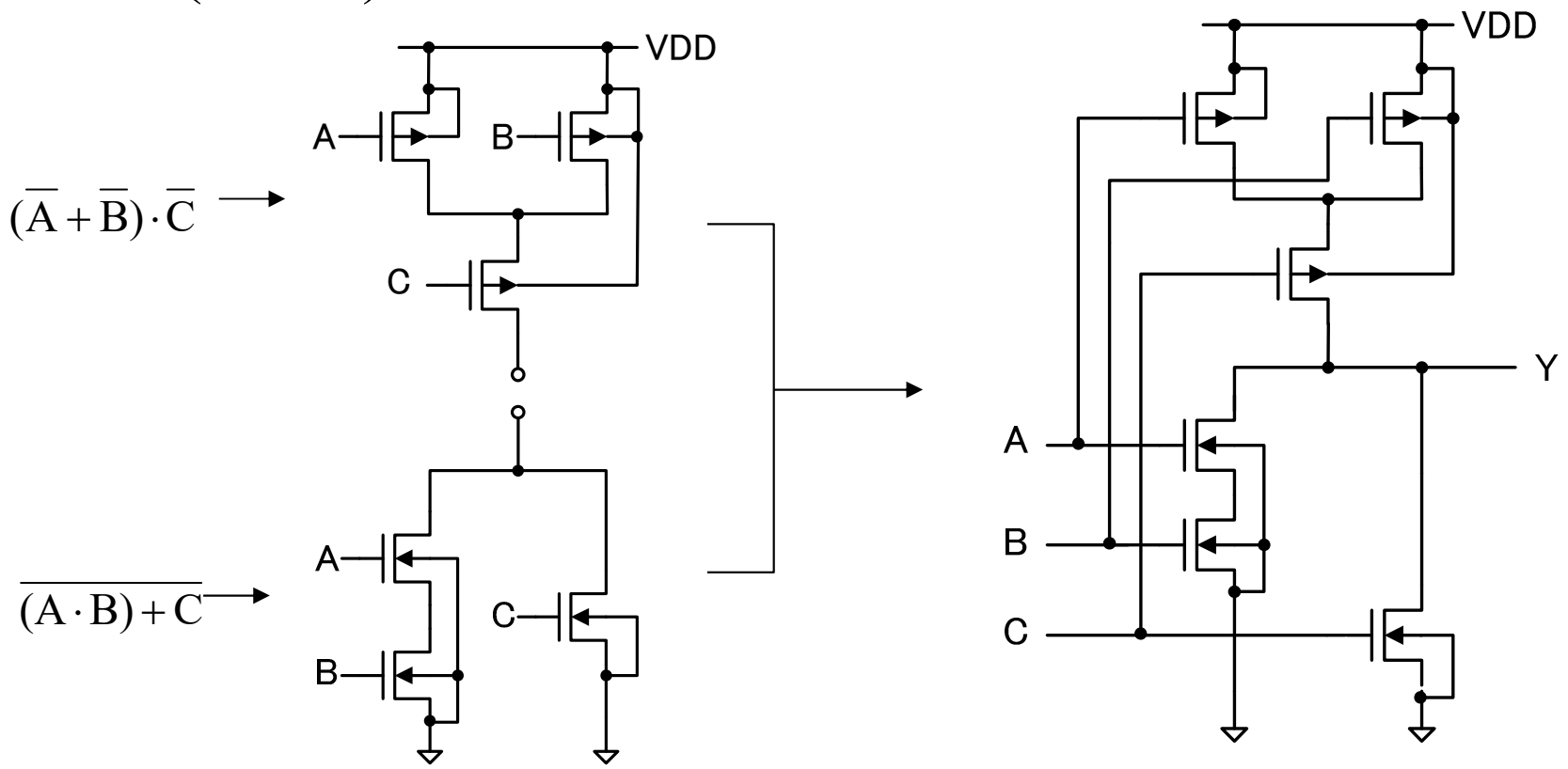
AND-NOR and OR-NAND are also called a complex gate (複合ゲート).

3-input AND-NOR gate 2

$$Y = \overline{(A \cdot B) + C}$$
$$= \overline{A \cdot B} \cdot \overline{C}$$
$$= (\overline{A} + \overline{B}) \cdot \overline{C}$$

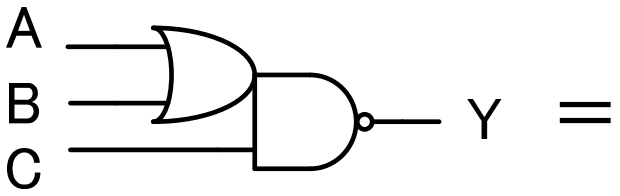
de Morgan's laws

6 MOSFETs, 1 stage



3-input OR-NAND gate 1

$$Y = \overline{(A + B) \cdot C}$$



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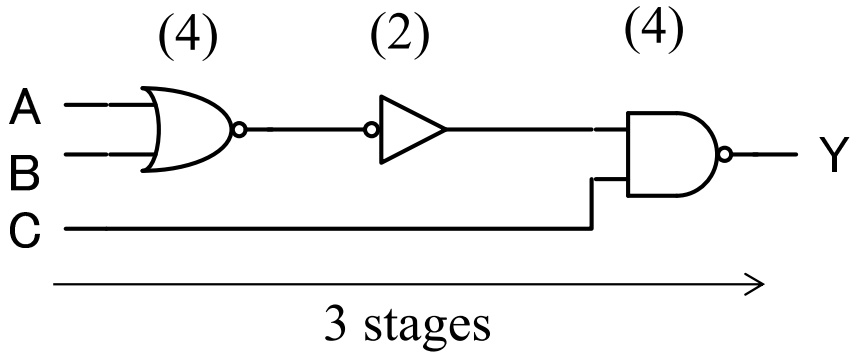
10 MOSFETs

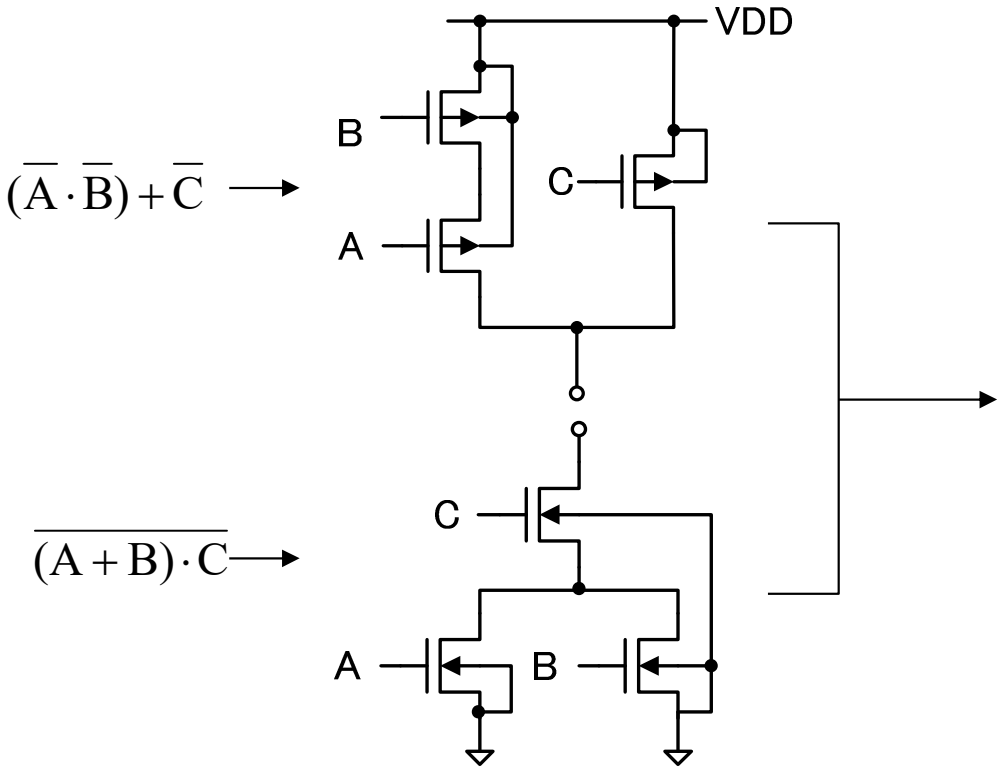


Construction by PUN and PDN

3-input OR-NAND gate 2

$$Y = \overline{(A + B) \cdot C}$$
$$= \overline{\overline{A + B}} + \overline{C}$$
$$= (\overline{A} \cdot \overline{B}) + \overline{C}$$

de Morgan's laws



6 MOSFETs, 1 stage