

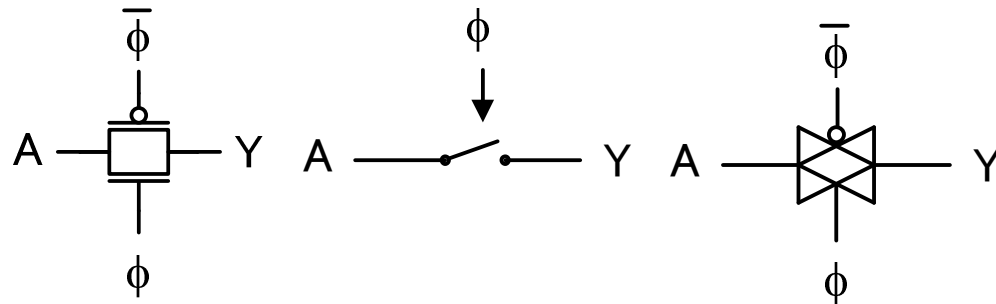
2.3 Transmission gate and tristate

Design of condition branch circuit

2.3.1 Transmission gate (TG)

Function of TG

Transmission Gate = TG



Various symbols of TG

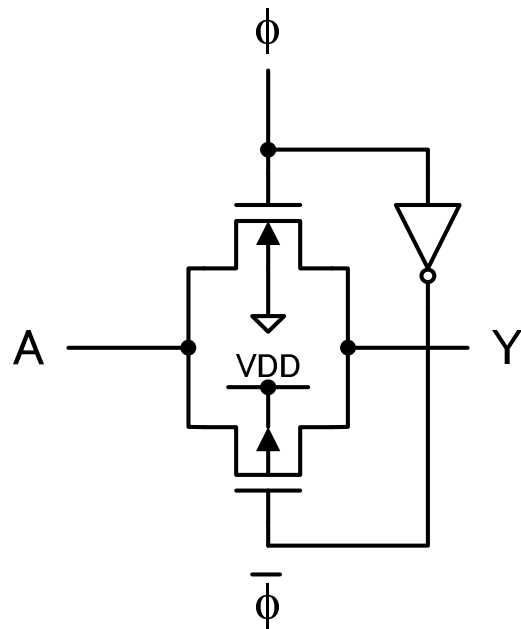
ϕ	A	Y
0	0	high Z
0	1	high Z
1	0	0
1	1	1

The high Z means [high-impedance](#) state.

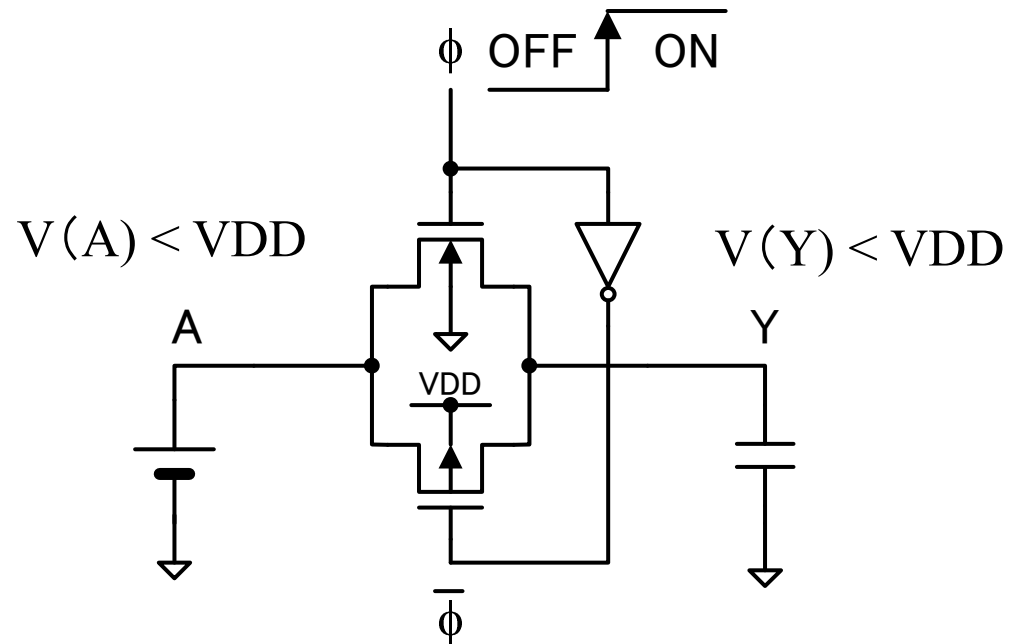
PUN and PDN are switch network to output a power supply voltage or a ground voltage. On the other hand, TG is a switch element between the input and the output.

The output voltage equals to input voltage when $\phi = '1'$. Thus, this circuit can be usable as a switch of analog signal ([analog switch](#)).

CMOS circuit of TG

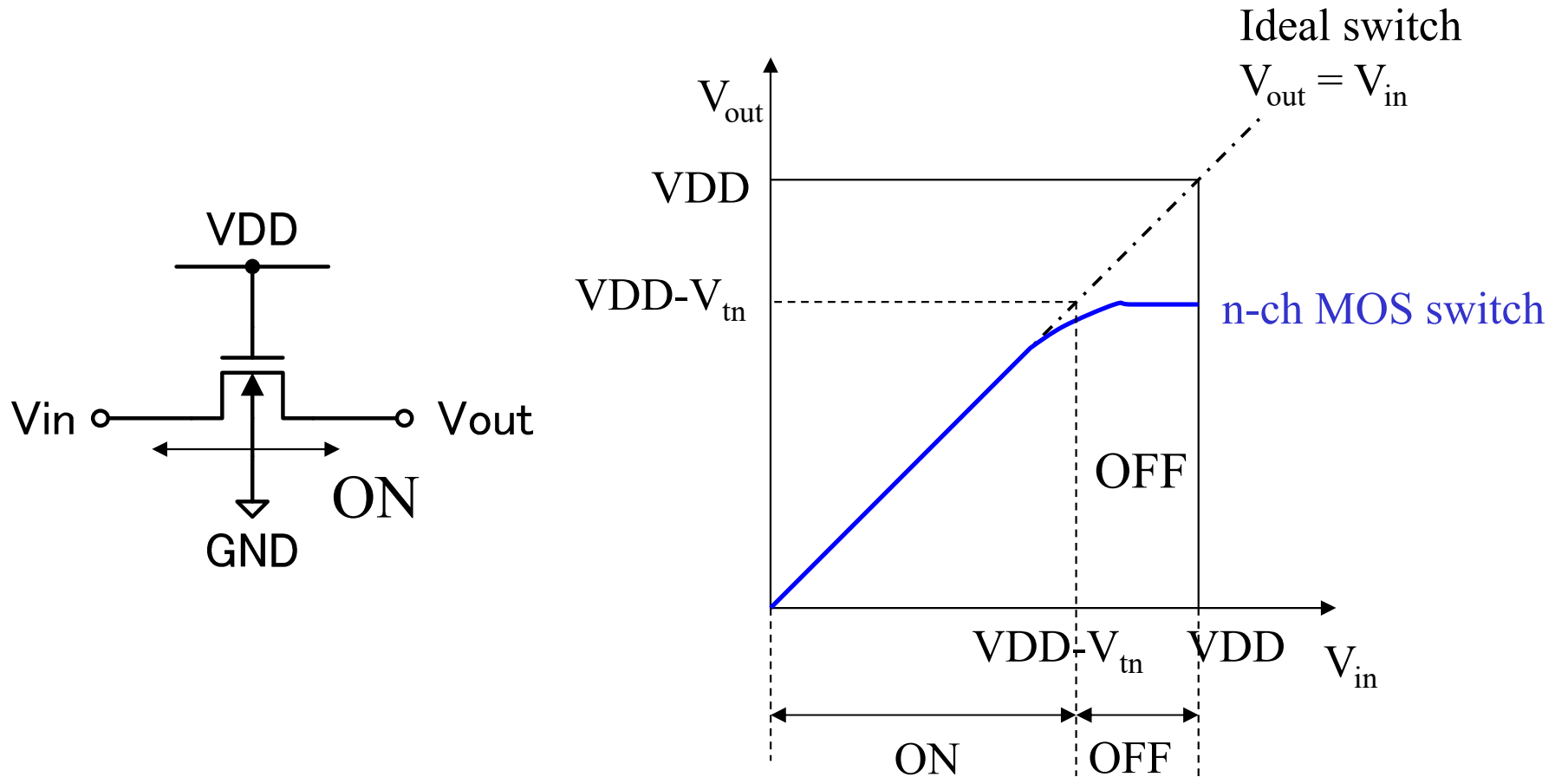


1 stage from ϕ to Y
2 MOSFETs
(4 MOSFETs including
the inverter)



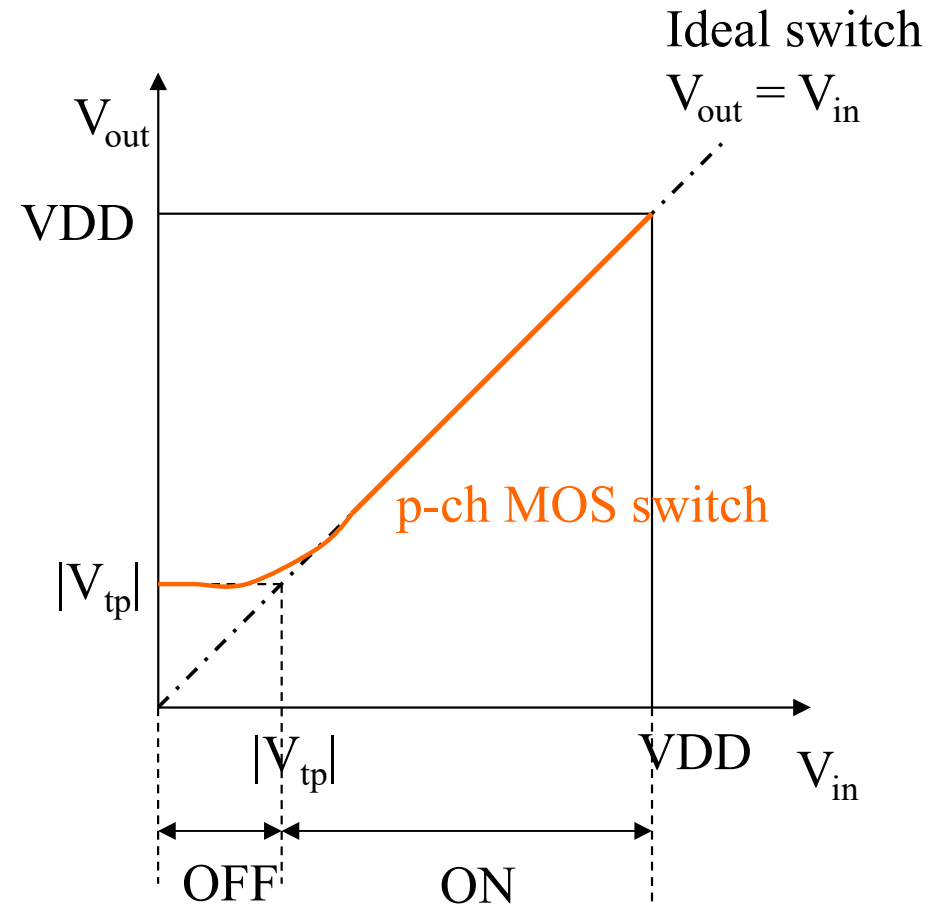
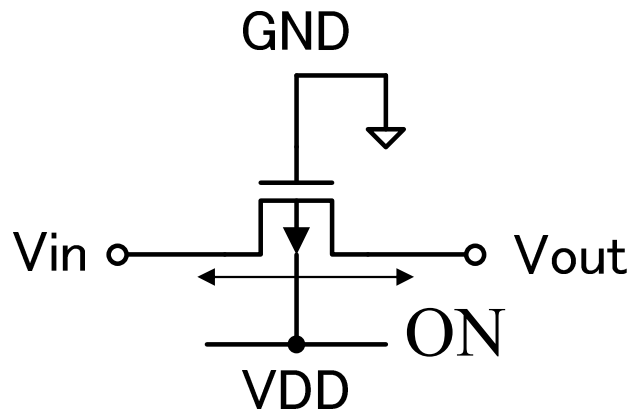
- TG: The cascade connection should be avoided. (The logic swing get decreased in the process of logic operation.)
- PUN, PDN: The logic swing is kept at the power supply voltage.)

n-ch MOS switch



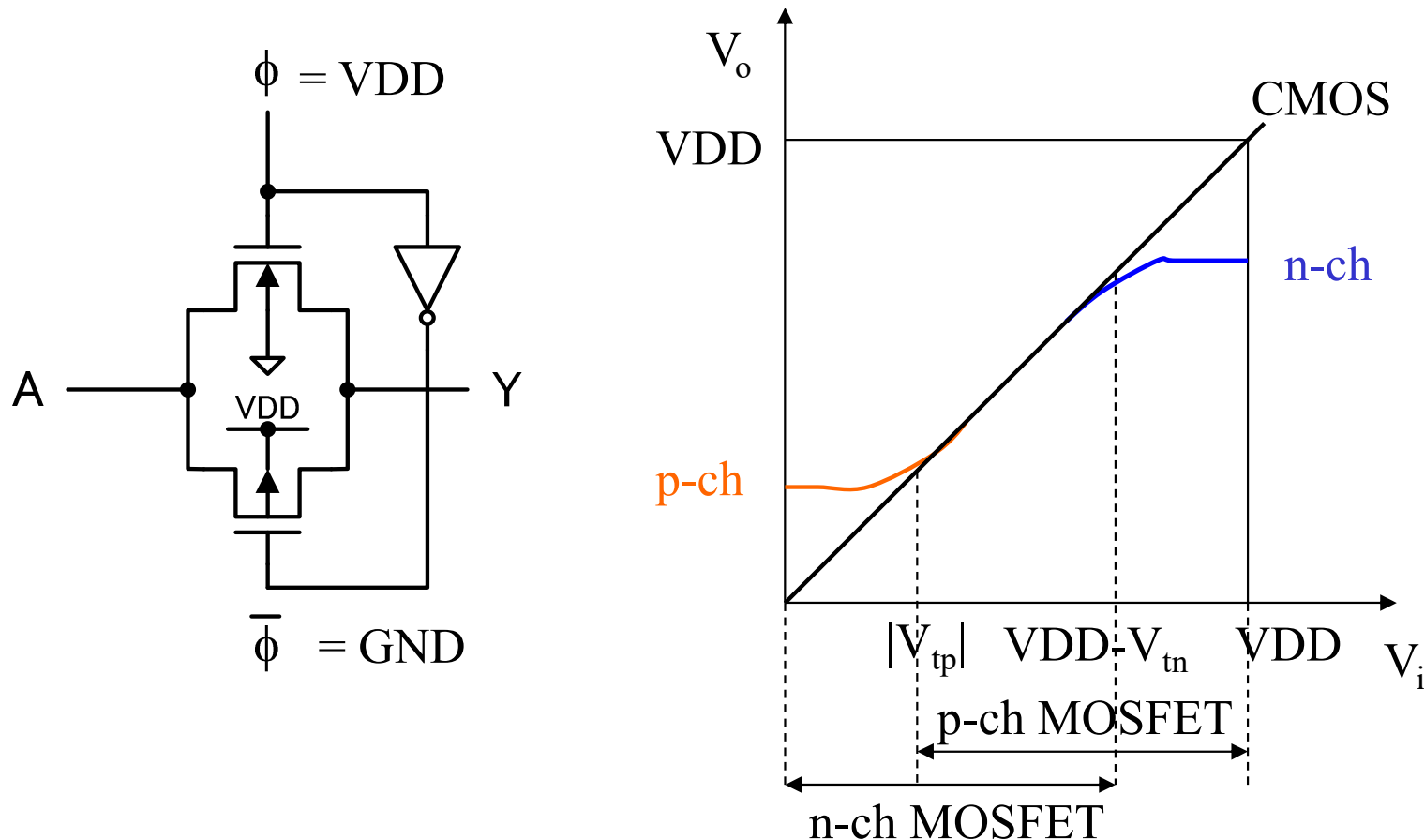
The output swing is limited within a range between 0 and $V_{DD} - V_{tn}$. The V_{tn} is a threshold voltage of n-ch MOSFET (see Chapter 4).

p-ch MOS switch



The output swing is limited within a range between $|V_{tp}|$ and V_{DD} . The V_{tp} is a threshold voltage of p-ch MOSFET (see Chapter 4).

CMOS switch (TG)



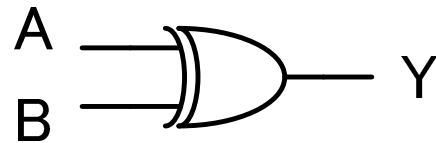
There is no degradation of a logic swing. However, the logic swing is not kept at the power supply voltage, but the output swing depends on the input swing.

2.3.2 Exclusive OR (EXOR)

Disjunctive canonical form of EXOR

* Disjunctive canonical: 加法標準形

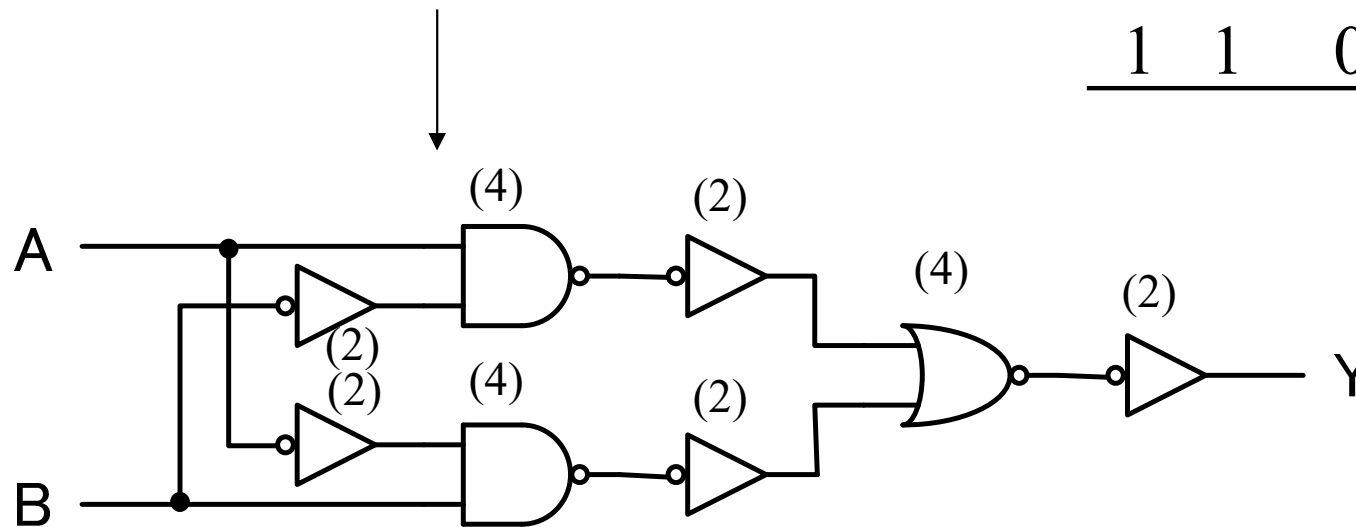
Symbol



Truth table

A	B	Y	← Parity
0	0	0	
0	1	1	
1	0	1	
1	1	0	← Difference from OR

$$Y = A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$$



22 MOSFETs, 5 stages

Optimization of EXOR

$$Y = A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$$

$$= \bar{A} \cdot B + \bar{A} \cdot A + \bar{B} \cdot B + A \cdot \bar{B} \quad (\text{Addition of constant term})$$

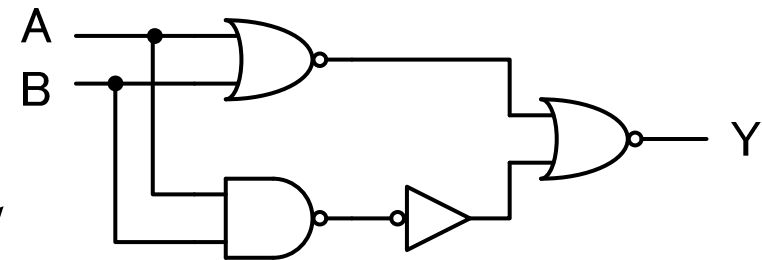
$$= \bar{A} \cdot (A + B) + \bar{B} \cdot (A + B)$$

$$= (A + B) \cdot (\bar{A} + \bar{B})$$

$$= \overline{\overline{A + B + \bar{A} + \bar{B}}}$$

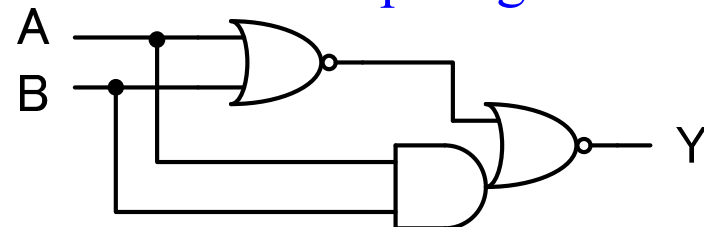
$$= \overline{A + B + A \cdot B}$$

De Morgan theorem



14 MOSFETs, 3 stages

Replacement with
complex gate



10 MOSFETs, 2 stages

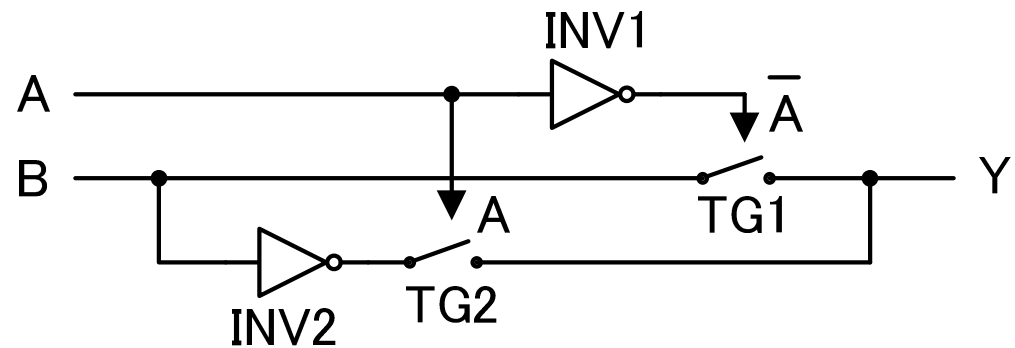
10

EXOR circuit with TG

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

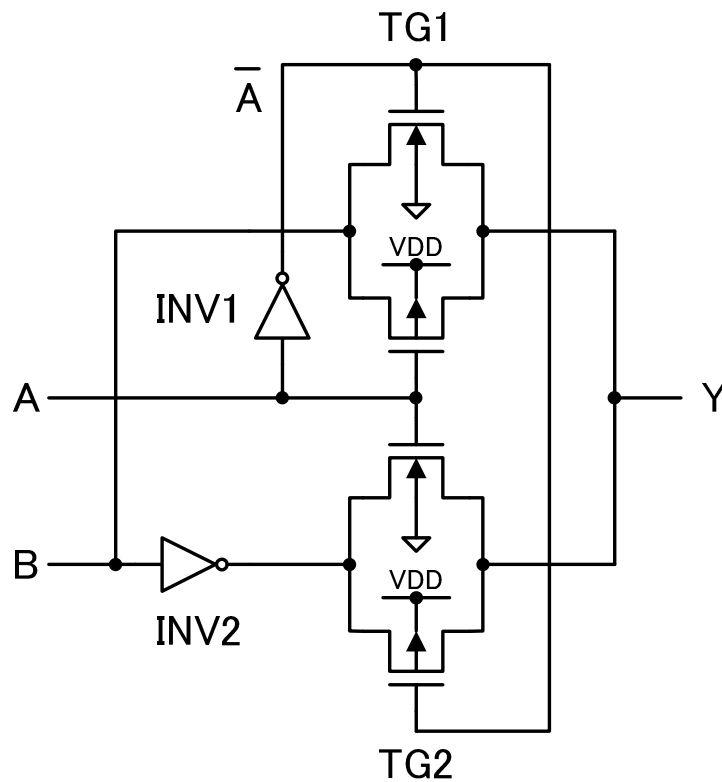
⇒ $\left\{ \begin{array}{l} \text{if } (A==0) \quad Y=B \\ \text{if } (A==1) \quad Y=\bar{B} \end{array} \right.$



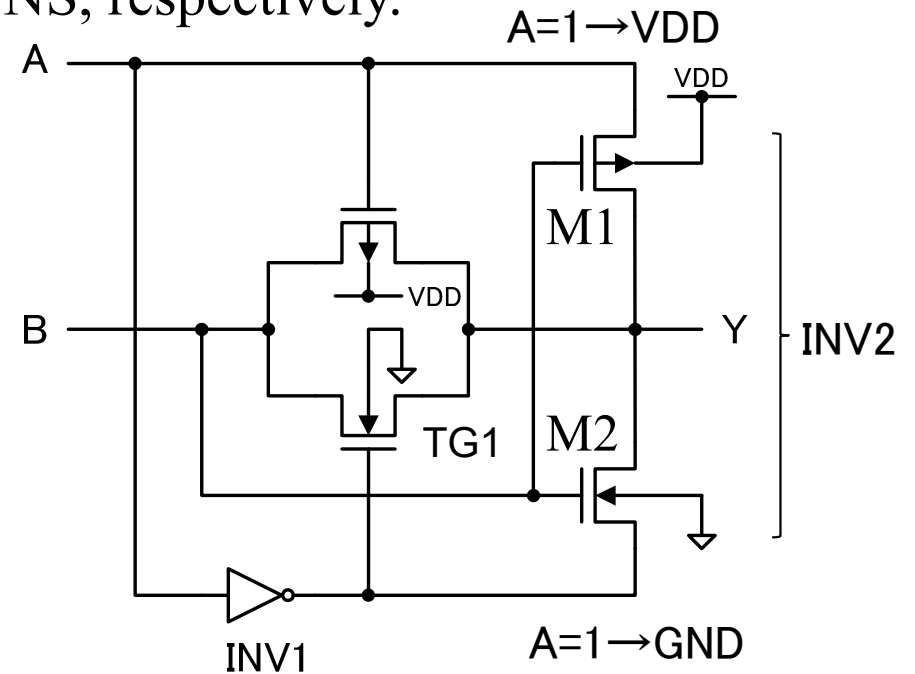
Optimization of EXOR with TG

The switch is replaced with TG.

The TG2 can be removed, because the INV2 is invalid when $A = 0$. The voltage of A applied to the drain of M1 for supplying power to INV2. However, remember that the body of M1 and M2 are connected to VDD and GNS, respectively.



8 MOSFETs, 2 stages

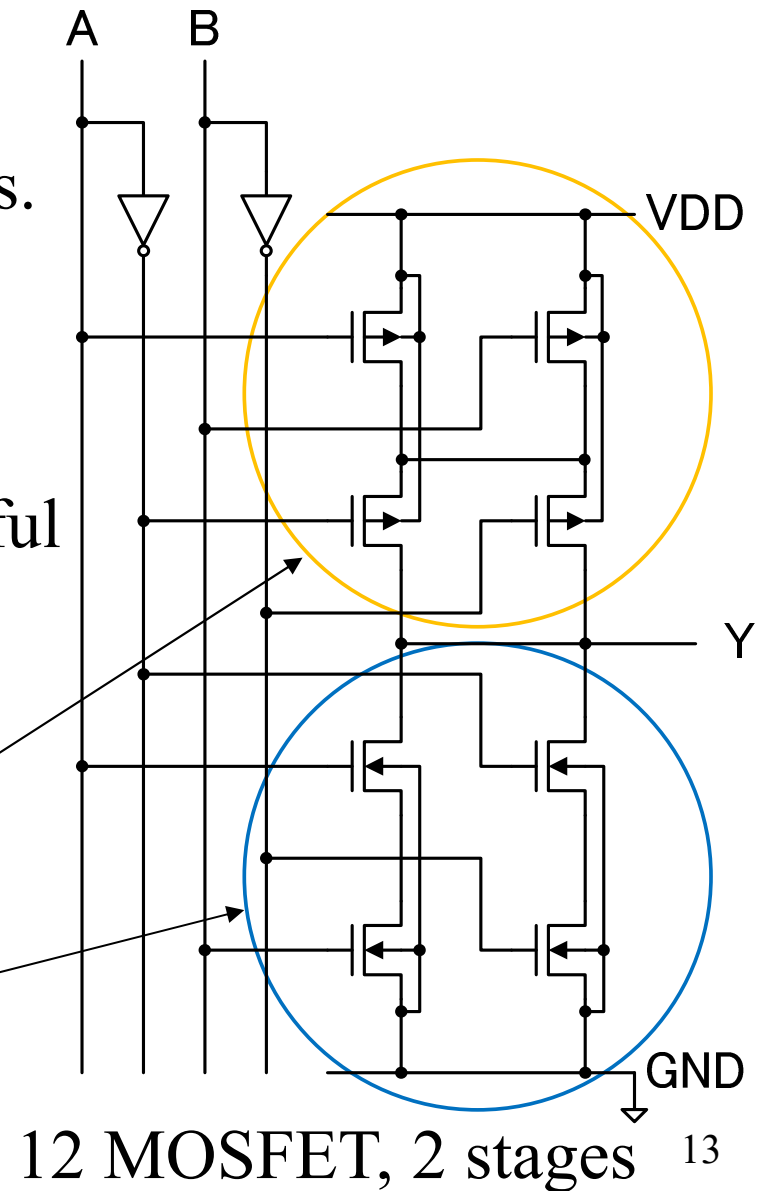


6 MOSFETs, 2 stages

EXOR with PUN and PDN

EXOR circuit composed of TG is optimized for the number of MOSFETs. However, this circuit is unsuitable for the cascade connection, because the logic swing of TG is non-recoverable. The EXOR with PUN and PDN is useful for the cascade connection of EXOR.

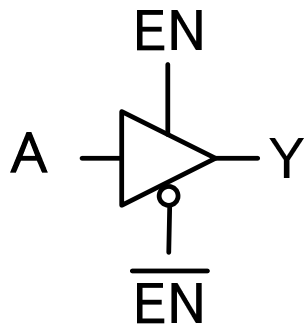
$$\begin{aligned} Y &= A \oplus B = \bar{A} \cdot B + A \cdot \bar{B} \\ &= (A + B) \cdot (\bar{A} + \bar{B}) \\ &= \overline{A \cdot B + \bar{A} \cdot \bar{B}} \end{aligned}$$



2.3.3 Tristate circuits

Function of tristate circuits

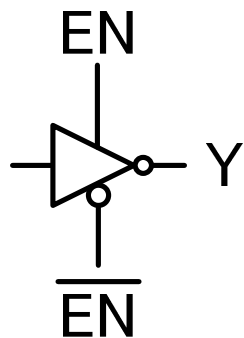
Tristate buffer



EN	A	Y
0	0	high Z
0	1	high Z
1	0	0
1	1	1

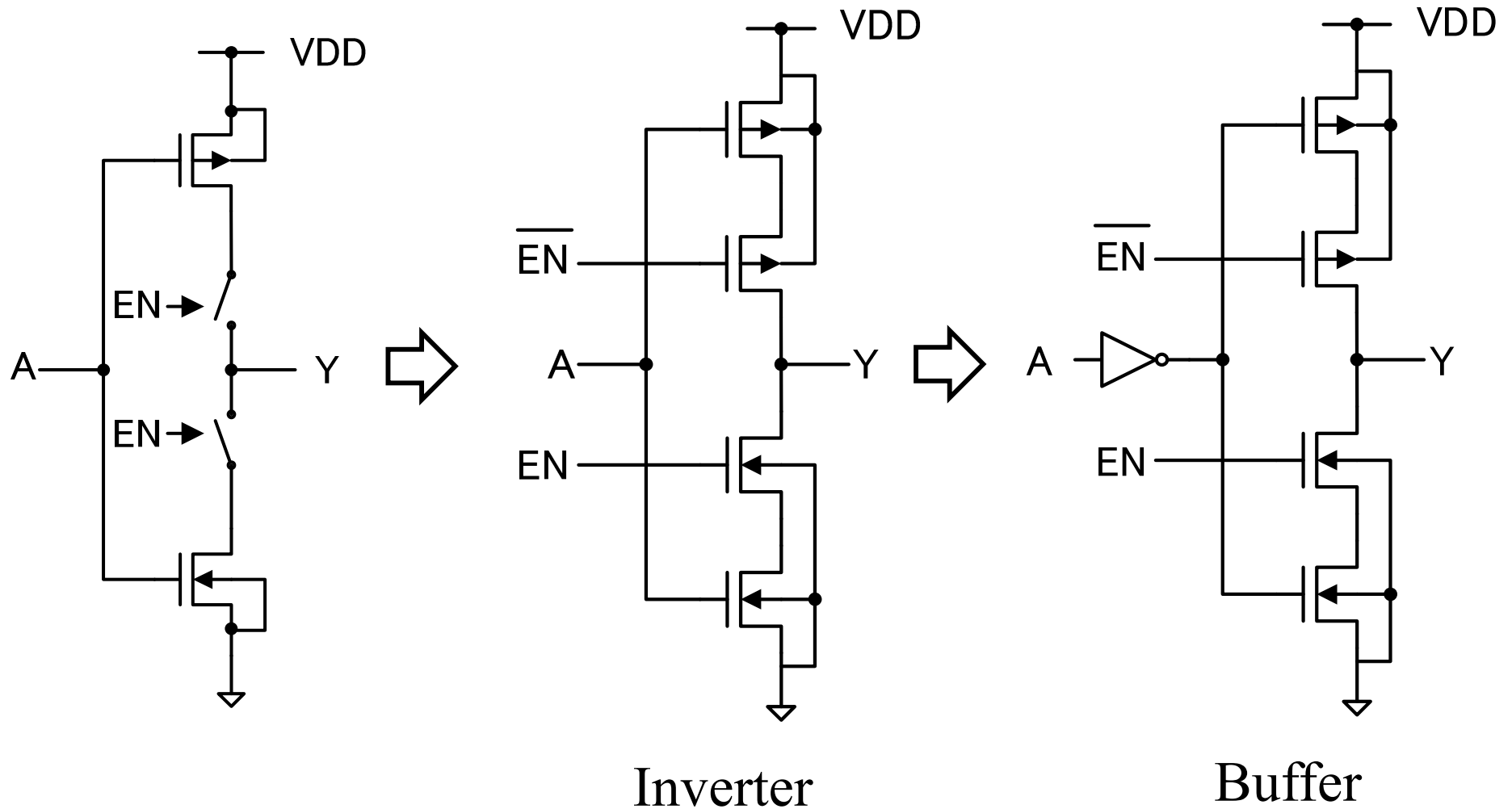
is the same as TG.
($EN \leq \phi$)

Tristate inverter



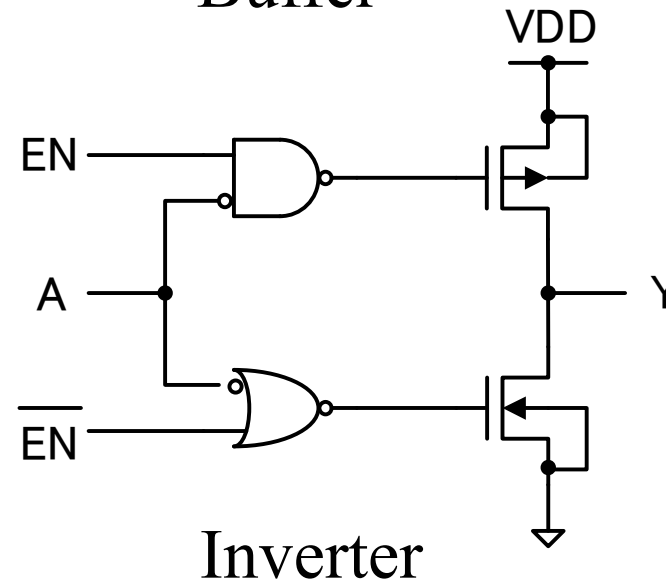
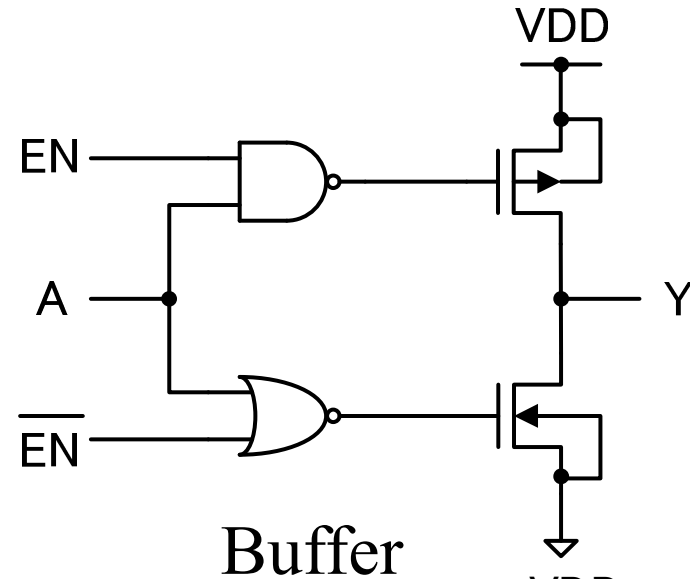
EN	A	Y
0	0	high Z
0	1	high Z
1	0	1
1	1	0

Tristate inverter and tristate buffer



Tristate inverter and tristate buffer 2

EN	A	Y
0	0	high Z
0	1	high Z
1	0	0
1	1	1



2.3.4 Multiplexer (MUX)

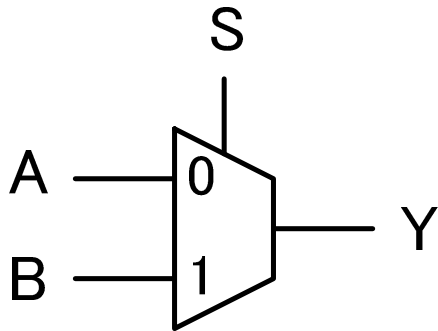
Function of multiplexer (MUX)

An alternative selector

$$Y = \bar{S} \cdot A + S \cdot B$$

$$= \overline{\overline{\bar{S} \cdot A} \cdot \overline{S \cdot B}}$$

De Morgan theorem

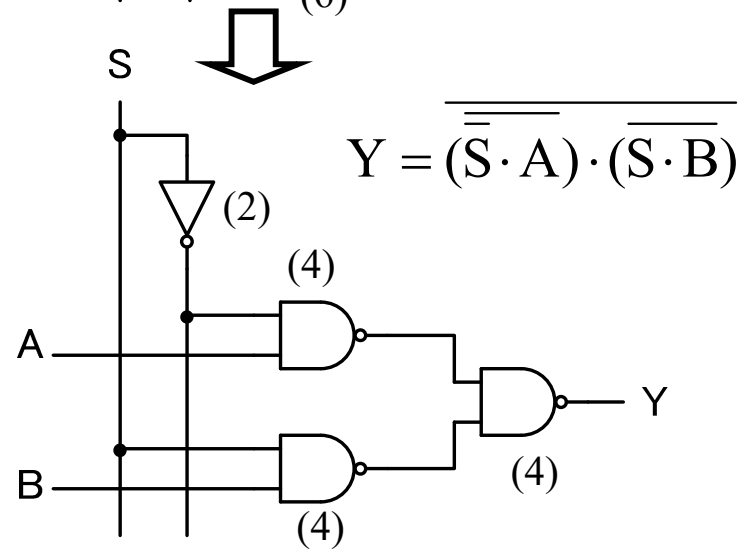
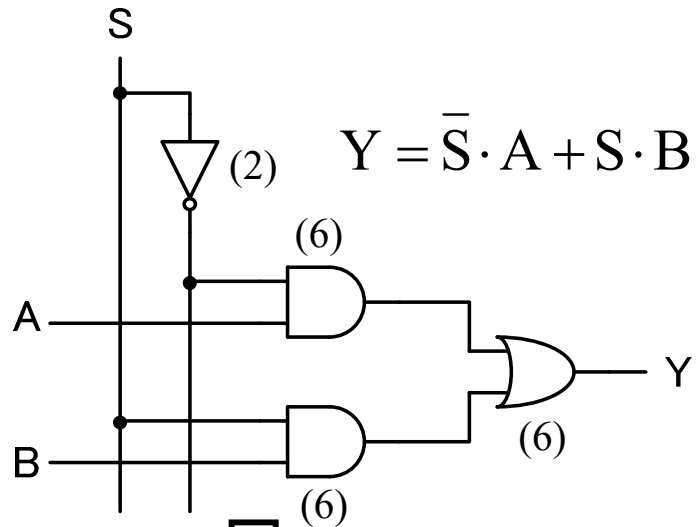


Truth table

S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

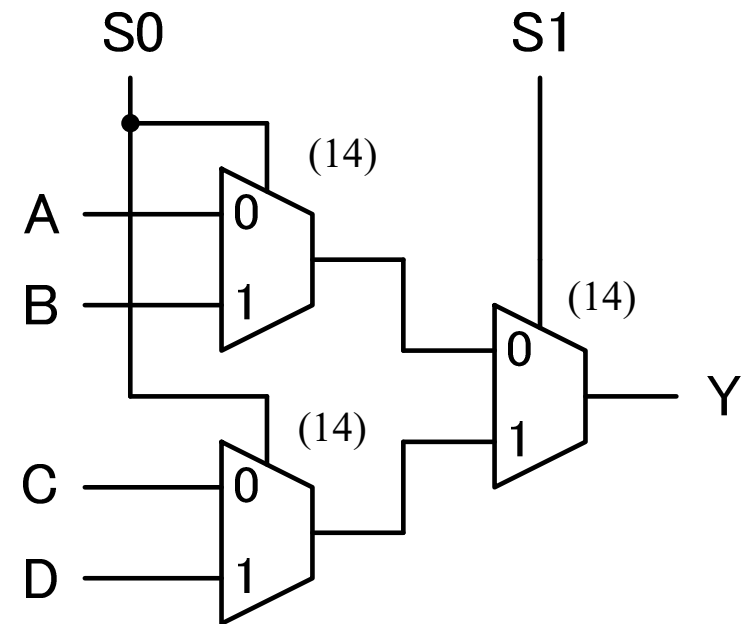
if (S == 0) Y = A;
else Y=B;

MUX using NAND gate



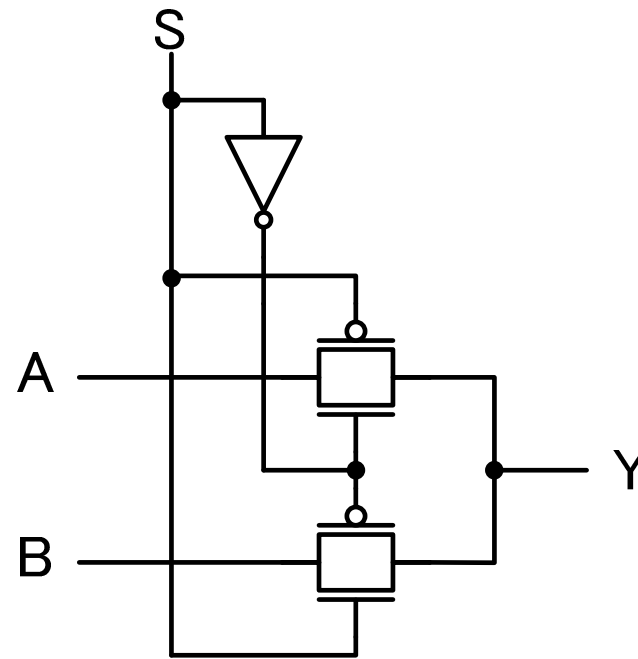
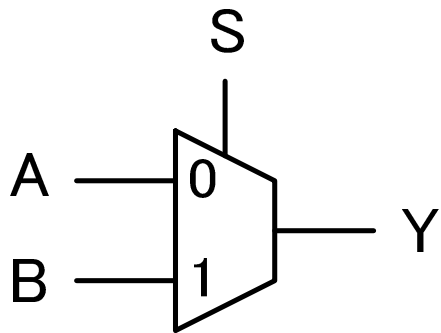
2:1 MUX with 14 MOSFETs

4:1 MUX

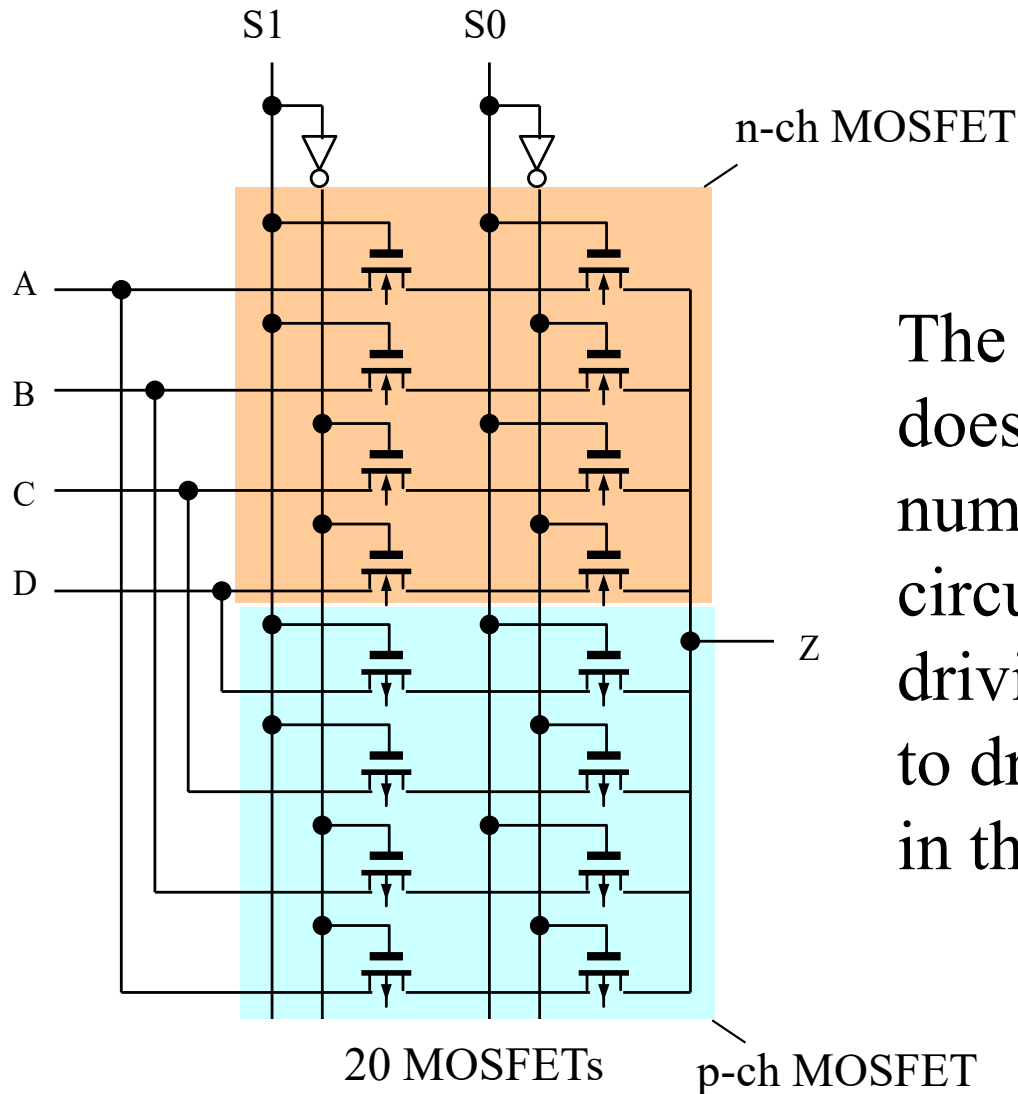


42 MOSFETs

2:1 MUX with TG

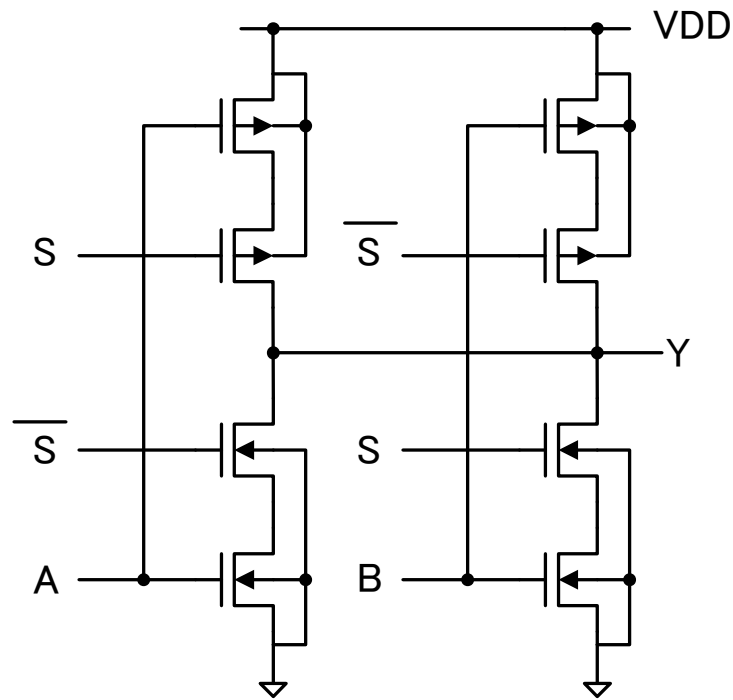
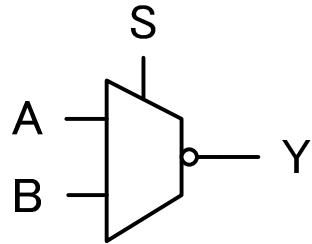


4:1 MUX with TG

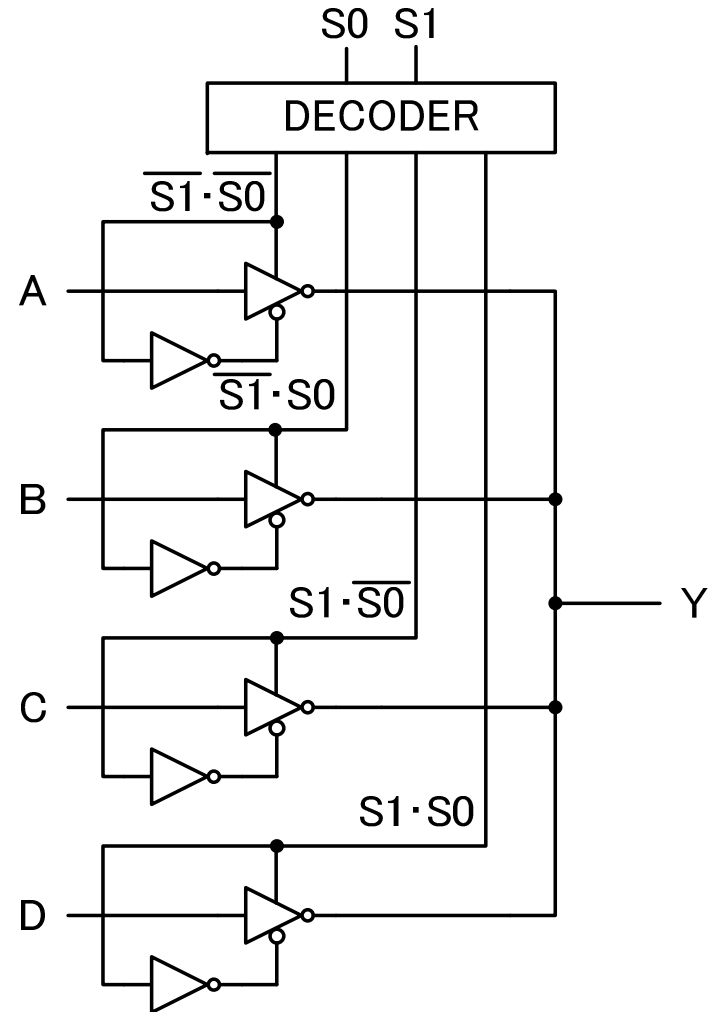


The number of stages does not depend on the number of inputs of this circuit. However, the driving power is required to drive many MOSFETs in the array of TG.

MUX with tristate inverter



2:1 MUX

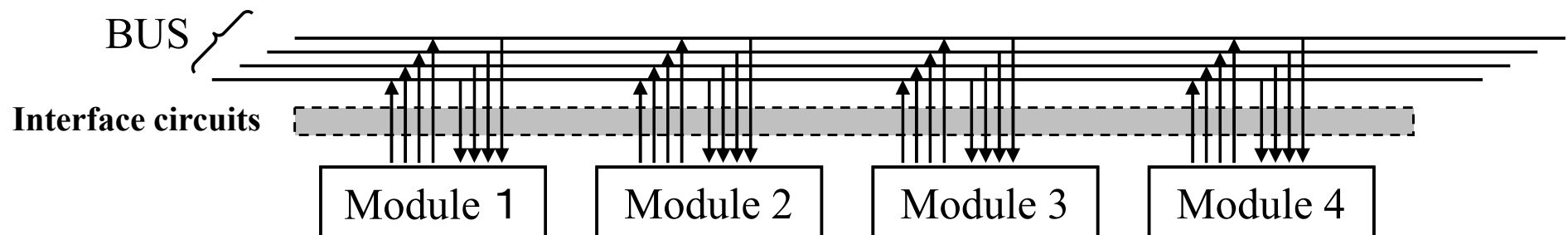


4:1 MUX

2.3.5 BUS control

Advantage and disadvantage of BUS

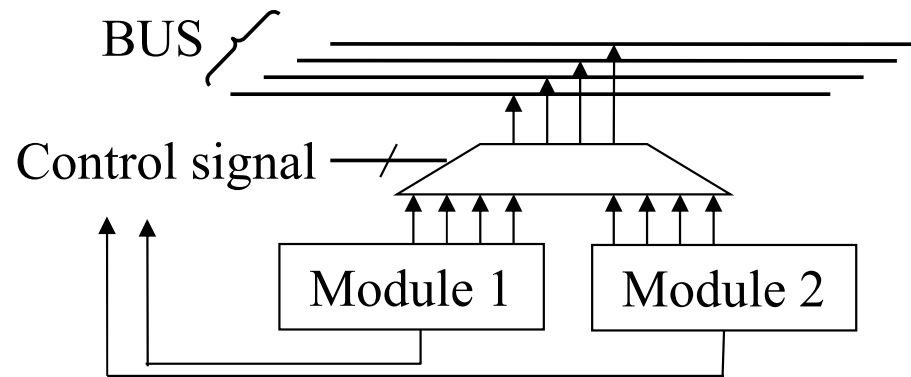
- Advantage
 - A BUS is shared by many circuit modules in LSI to reduce the number of the interconnects.
 - Example: Data BUS, Address BUS
- Disadvantages
 - Additional control circuit to prevent the signal collision
 - Problem of **noise immunity** (ノイズ耐性)
 - Problem of **signal integrity** (信号品質の維持)



Interface circuit for BUS connection

1. MUX

- The output signals from the modules is multiplexed.



2. OR BUS

- The result of OR operation of outputs from all modules is sent to BUS.
- The modules in receiving output a logic value '0'.

3. Tristate buffer

- The modules outputs the tristate value.
- The modules in receiving mode output a logic value 'high Z'.
- The BUS controller is required.