2.4 Latch and flip-flop

Primitive gates of sequential circuits

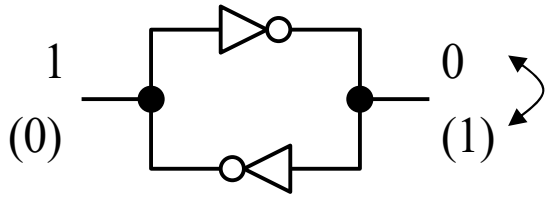
Applications of D-type flip-flop (D-FF)

Register = Parallel connection of D-FFs

Synchronization (同期) = Combinational logic + Register (without feedback)

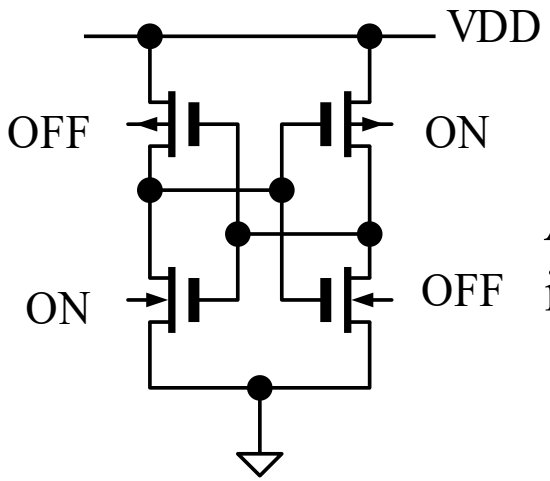
Sequential logic = Combinational logic + Register (with feedback)

D-type latch



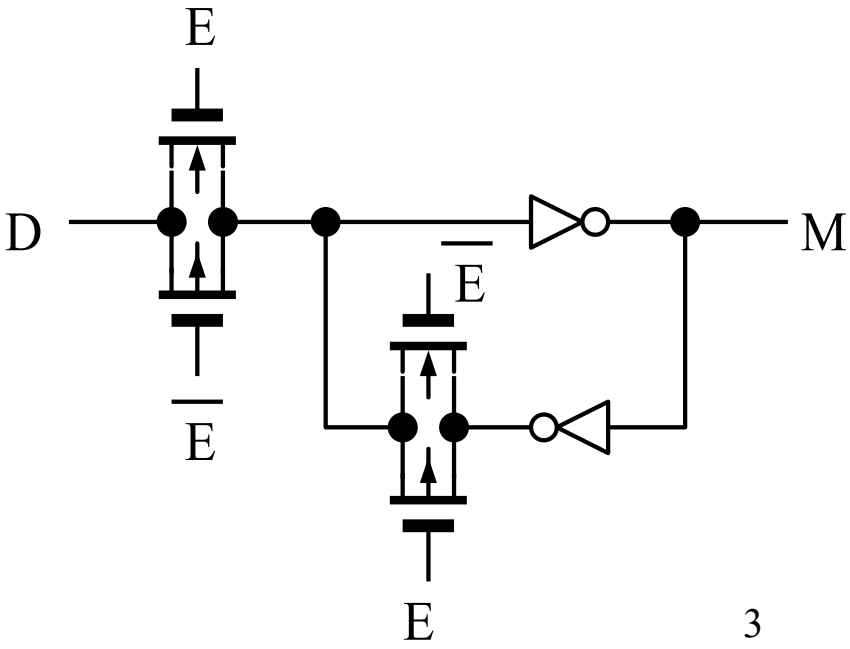
Bistable (双安定)

CMOS

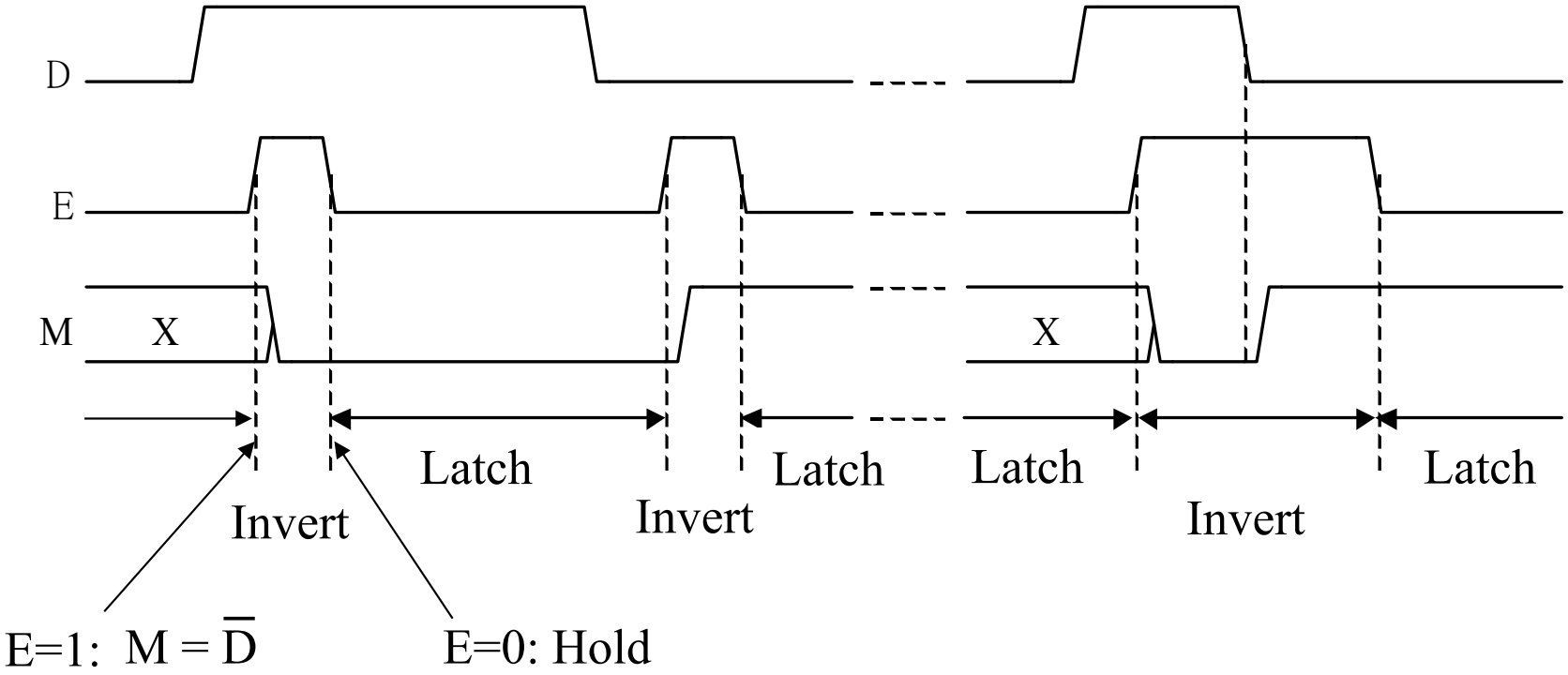


Addition of input switch

D-Latch with enable-input

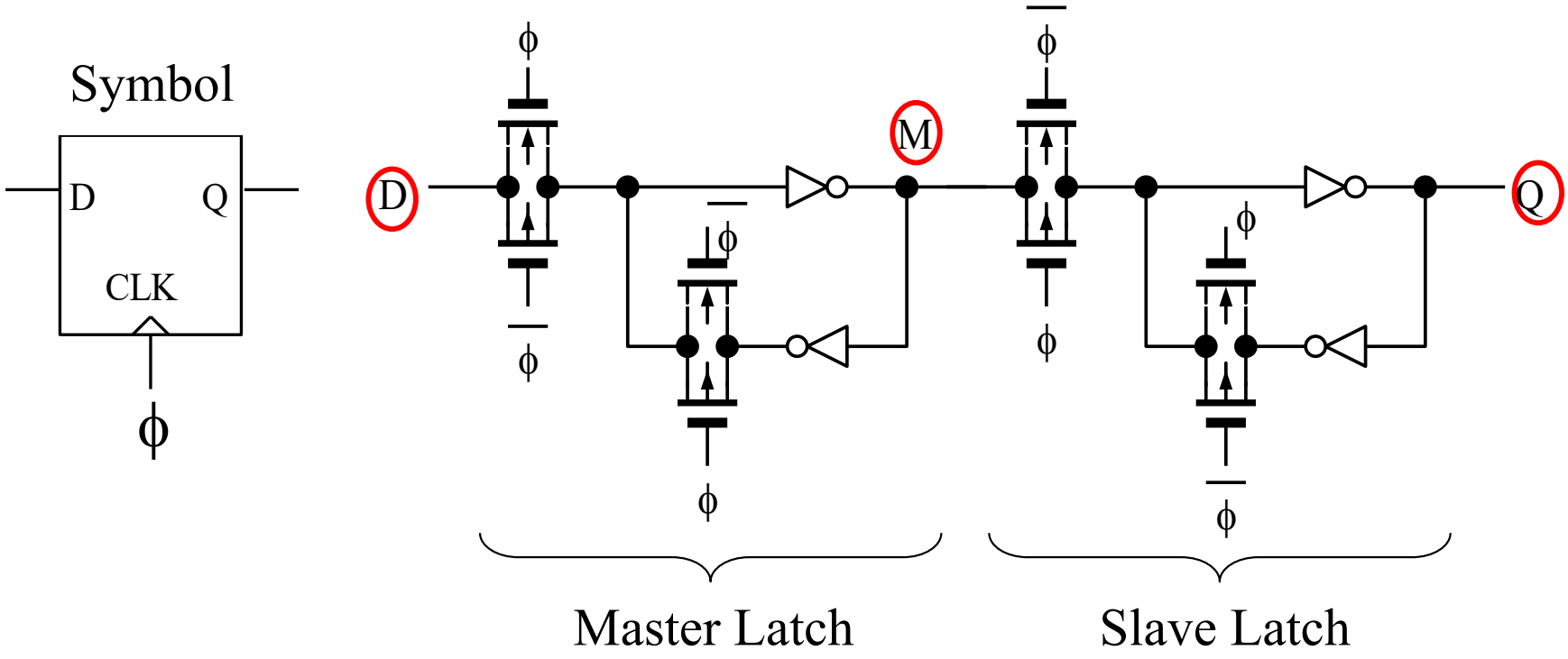


Timing diagram of D-latch



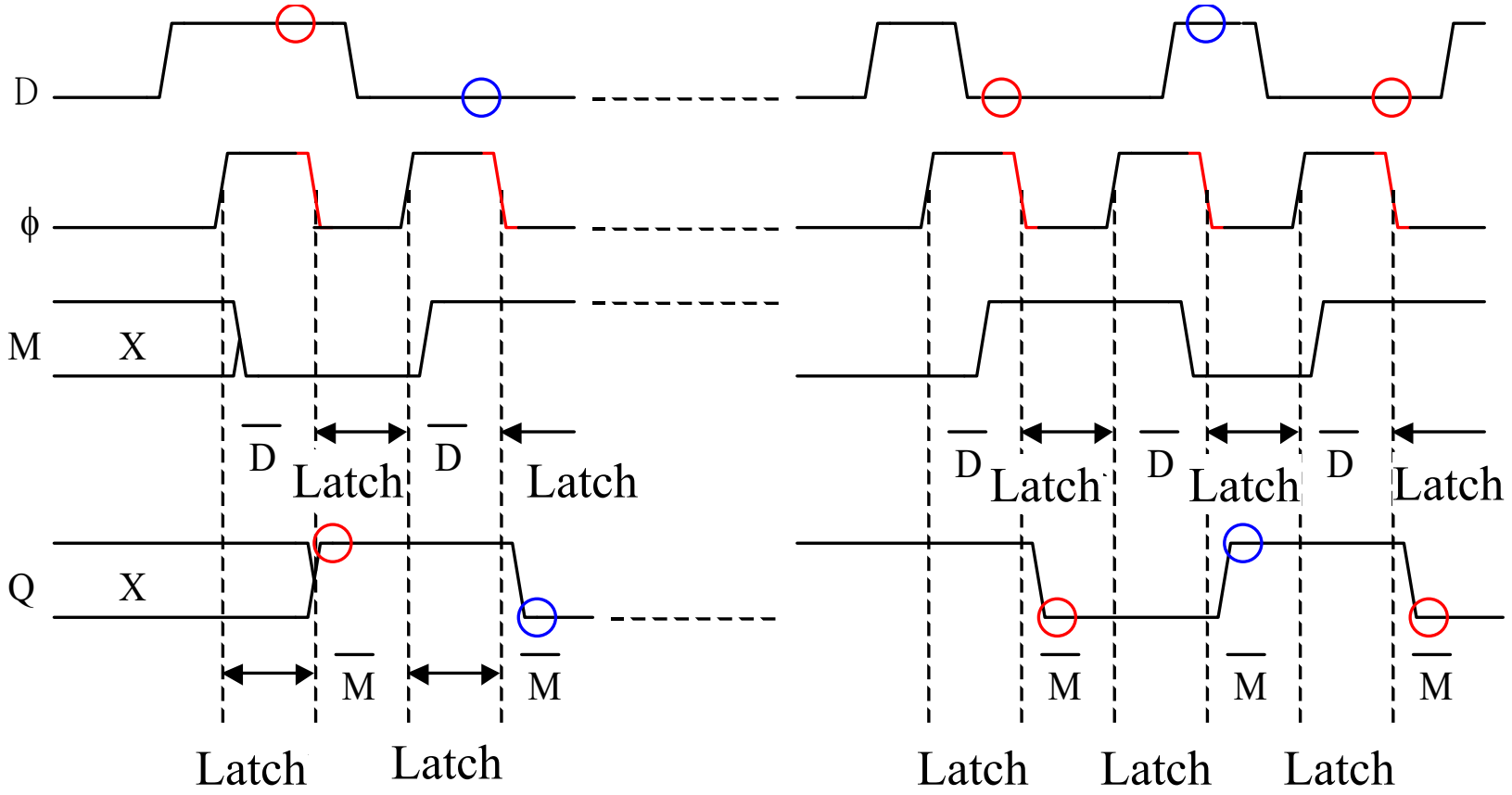
- The input value is latched at the falling edge of E.
- When the clock is input to E, this circuit operates as a level sensitive flip-flop.
  - The input value cannot update during the period of E = 1.

D-type flip-flop (D-FF)



- When the master latch is in the inverter mode, the slave latch hold the logic value of Q and vice versa.
- When the clock is input to ϕ, this circuit operates as an edge sensitive flip-flop.

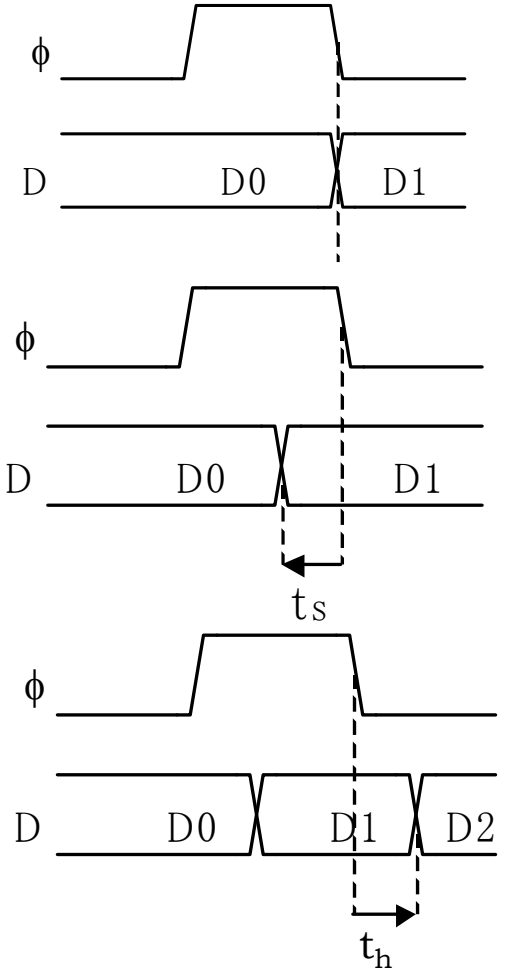
Timing diagram of D-FF



The value of Q is not changed at a timing other than the falling edge of the clock ϕ, because the slave latch hold the output Q, if the value of the input D is changed during ϕ = 1. If you employ the clock $\overline{f}$, the flip-flop updates the output value Q at the rising edge of the clock.

Setup time and hold time

The jitter (timing variation) of the rising edge and the falling edge is observed in the digital signal. Therefor, timing constraints are imposed on the flip-flop.



The prohibited timing

The fluctuation of D at the clock edge causes the unstable state of the positive feedback loop of D-FF (Meta-stable).

Setup time t_s

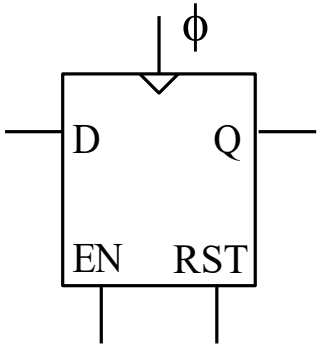
The value of D should arrive the setup time before the clock edge.

Hold time t_h

The value of D should be held the hold time before the clock edge.

D-FF with reset

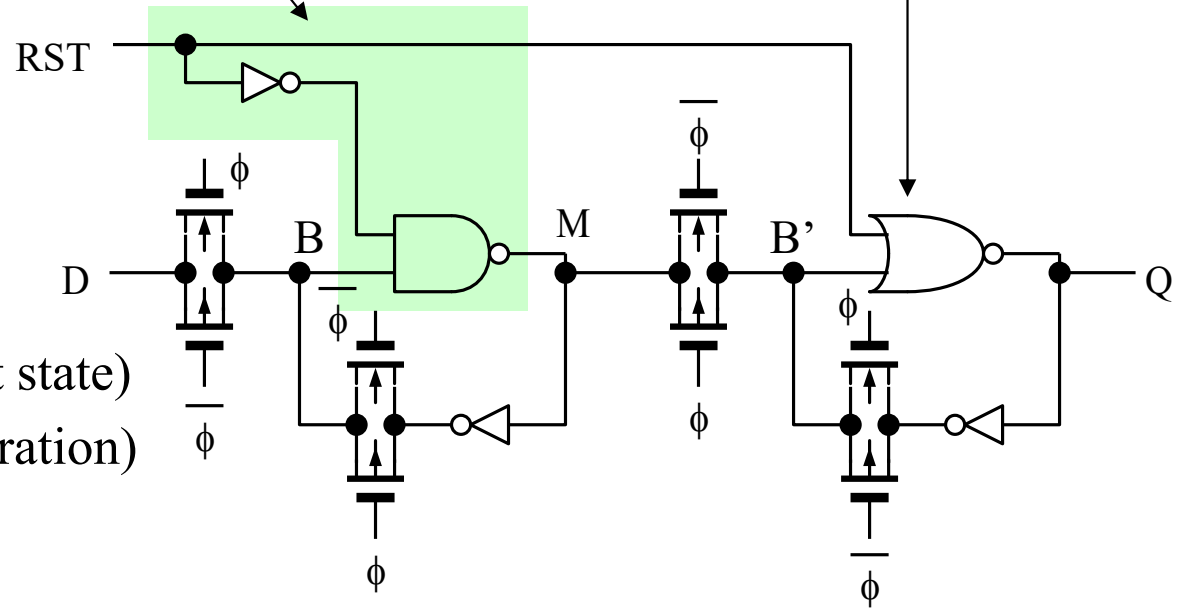
Symbol



Enable Reset

RST	B	M	
0	0	1	$\overline{B}$
0	1	0	
1	0	1	Set
1	1	1	

RST	B'	Q	
0	0	1	$\overline{B}$'
0	1	0	
1	0	0	Reset
1	1	0	



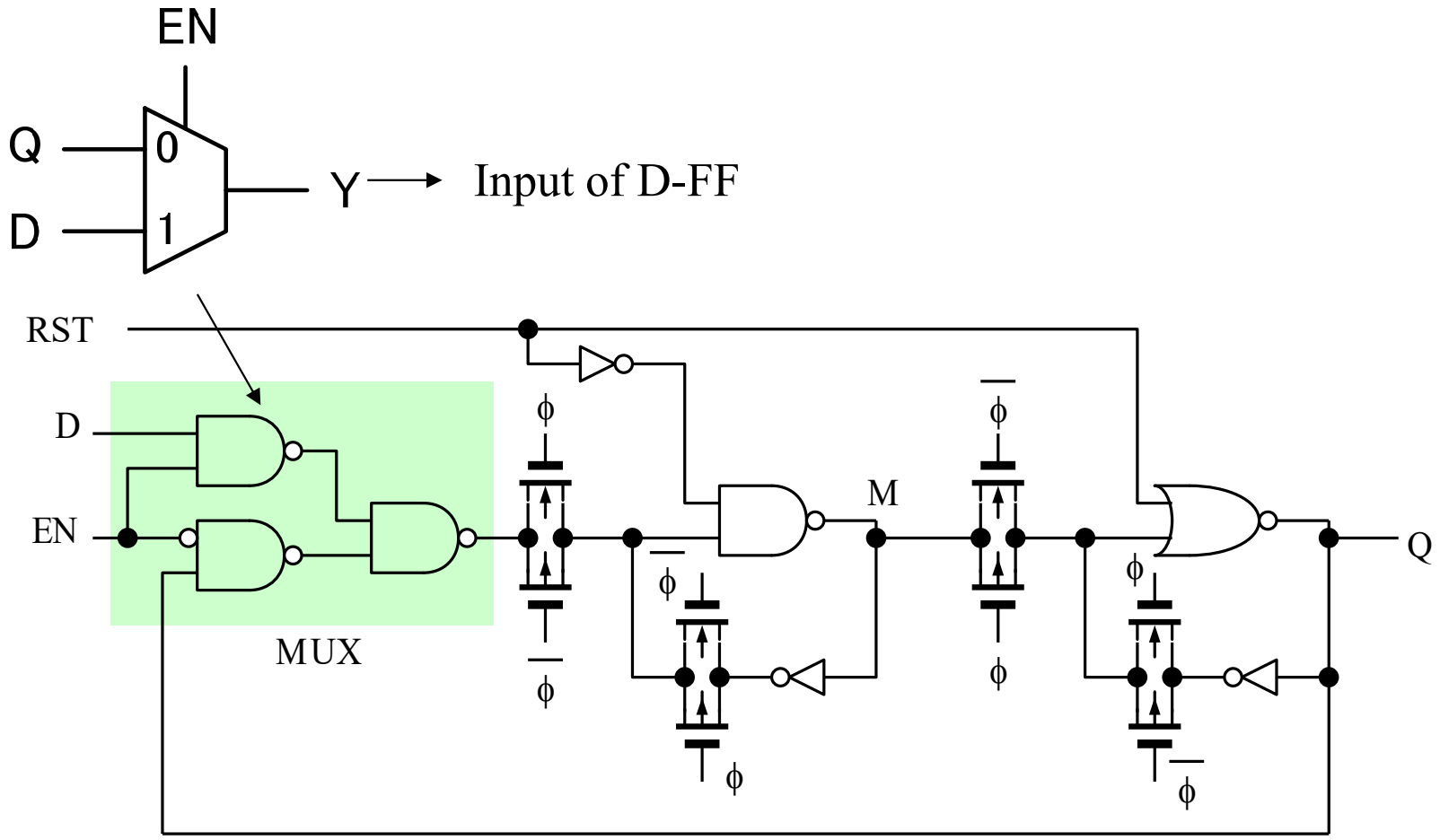
Characteristic table

RST	EN	Q_{n+1}	
0	0	Q_n	(Quiescent state)
0	1	D_n	(D-FF operation)
1	0	Reset	
1	1	Reset	

The term "Reset (RST)" is the same as the term "Clear (CLR)".

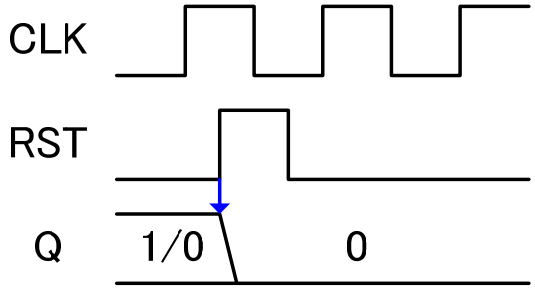
D-FF with Enable

- EN=0: Q is input into D-FF. (The output is fed back to the input of D-FF.)
- EN=1: D is input into D-FF. (The operation is the same as D-FF.)

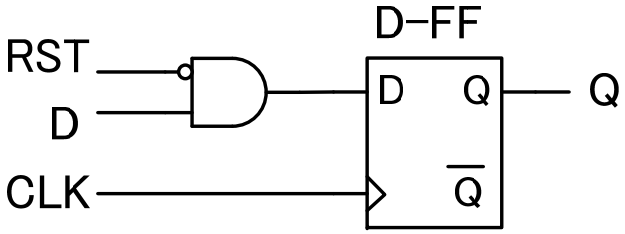


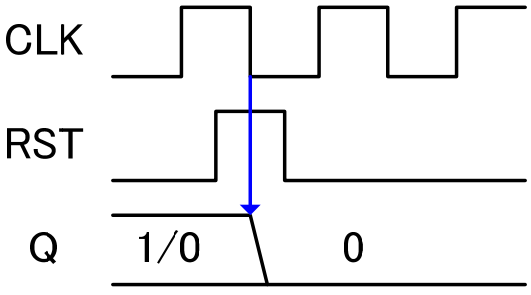
2 types of reset

- Asynchronous reset (非同期リセット) → Circuits shown in slide 8
  - The output value is reset at the rising edge of RST signal.



- Synchronous reset (同期リセット)
  - The output value is reset at the rising edge of clock signal, when the RST signal is asserted.



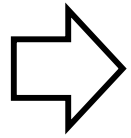


T-FF (Toggle flip-flop)

Other flip-flops can be derived from D-FF.

T-FF

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

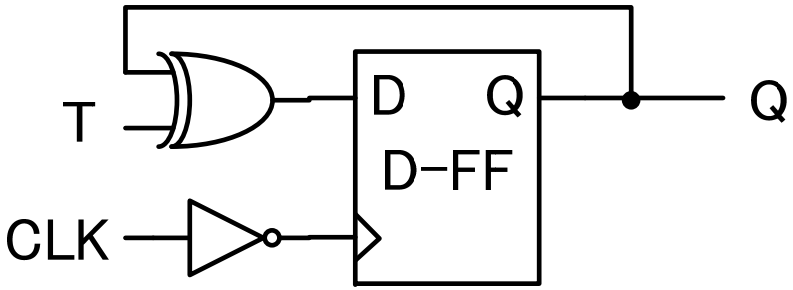


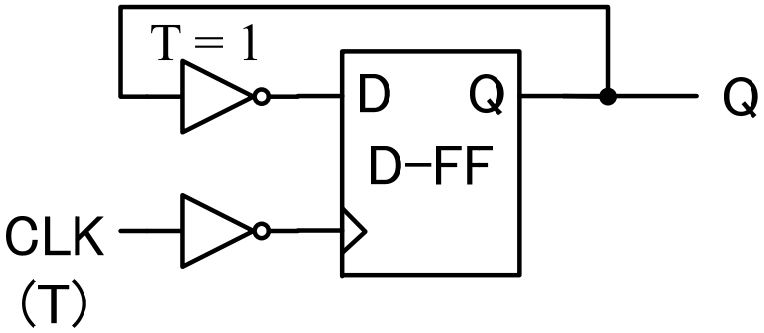
D-FF (Synchronization)

D	Q_{n+1}
0	0
1	1

$$Q_{n+1}=\overline{T}\cdot Q_n+T\cdot\overline{Q_n}=T\oplus Q_n=D$$

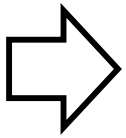
Edge trigger T-FF





JK-FF

JK-FF		
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

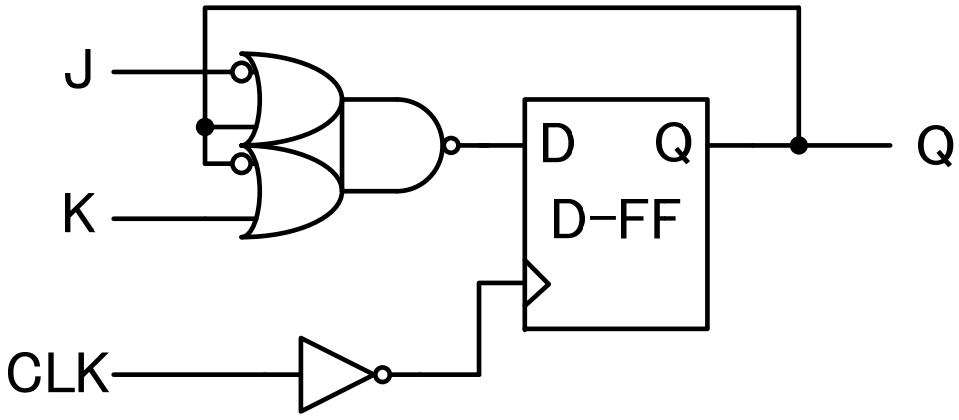


D-FF	
D	Q_{n+1}
0	0
1	1
Synchronization	

$$Q_{n+1}=\bar{J}\cdot\bar{K}\cdot Q_n+J\cdot\bar{K}+J\cdot K\cdot\overline{Q_n}=\bar{J}\cdot\bar{K}\cdot Q_n+J\cdot\bar{K}\cdot(Q_n+\overline{Q_n})+J\cdot K\cdot\overline{Q_n}$$

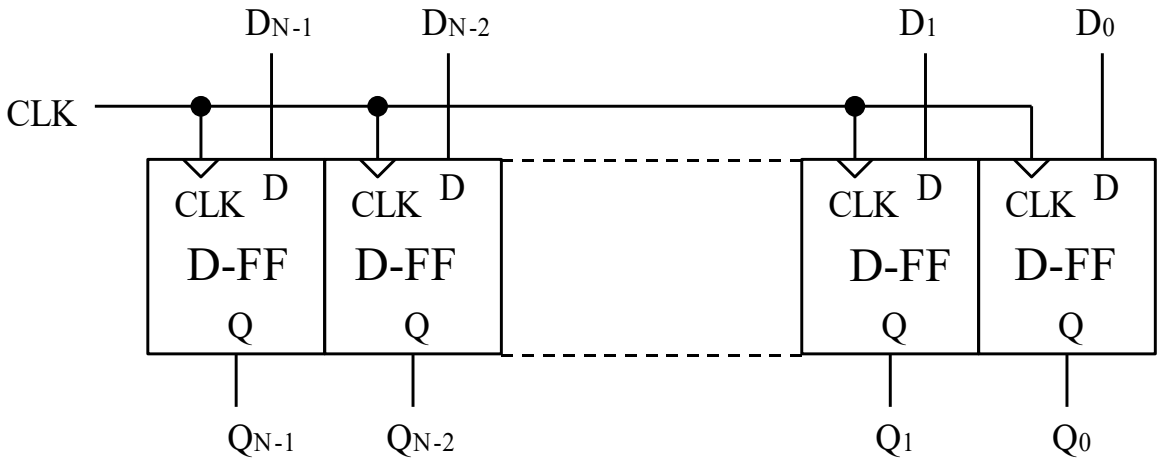
$$=J\cdot\overline{Q_n}+\bar{K}\cdot Q_n=\overline{(\bar{J}+Q_n)\cdot(K+\overline{Q_n})}=D$$

Edge trigger JK-FF



Register

I/O register
Pipeline register
Instruction register
Address register
…



N bit Register