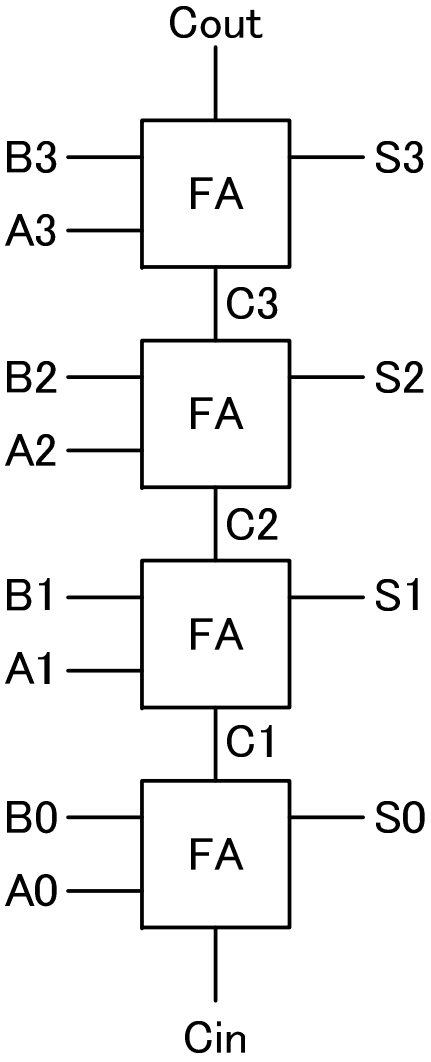
3.2 Combinational logic

Components of microprocessors

3.2.1 Adder and subtractor

Ripple Carry Adder (RCA)



Truth table of full adder (FA)

A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

A+B+Cin

Add

Full Adder

Truth table

A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

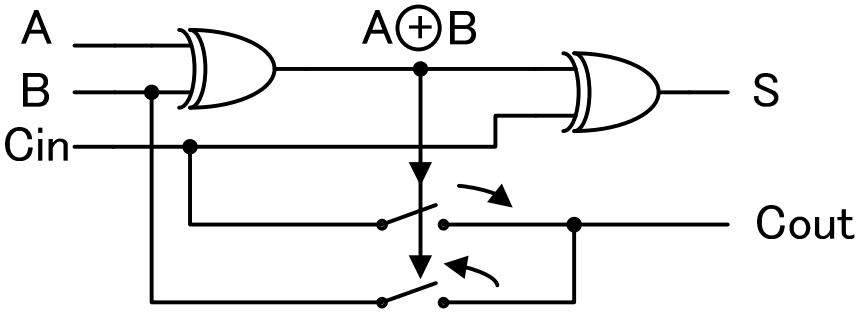
$\overline{A \oplus B}$: A = B; Cout = B

$A \oplus B$: A ≠ B; Cout = Cin

If (A xor B) Cout = Cin;
else Cout = B;

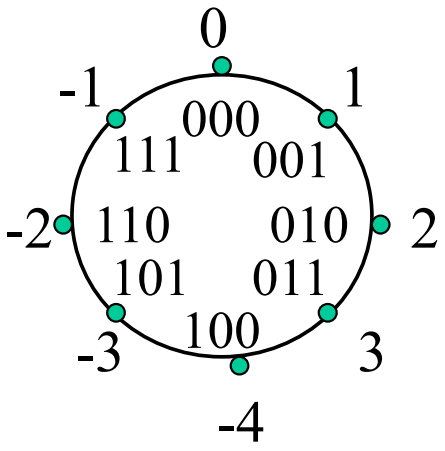
A+B+Cin = Odd number
(Add)

Logic



Subtractor

$$F = A - B = A + (-B)$$

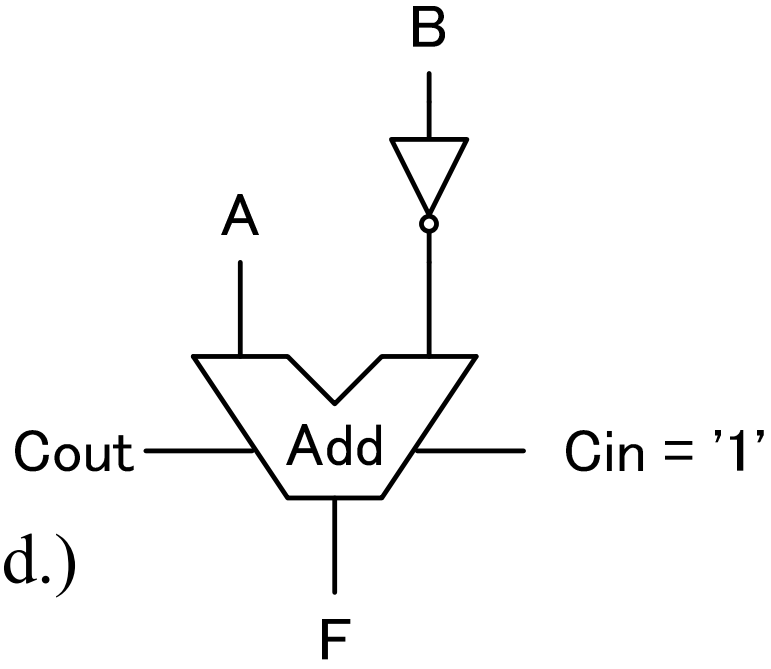


3bit two's complement

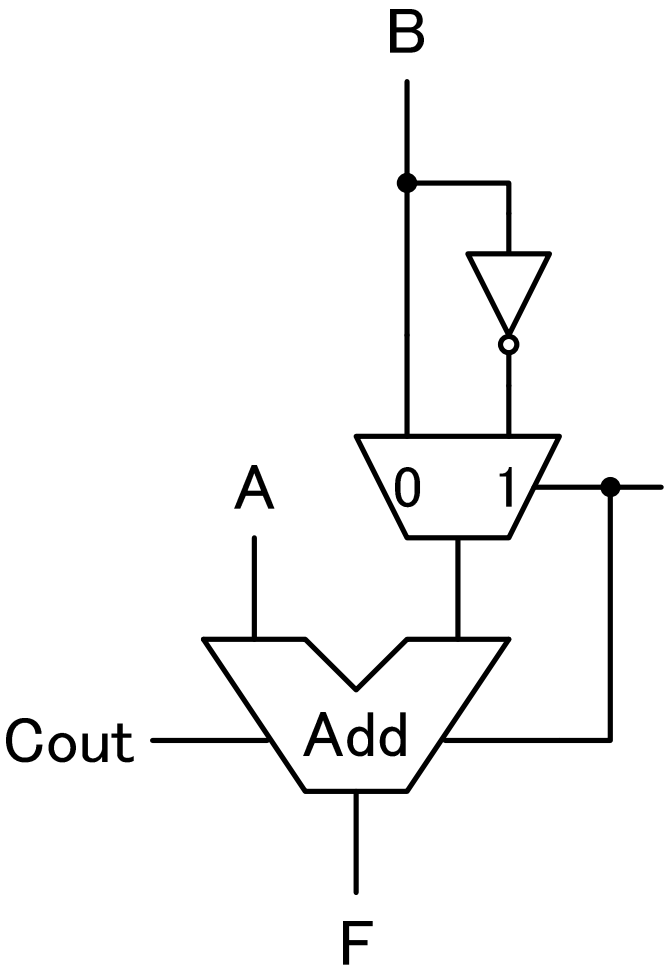
Complement on two

1. Bit-wise inversion
2. Addition of 1

(A carry input is used.)



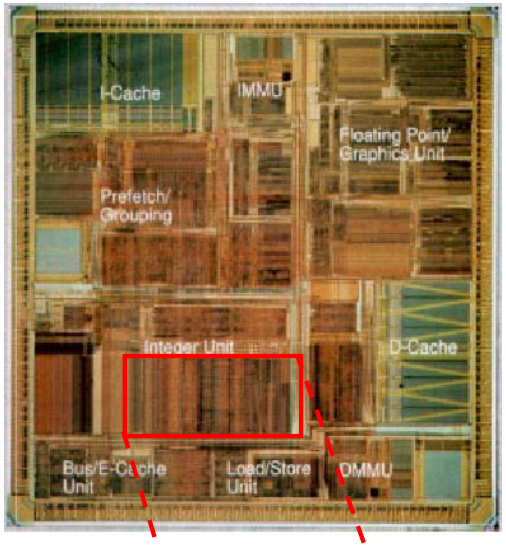
Adder-subtractor

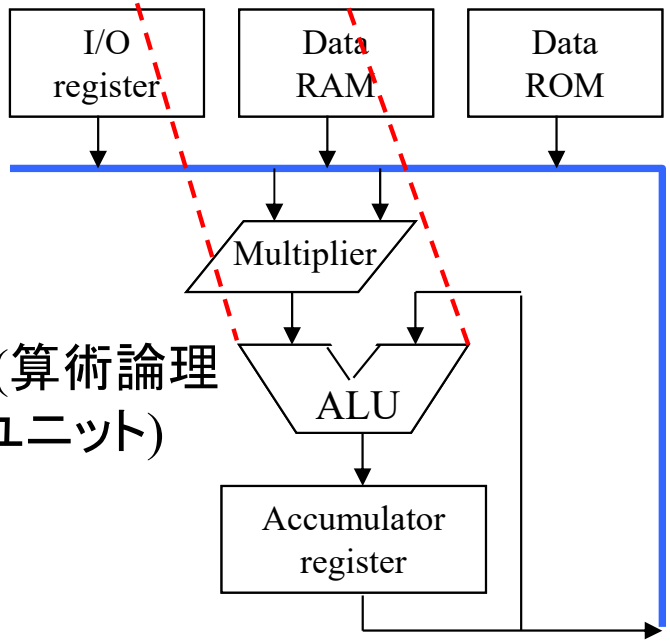


I	F
0	A + B
1	A - B

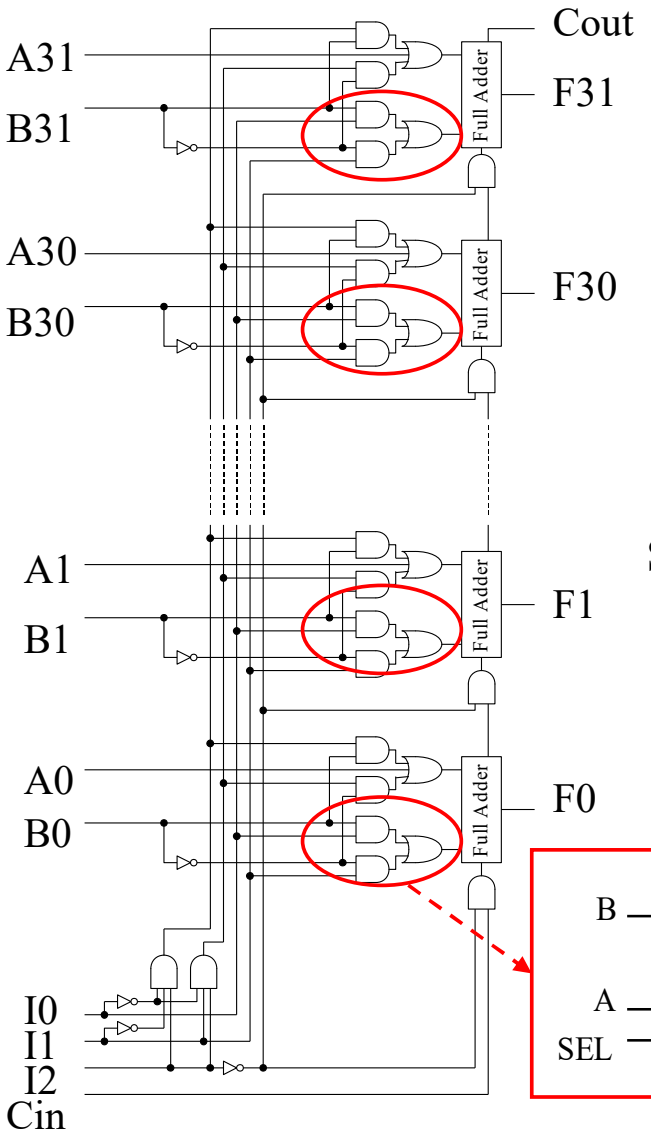
Arithmetic logic unit (ALU)

SUN SPARC





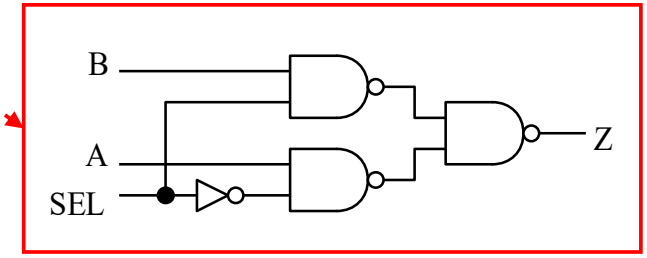
ALU (算術論理演算ユニット)



32bit ALU

Subtraction instruction

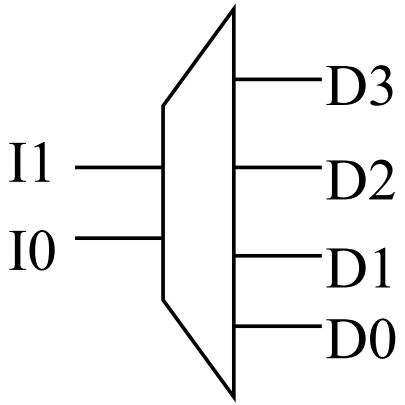
I0	1
I1	0
I2	0
Cin	1



MUX

3.2.2 Decoder

Function of binary decoder



A 1-of-N binary decoder asserts one of its n output bits for every integer input value. There are some types of decoder, for example, a BCD to decimal decoder, demultiplexer and code translators.

Truth table of 2 oto4 line decoder

I1	I0	Line	D3	D2	D1	D0
0	0	D0	0	0	0	1
0	1	D1	0	0	1	0
1	0	D2	0	1	0	0
1	1	D3	1	0	0	0

Disjunctive canonical form

$$\begin{cases} D0 = \overline{I1} \cdot \overline{I0} \\ D1 = \overline{I1} \cdot I0 \\ D2 = I1 \cdot \overline{I0} \\ D3 = I1 \cdot I0 \end{cases}$$

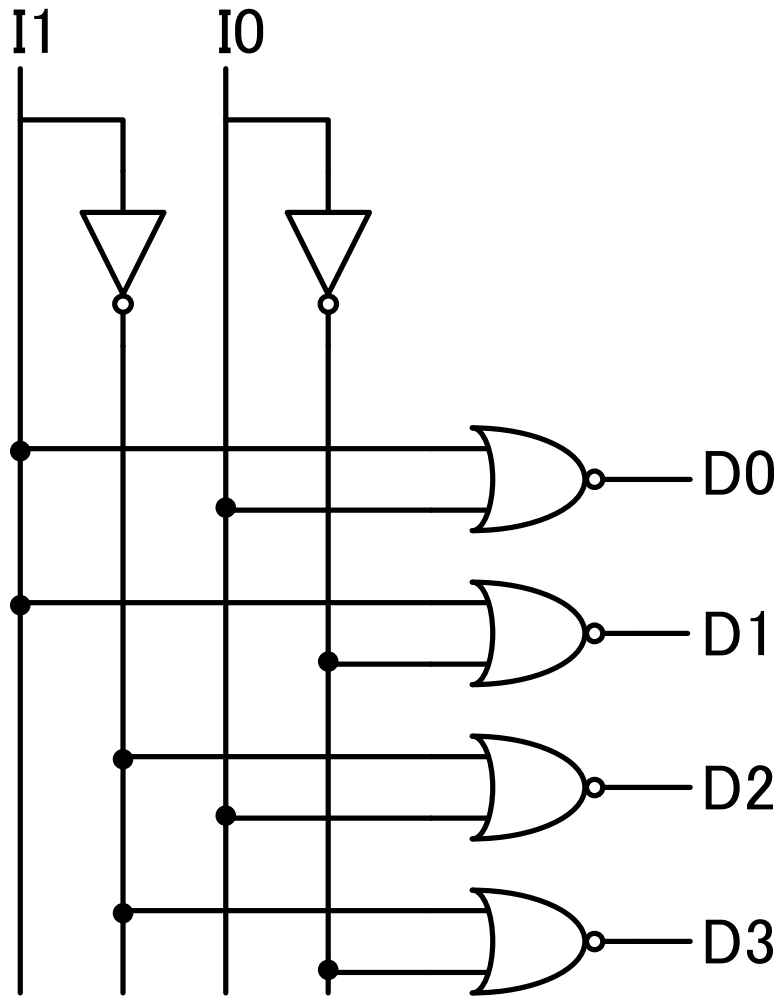
Circuit of decoder

$D0=\overline{I1}\cdot\overline{I0}=\overline{I1+I0}$

$D1=\overline{I1}\cdot I0=\overline{I1+\overline{I0}}$

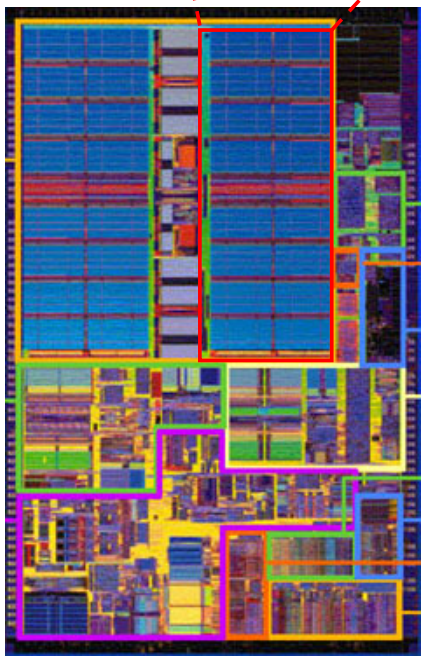
$D2=I1\cdot\overline{I0}=\overline{\overline{I1}+I0}$

$D3=I1\cdot I0=\overline{\overline{I1}+\overline{I0}}$

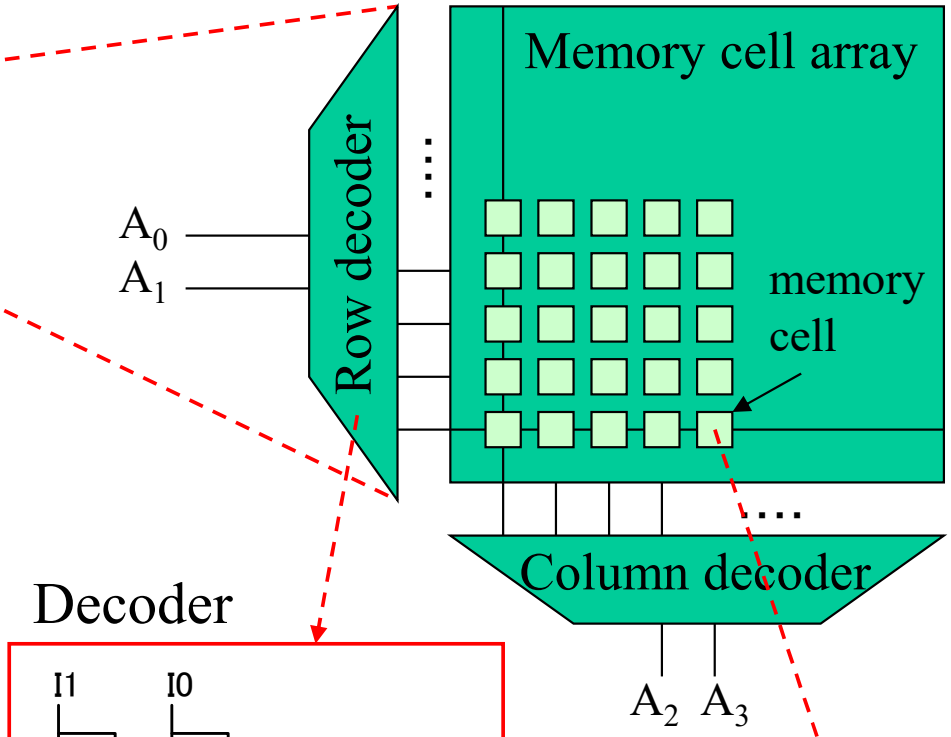


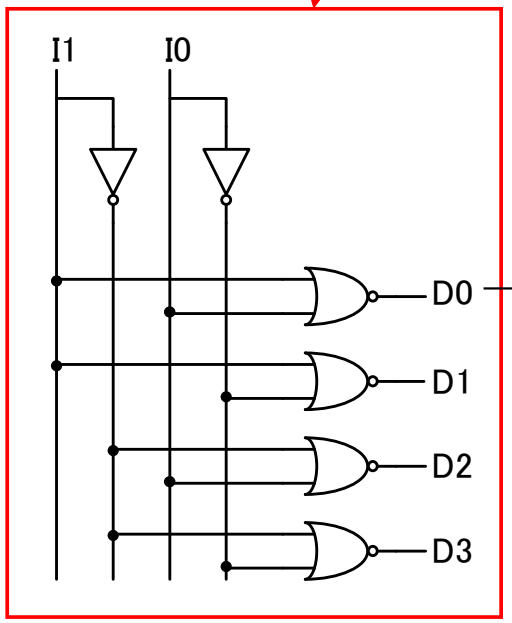
Usage example of decoder

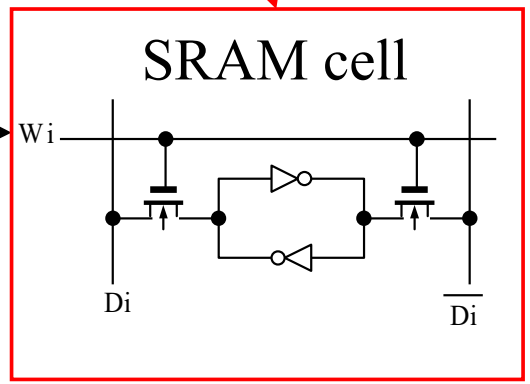
Cache Memory



Intel Mobile Pentium III







3.2.3 Shifter

Uses of shifter

- Shift operation
  - Constant multiplication (= Shift and addition), floating-point arithmetic

    Example: $a * b = a * (b_n \cdot 2^n + b_{n-1} \cdot 2^{n-1} + \cdots + b_0 \cdot 2^0)$

    $= b_n \cdot (a<<n) + b_{n-1} \cdot (a<<n-1) + \cdots + b_0 \cdot a$

- Circuit system
  - Barrel shifter (See next slide.)
  - Logarithmic shifter

Algorithms and circuits of other arithmetic operations (multiplication, division, discrimination, modulo) will be covered in the lectures of integrated circuit C and D.

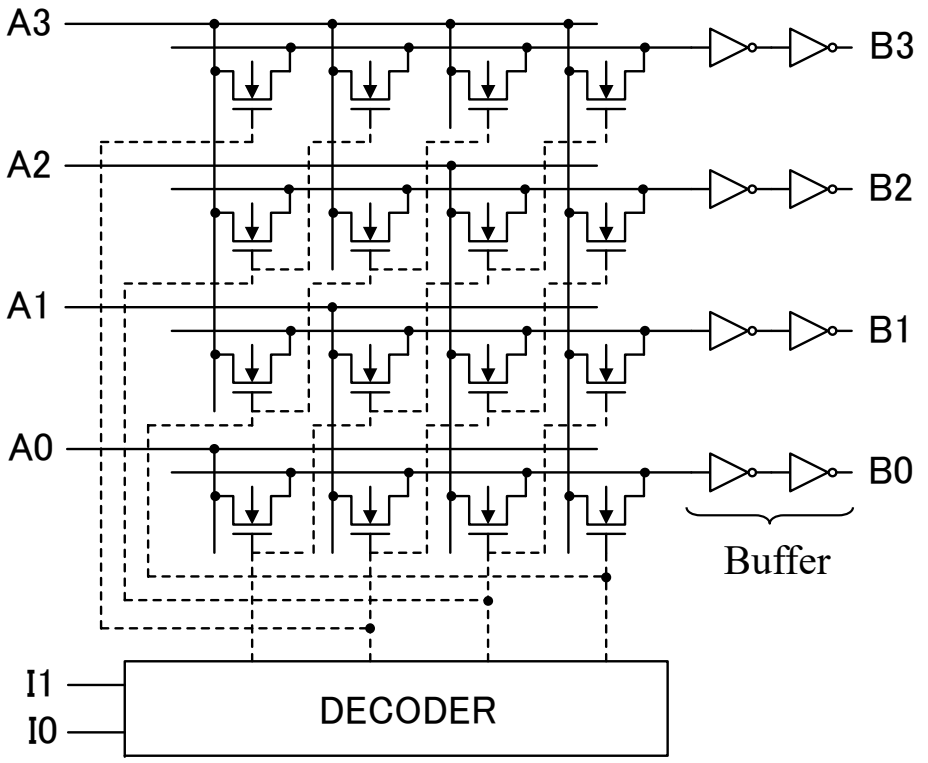
Barrel shifter

Truth table of right shift operation

Sh3	Sh2	Sh1	Sh0	B3	B2	B1	B0
0	0	0	1	A3	A2	A1	A0
0	0	1	0	A3	A3	A2	A1
0	1	0	0	A3	A3	A3	A2
1	0	0	0	A3	A3	A3	A3

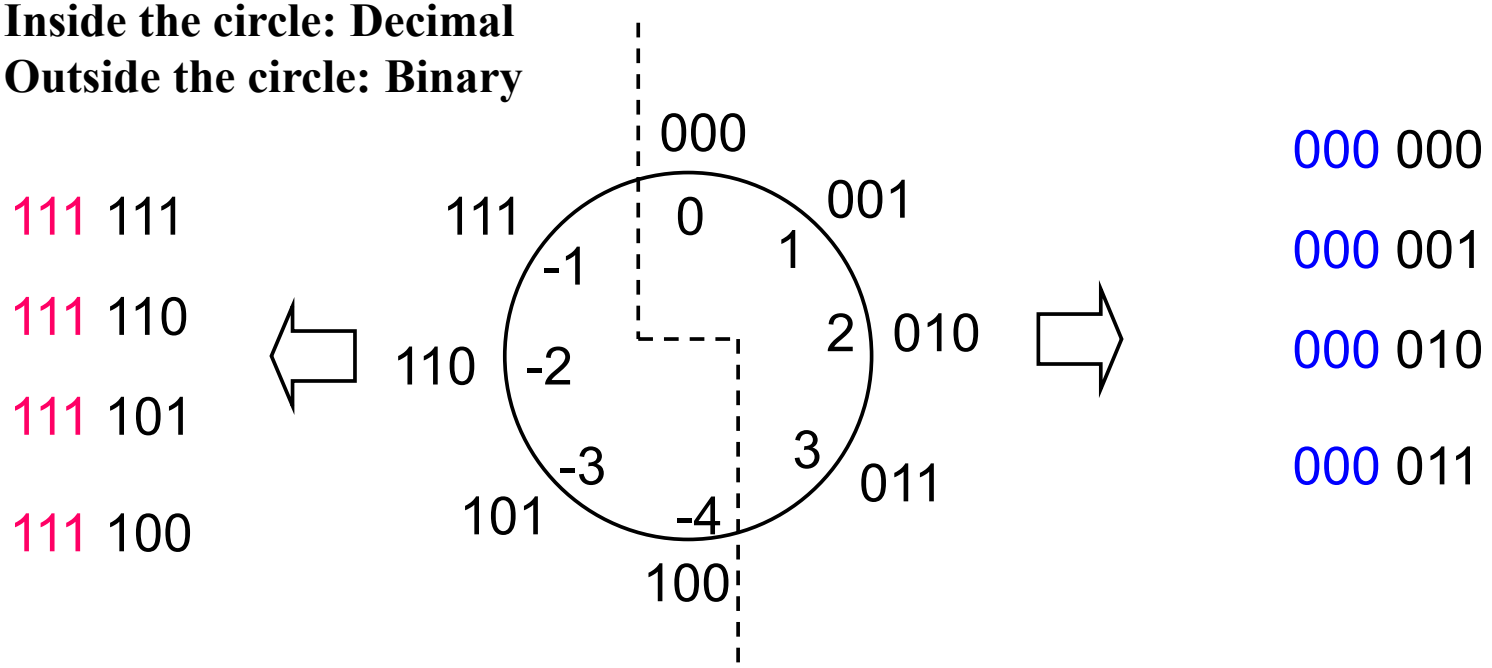
The blue A3 is a sign-extended value.

Rhe n-ch MOSFET switch matrix
(The p-ch MOSFET switch matrix is omitted.)



Sign extension (符号拡張)

Inside the circle: Decimal
Outside the circle: Binary



Extended 6bit complement (Negative number)

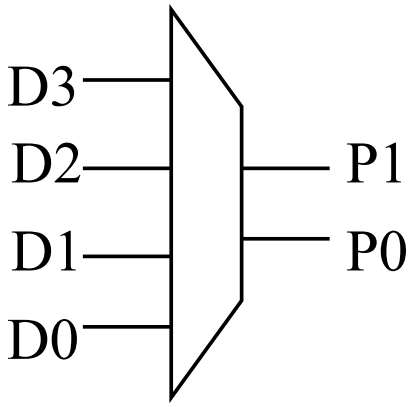
3bit complement

Extended 6bit complement (Positive number)

⇨ The value of MSB is added as the upper bits.

3.2.4 Encoder

Function of encoder



If there are 2n input lines, and at most only one of them will ever be high, the binary code of this 'hot' line is produced on the n-bit output lines.

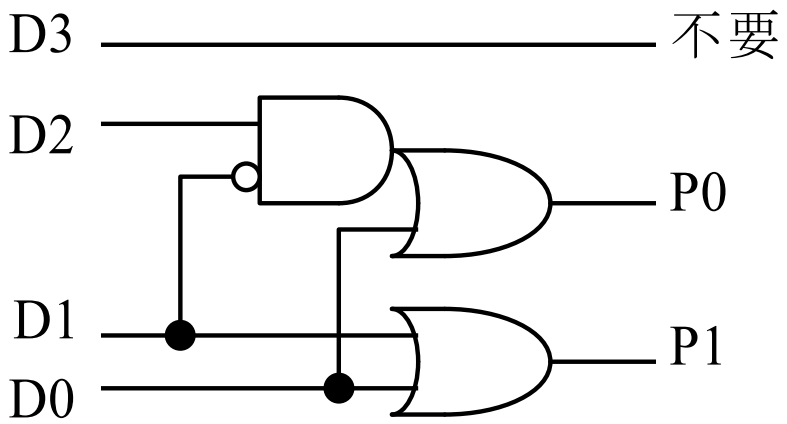
Truth table

D3	D2	D1	D0	P1	P0
0	0	0	0	(0	0)
DC	DC	DC	1	1	1
DC	DC	1	0	1	0
DC	1	0	0	0	1
1	0	0	0	0	0

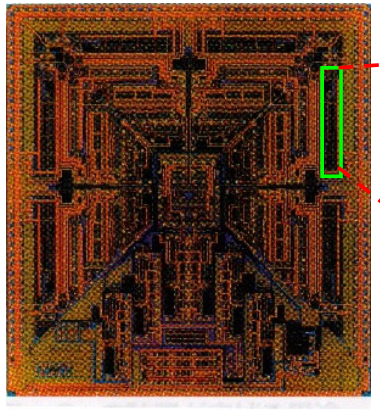
Circuit of encoder

$$P1 = D0 + \overline{D0} \cdot D1$$
$$= D0 \cdot (1 + D1) + \overline{D0} \cdot D1$$
$$= D0 + D0 \cdot D1 + \overline{D0} \cdot D1$$
$$= D0 + (D0 + \overline{D0}) \cdot D1$$
$$= D0 + D1$$

$$P0 = D0 + \overline{D0} \cdot \overline{D1} \cdot D2$$
$$= D0 + \overline{D0} \cdot (\overline{D1} \cdot D2)$$
$$= D0 \cdot (1 + \overline{D1} \cdot D2) + \overline{D0} \cdot (\overline{D1} \cdot D2)$$
$$= D0 + (D0 + \overline{D0}) \cdot (\overline{D1} \cdot D2)$$
$$= D0 + \overline{D1} \cdot D2$$



Usage example of encoder

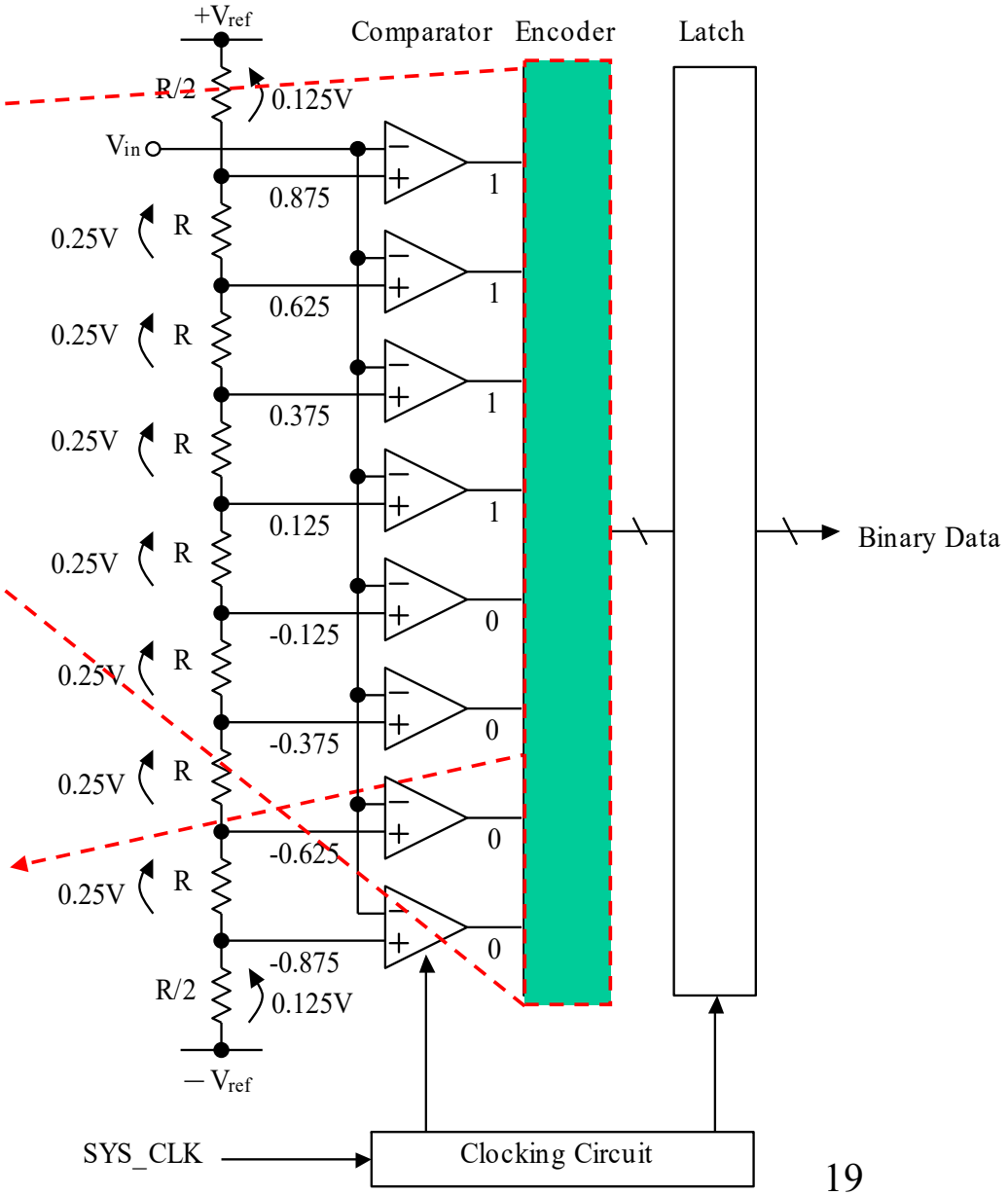


Lecroy 10GS/s ADC

Flash ADC

$V_{ref} = 1V$

$V_{in} = 0V$



Vin (V)	Thermometer Code		Binary Code
~ -0.875	1 1 1 1	1 1 1 1	(1) 0 0 0
-0.875 ~ -0.625	0 1 1 1	1 1 1 1	1 1 1
-0.625 ~ -0.375	0 0 1 1	1 1 1 1	1 1 0
-0.375 ~ -0.125	0 0 0 1	1 1 1 1	1 0 1
-0.125 ~ 0.125	0 0 0 0	1 1 1 1	1 0 0
0.125 ~ 0.375	0 0 0 0	0 1 1 1	0 1 1
0.375 ~ 0.625	0 0 0 0	0 0 1 1	0 1 0
0.625 ~ 0.875	0 0 0 0	0 0 0 1	0 0 1
0.875 ~	0 0 0 0	0 0 0 0	0 0 0

Encode