3.3 Synchronization

Removing a hazard and a timing control

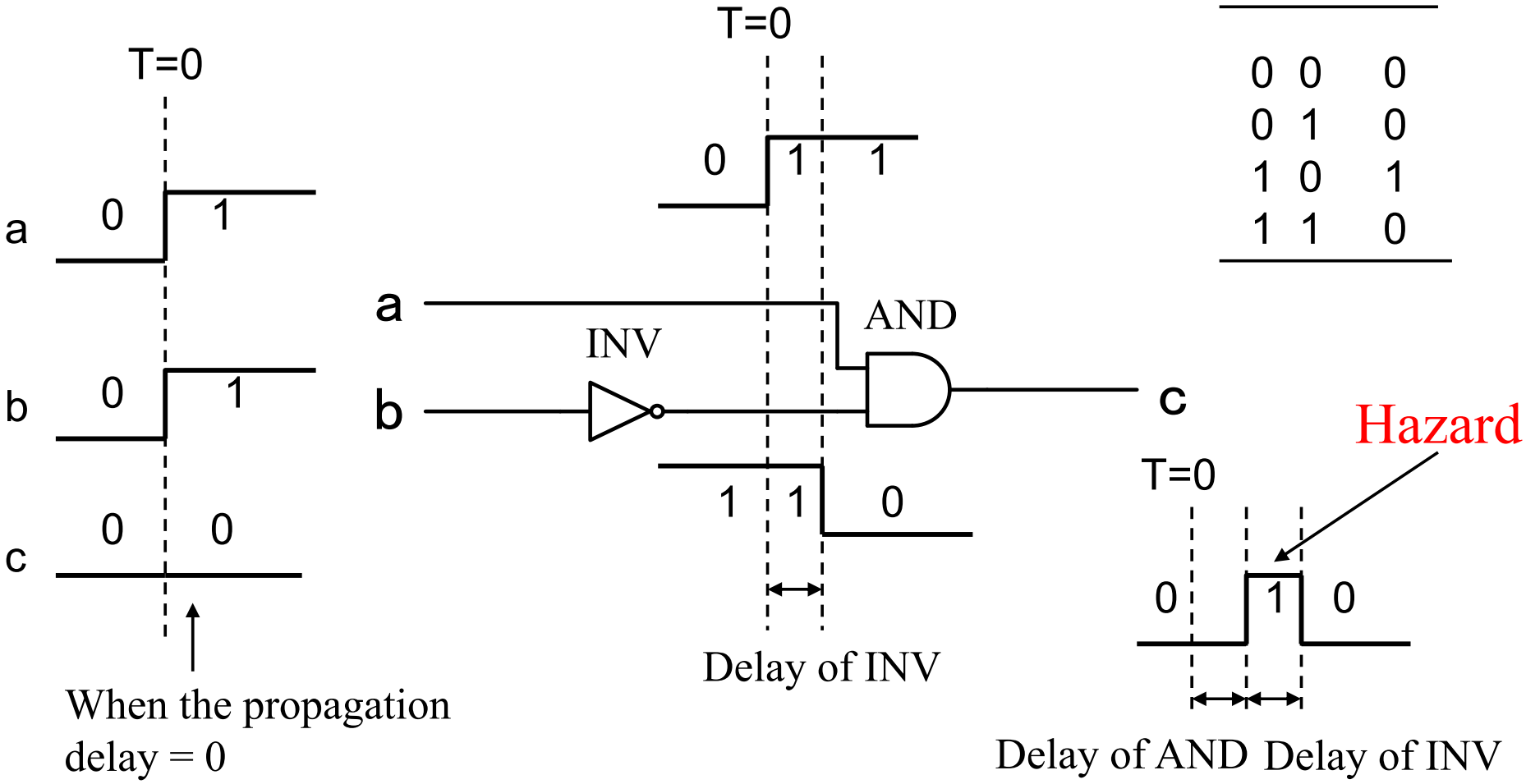
3.3.1 Hazard in combinational logic

Example of single output

The 2-input logic generates the hazard (incorrect result) during the delay time of the signal path.

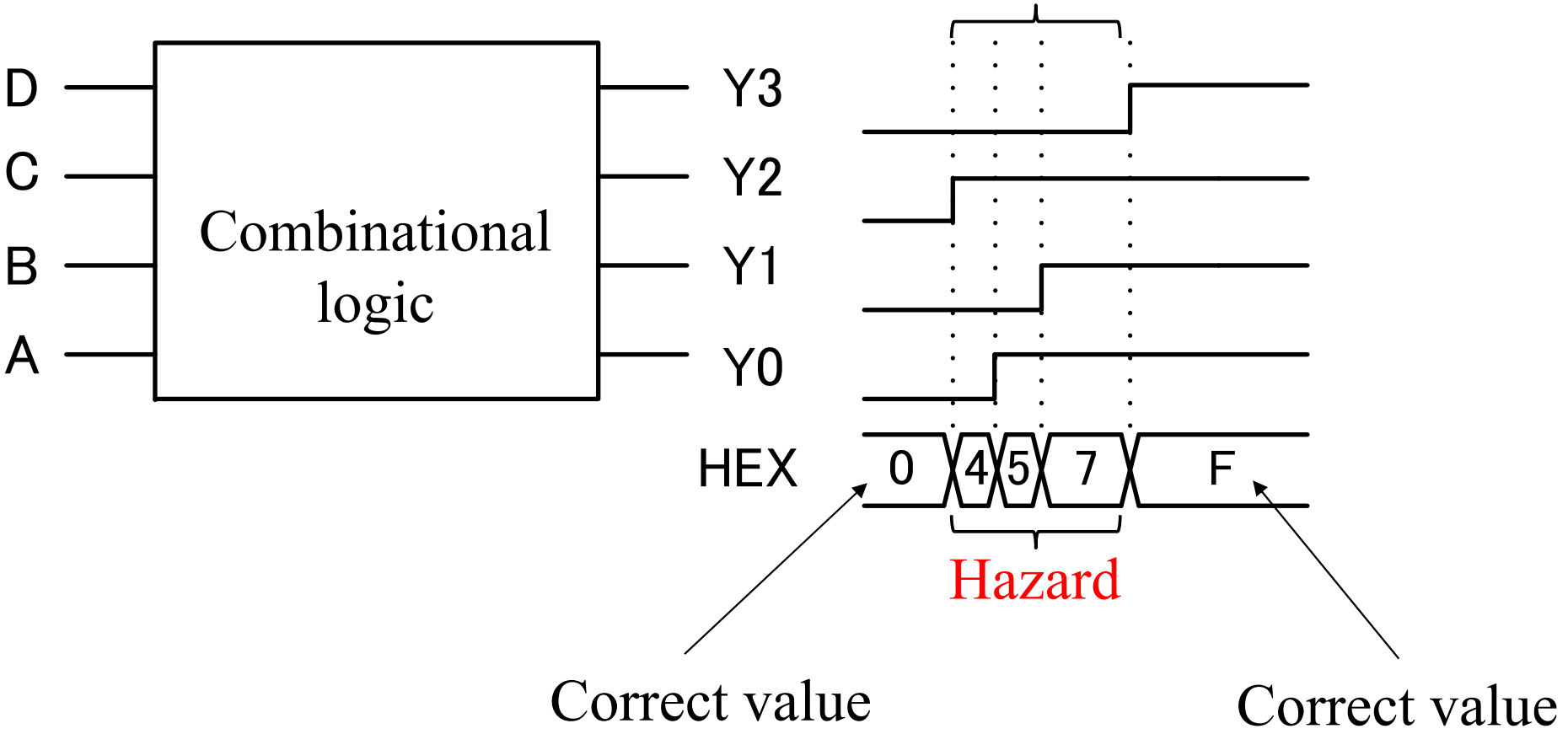
Truth table

a	b	c
0	0	0
0	1	0
1	0	1
1	1	0



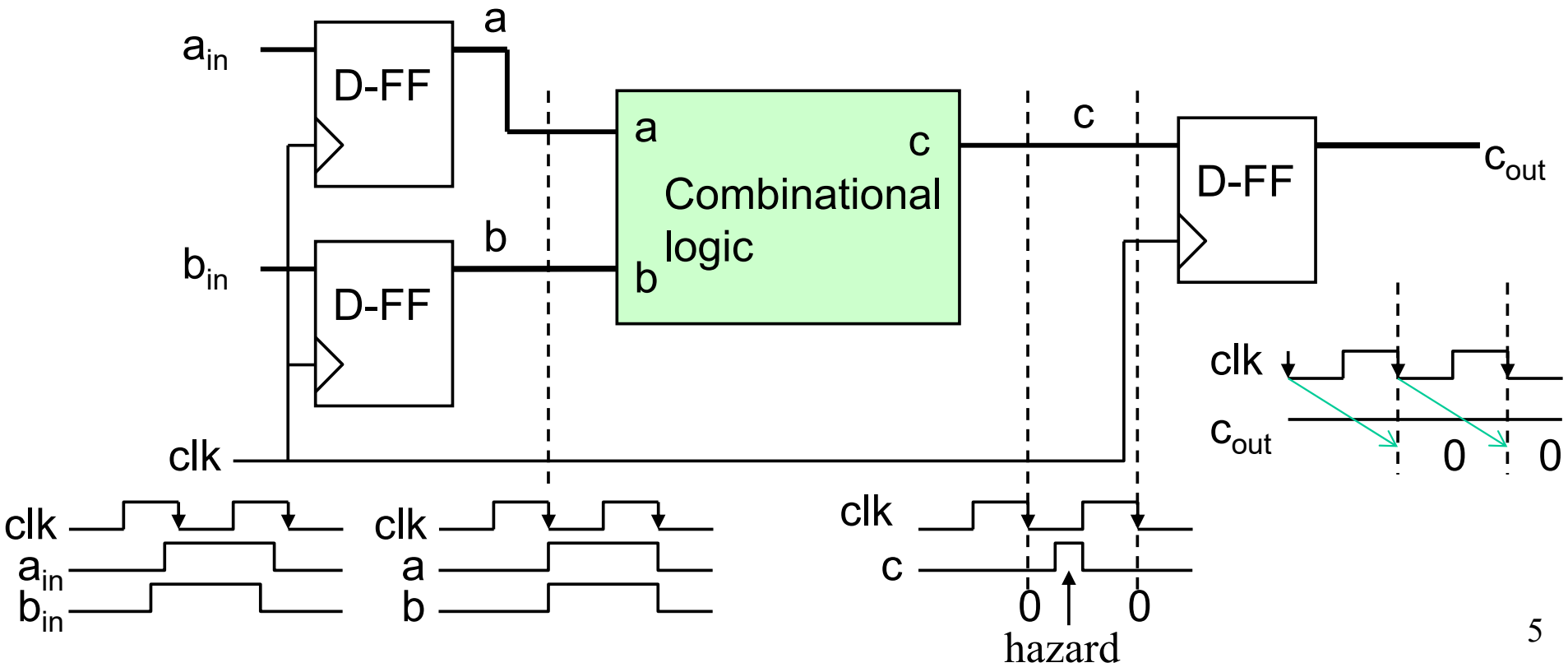
Example of multiple output

The time-of-arrival of each output is different from each other.



Sequence control of combinational logic

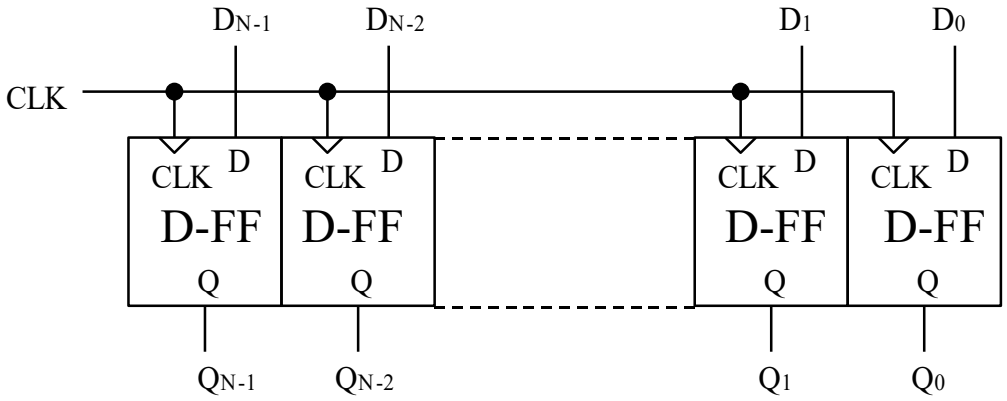
- The hazard is removed by using a synchronizing clock.
- The logic synthesizers basically generates the synchronous circuits.



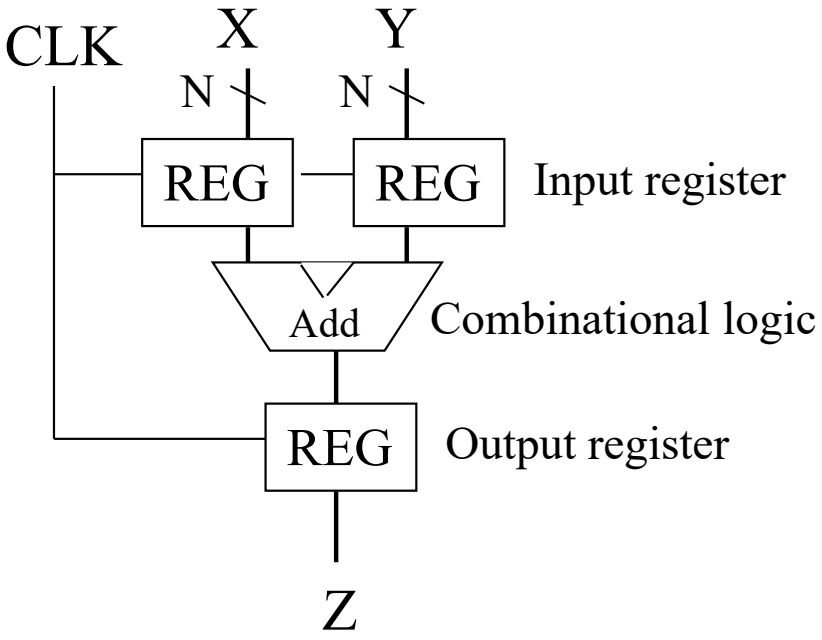
Circuit of register

I/O register
Pipeline register
Instruction register
Address register

These registers synchronize any signals of ALU, IO and BUS.

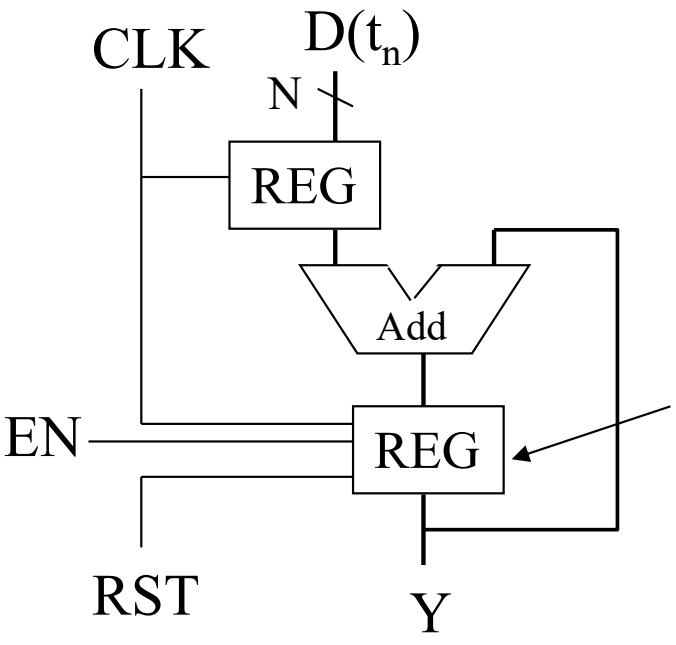


N bit Register



Accumulator

1. The registers are reset before accumulation.
2. This circuit performs an accumulation during EN = 1.

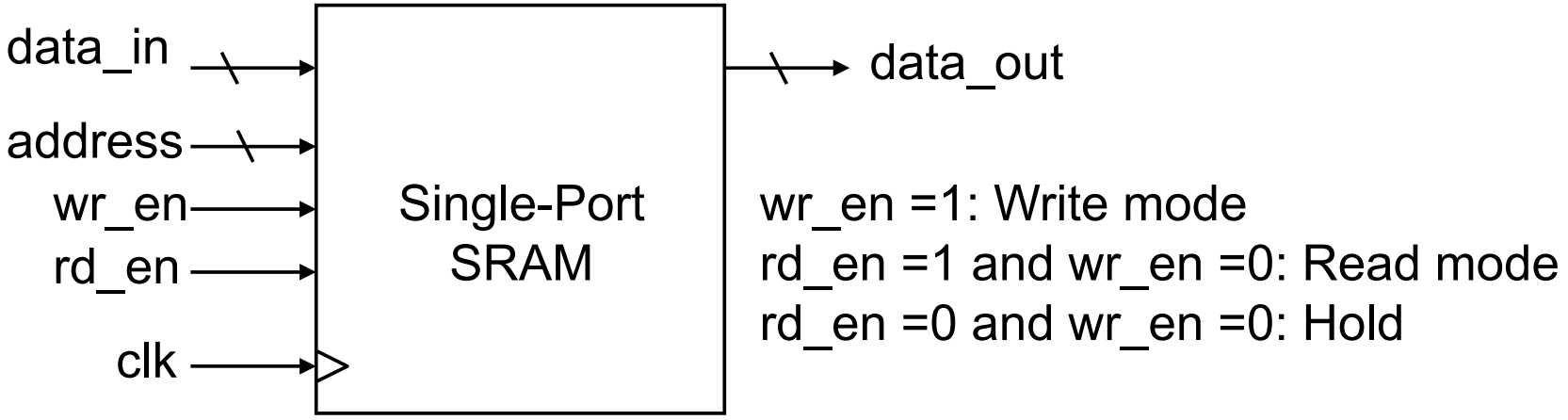


A register with reset and enable.

Note: The output value of D-FF is unknown after power-on. The initialization or reset signal is required.

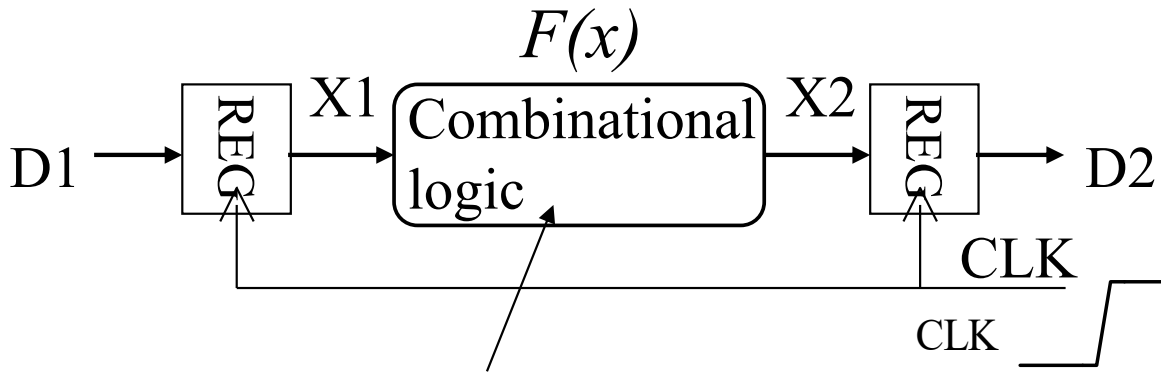
Register and memory

- 2 types of embedded memoirs
  - Register file
    - consists of an array of registers and an address decoder . ← Synthesizable from HDL code.
    - can be also implemented by using a high-speed multiport SRAM.
  - SRAM (Static Random Access Memory)
    - An SRAM is usually provided in the form of IP core.
    - You can design a SRAM core, however, the knowledge of the transistor-level design is required.

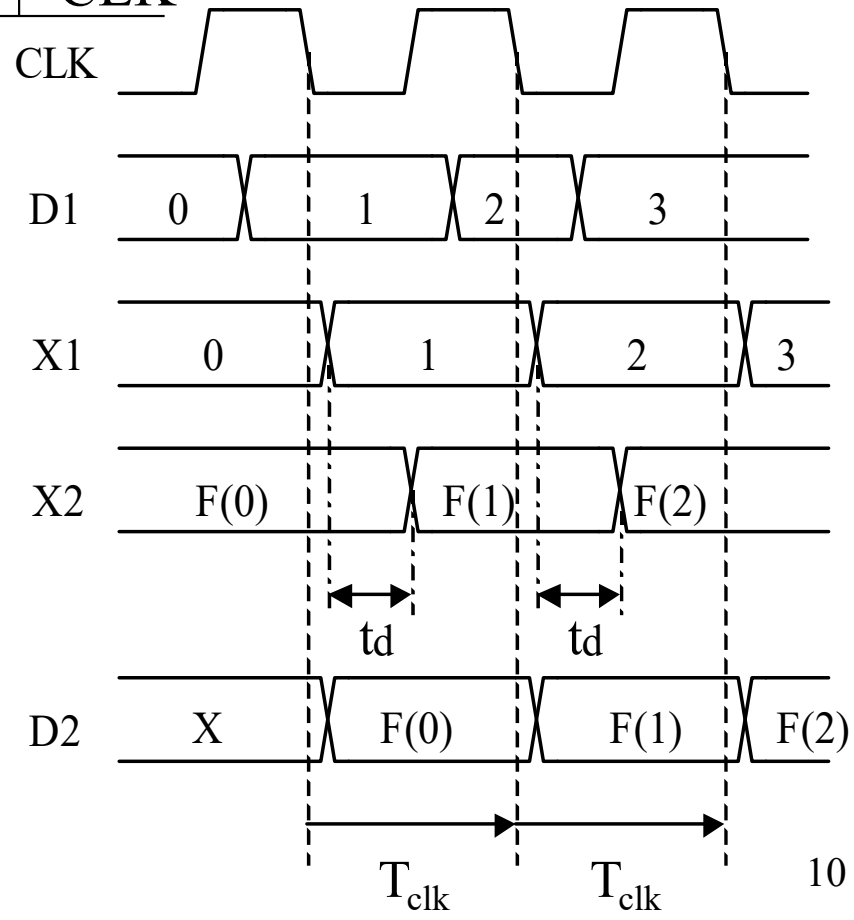


3.3.2 Maximum clock frequency

Maximum delay constraint



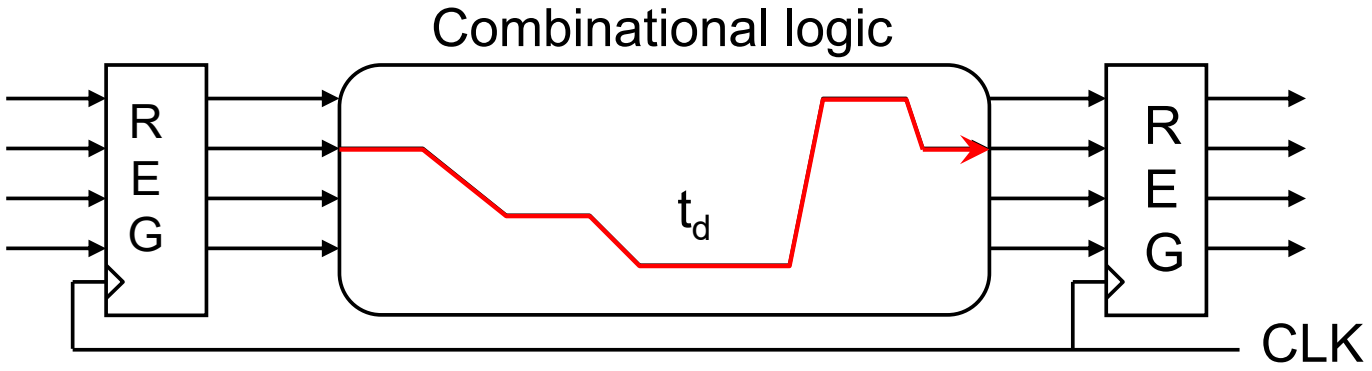
A signal propagation path which has a maximum delay time is called a critical path of combinational logic.



Constraint: $t_d < T_{clk}$

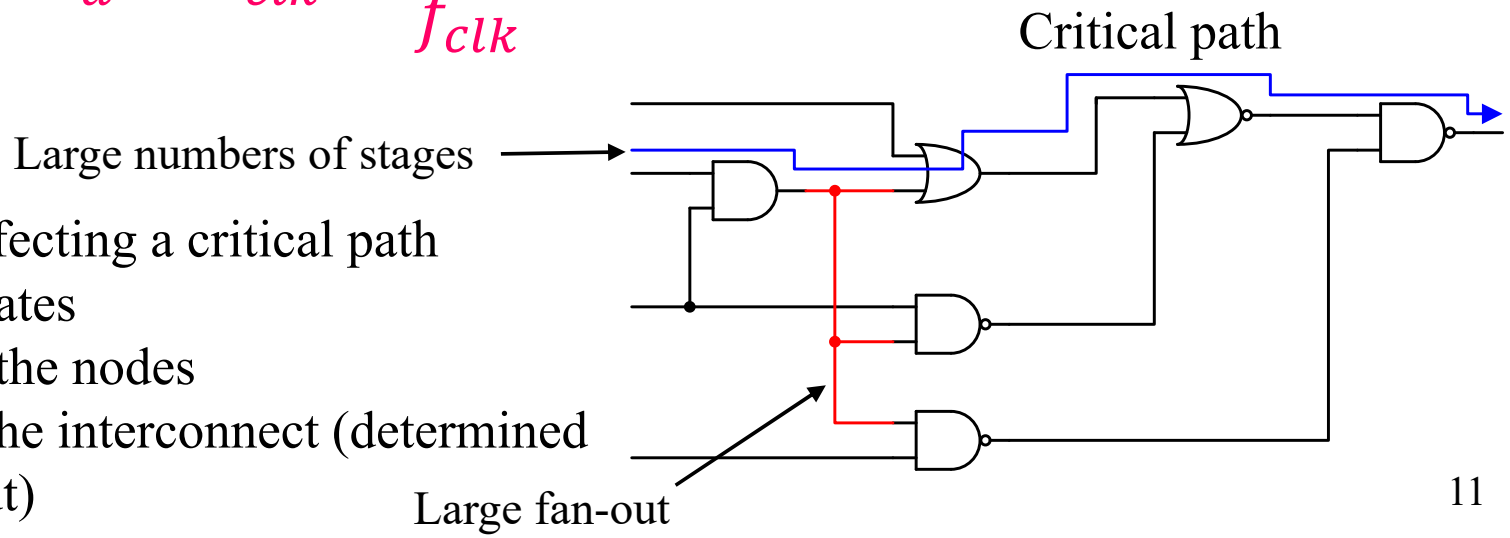
The result is output after one clock cycle.

The factors affecting a critical path



The delay time t_d of the signal propagation through the critical path is longest.
The delay time of the critical path must be smaller than the period of the clock signal.

$$t_d < T_{clk} = \frac{1}{f_{clk}}$$

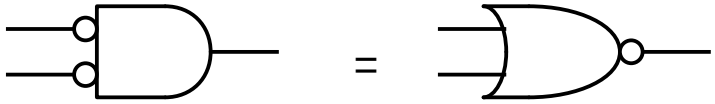


The factors affecting a critical path

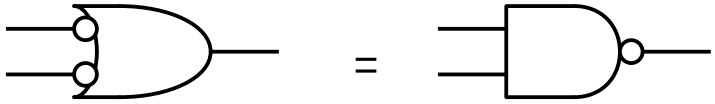
- Stages of gates
- Fan-out of the nodes
- Length of the interconnect (determined after the layout)

Improvements of a critical path

$$\overline{A} \cdot \overline{B} = \overline{A + B}$$

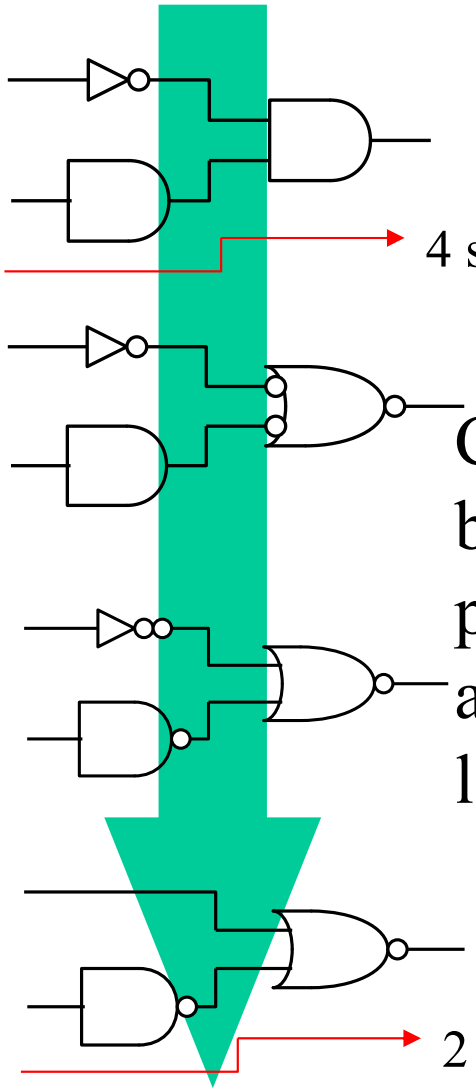


$$\overline{A} + \overline{B} = \overline{A \cdot B}$$



De Morgan's theorem

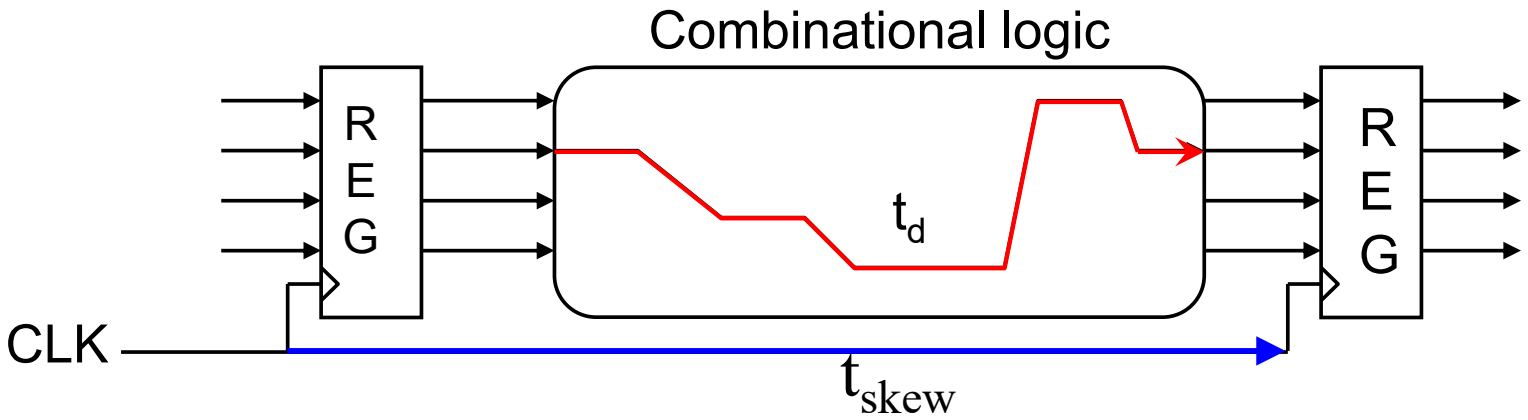
Note: Do not carry out the optimization of logic stages manually. This procedure should be left to CAD software.



Conversion between positive logic and negative logic.

Clock skew

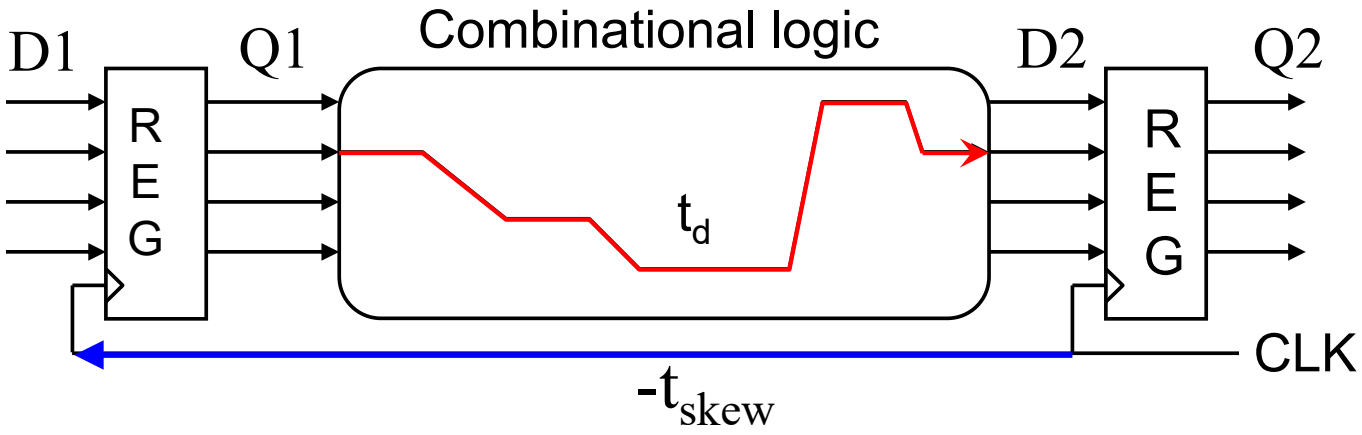
A phenomenon in synchronous digital circuit in which the same sourced clock signal arrives at different components at different times.



If $t_d < t_{skew}$, the result of the combinational logic is output from the output resistor in the same clock cycle as input cycle. (The result should be output one cycle later.)

Racing

A clock skew causes a racing between the signal in the combinational logic and the clock signal.

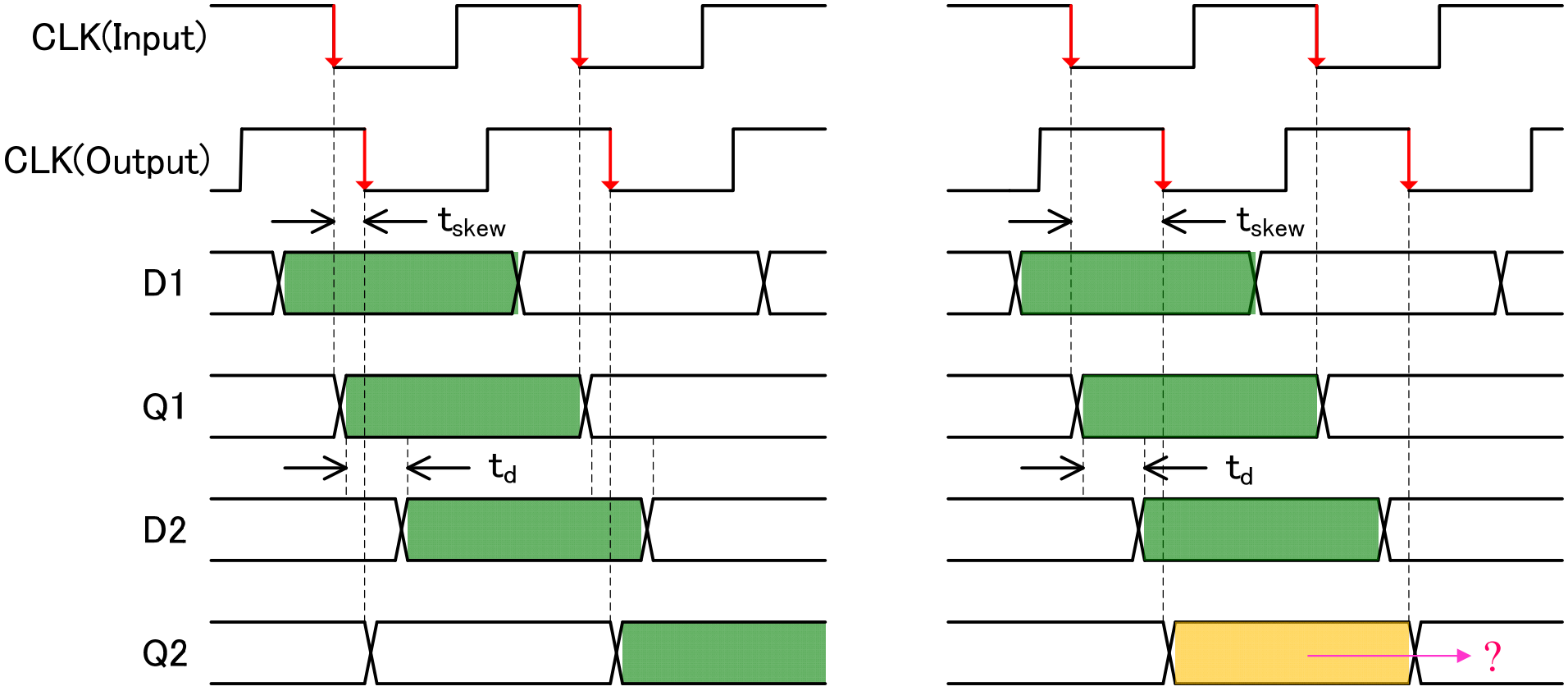


$t_d < t_{skew}$ (Previous slide) : An error occurs by racing.
$t_d > 0 > -t_{skew}$ (See the illustration): The circuit operates normally.

Summary of timing constraint

$T_{clk} > t_d - t_{skew}$
$t_d > t_{skew}$ (Normal)

$T_{clk} > t_d - t_{skew}$
$t_d < t_{skew}$ (Error)

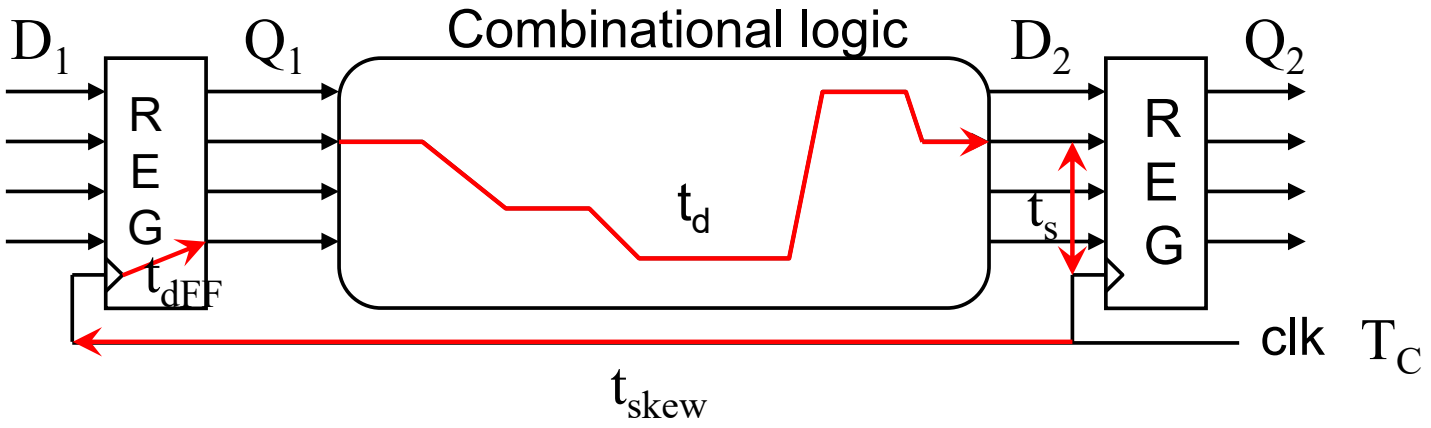


STA (Static Timing Analysis)

- STA and logic simulation
  - The delay time can be calculated by STA and logic simulation.
  - In STA, the delay time is calculated from the number of the stages and the number of fanout through the critical path.
  - STA has an advantage in comparison with the timing simulation, because the it does not require the test vector and does not take a lot of time.
  - STA satisfy the timing constraints for the logic synthesis.
- Propagation delay of logic gates and wires
  - A prorogation delay is a total of a gate delay and a wiring delay.
  - A gate delay is estimated by a delay information of each gates.
  - A wiring delay is estimated by a delay model based on a statistical data which associates a delay time with a wiring length.

3.3.3 Detail of the timing constraint

Timing constraints of synchronous circuits 1

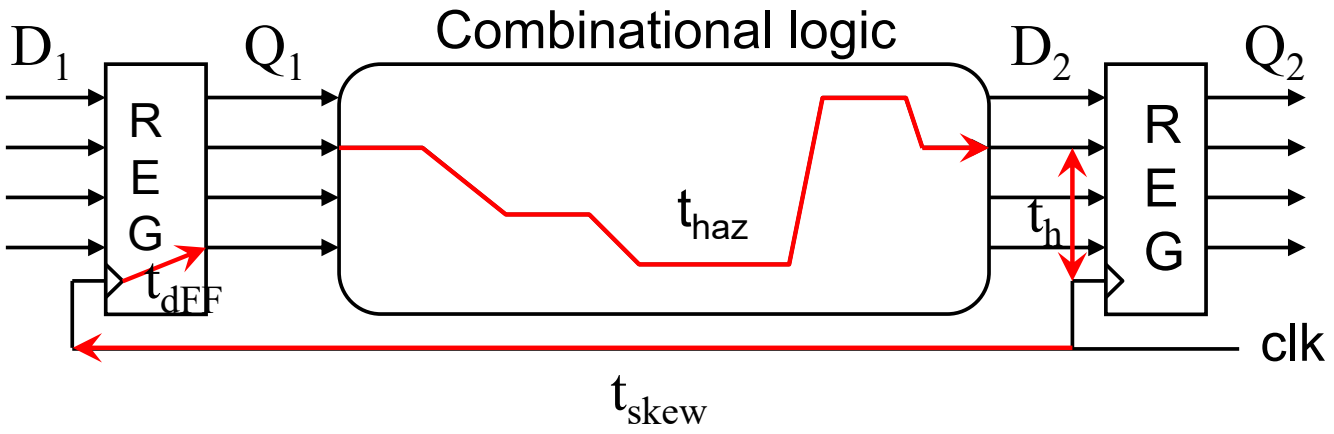


t_{dFF}: Delay time of the register
t_d: Delay time of the critical path
t_{skew}: Clock skew (Note the transmitting direction of the clock.)
t_s: Setup time of the register

$$T_C > t_{dFF} + t_d + t_{skew} + t_s$$ (Setup time constraint)

- Large combinational logic: t_d is dominant.
- Small combinational logic: t_{skew} is comparable with td.

Timing constraints of synchronous circuits 2

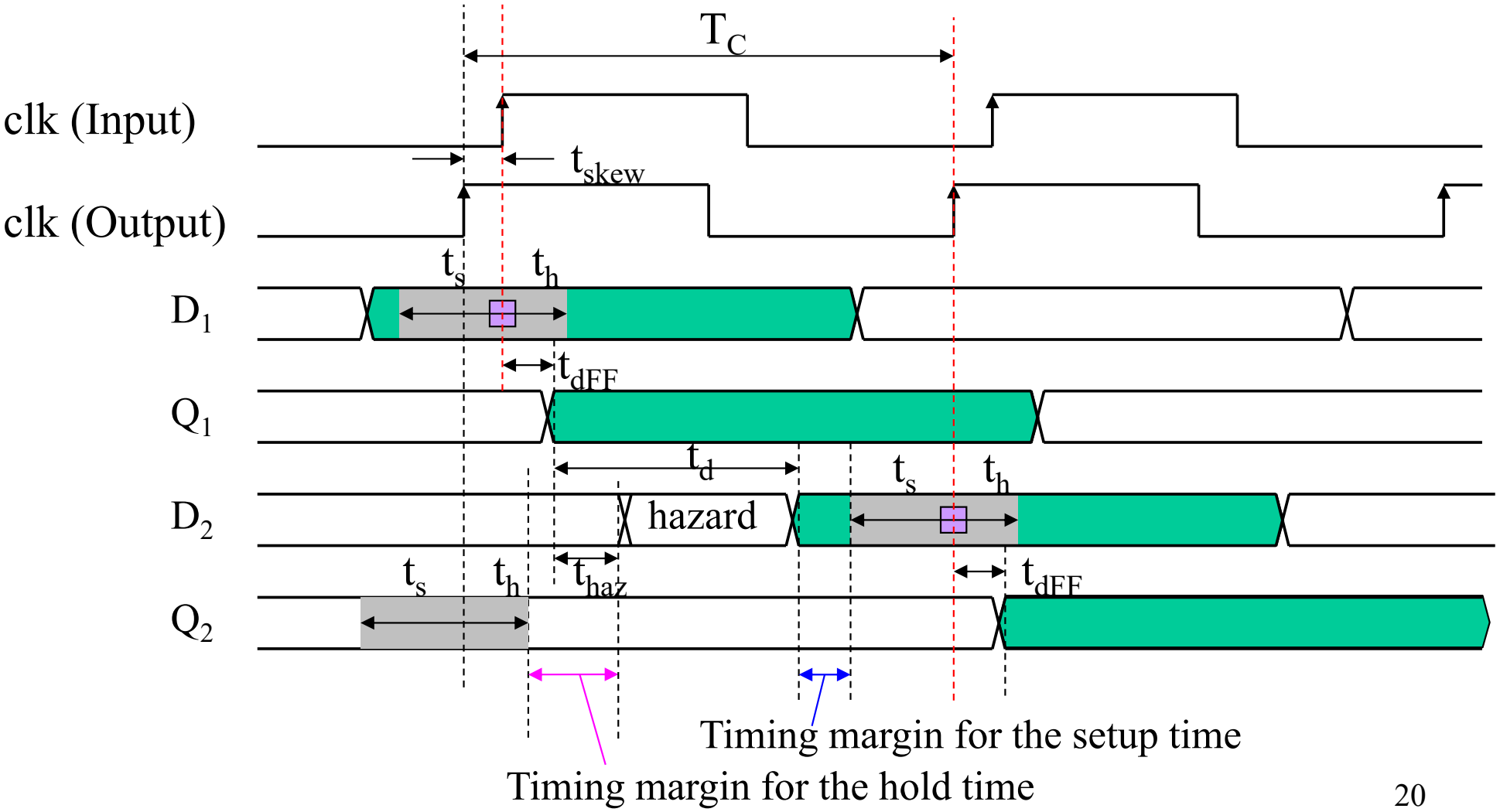


t_{dFF}: Delay time of the register
t_{haz}: Start time of hazards
t_{skew}: Clock skew
t_h: Hold tome of the register

$$t_h < t_{dFF} + t_{haz} + t_{skew}$$ (Hold time constraint)

When $t_{skew} < 0$ (The arrival time of the clock signal to the output register is delayed), there is a risk of the malfunction.

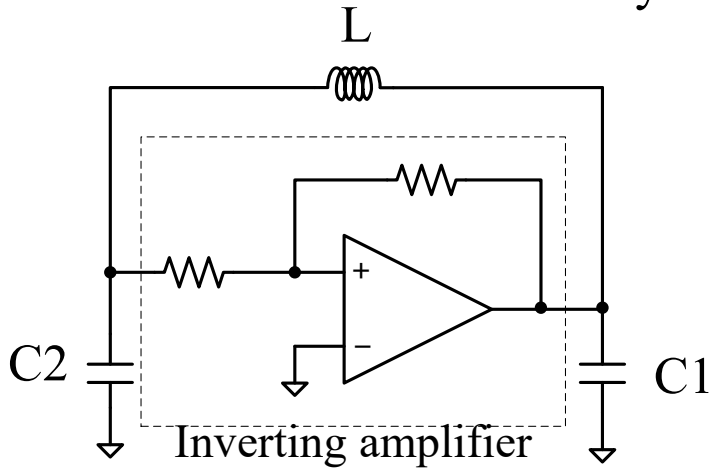
Detailed timing chart of synchronous circuits



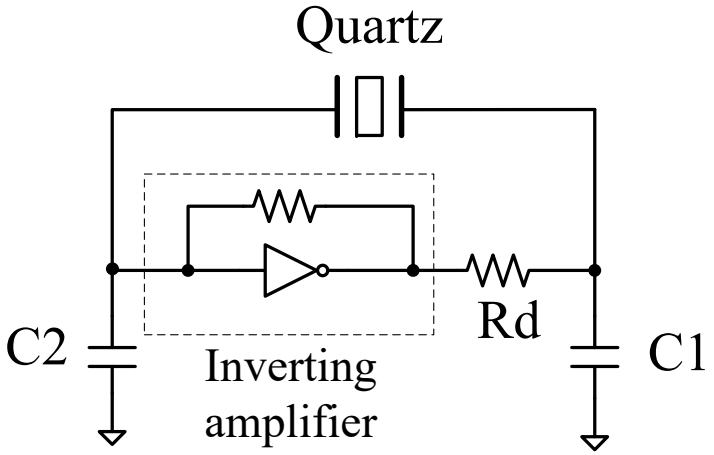
3.3.4 Clock generator

Reference clock generator

- Principle of quarts crystal oscillator is the same as a Colpitts oscillator. The quarts resonator is electrically equivalent to the inductor in the Colpitts oscillator.
- A Q factor of quarts crystal resonators is normally over 100,000. Therefore, the effective digit of the oscillation frequency is 6 digits.
  - Reference clock of digital systems
  - Real time clock (32.768kHz)
  - Reference clock of a wireless communication
  - Reference clock of audio systems (5.6448MHz)



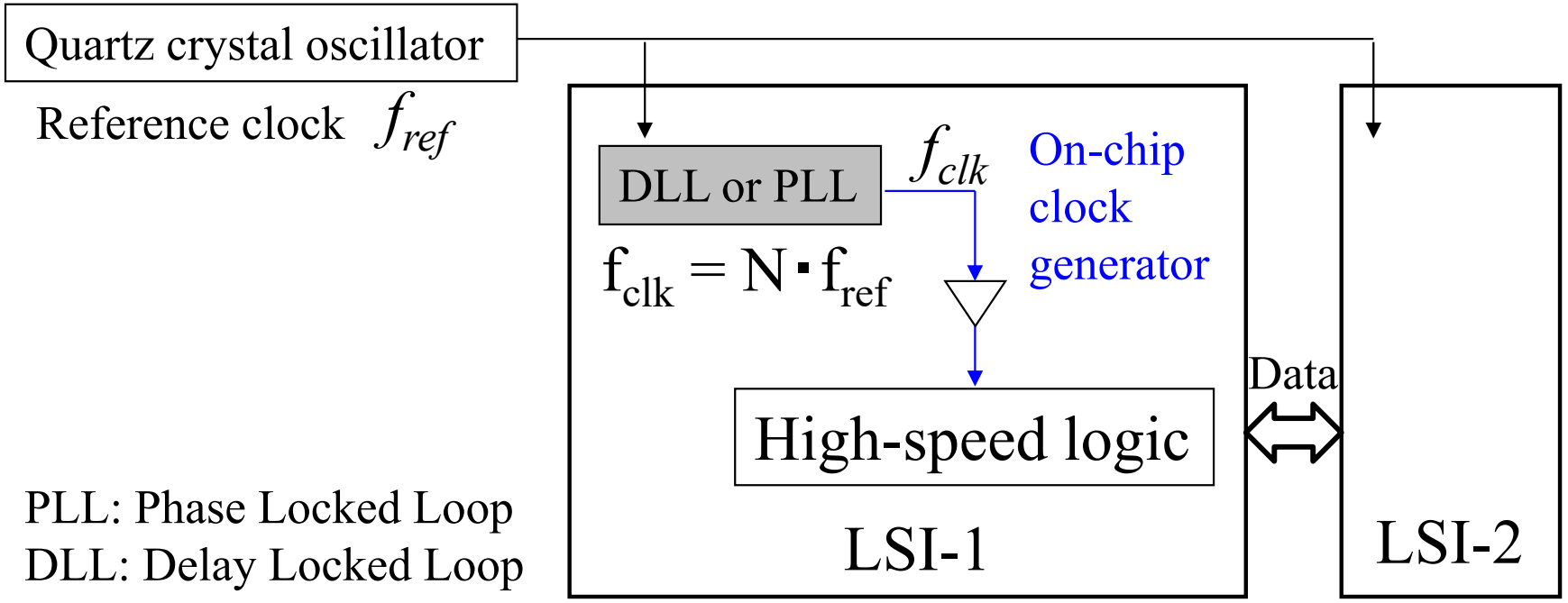
Colpitts oscillator



Quartz crystal oscillator

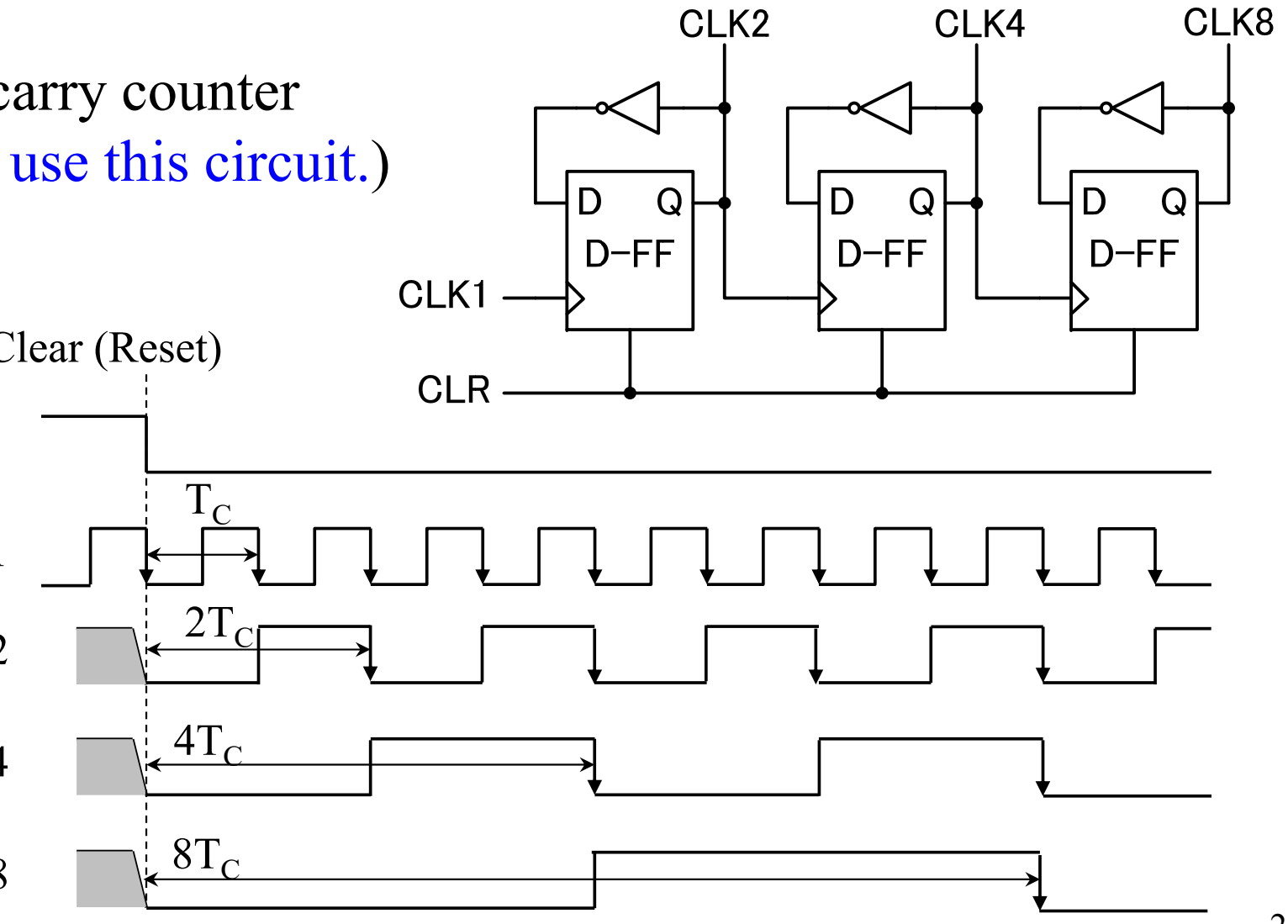
Synchronization at the system level

- The internal clock in each LSI is synchronized to the reference clock (System clock) .
- The reference clock frequency can be multiplied by PLL or DLL.
- The main clock signal in LSI is divided to the required frequency and distributed to the sub-systems.

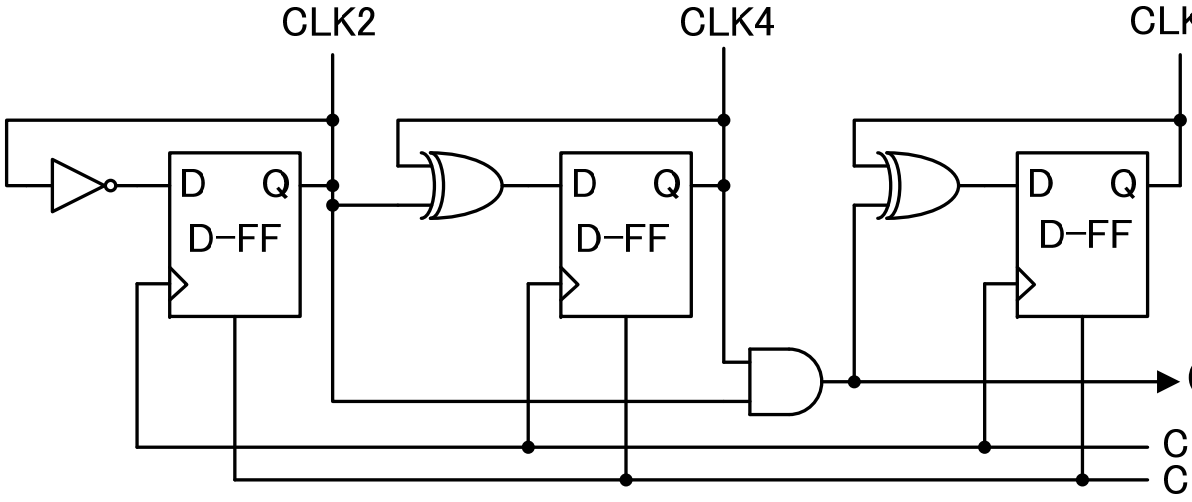


Asynchronous 2^i divider

Ripple carry counter
(Do not use this circuit.)



Synchronous 2^i divider



(The details will be discussed in Sec. 3.4.)