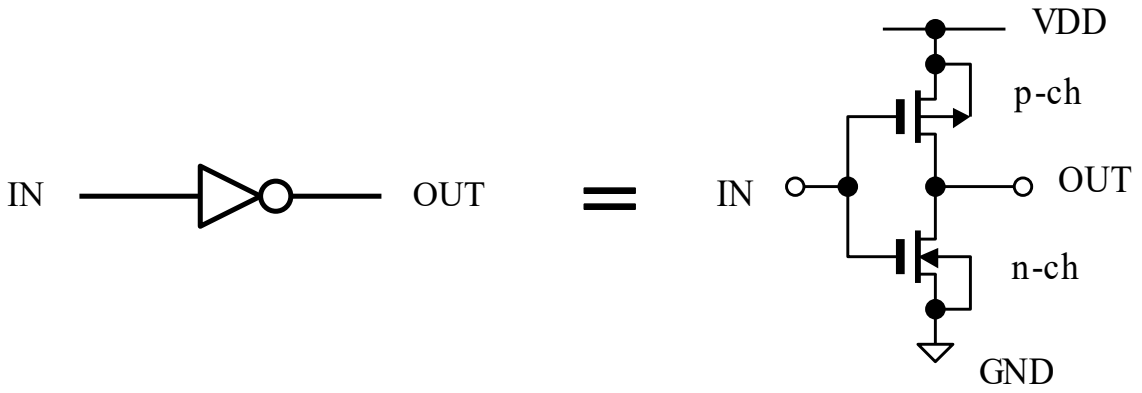
5.1 CMOS process

Overview of CMOS process

5.1.1 Structure of CMOS LSI

CMOS

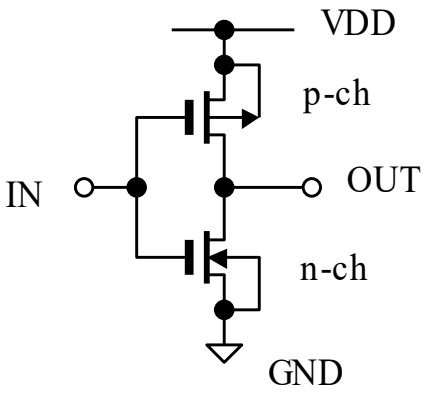
- Complementary Metal-Oxide-Semiconductor process flow is complicated, but CMOS circuits have a number of advantages as follows.
  - Low power consumption
  - High speed
  - High reliability (Less malfunction)
  - Small area of MOSFET



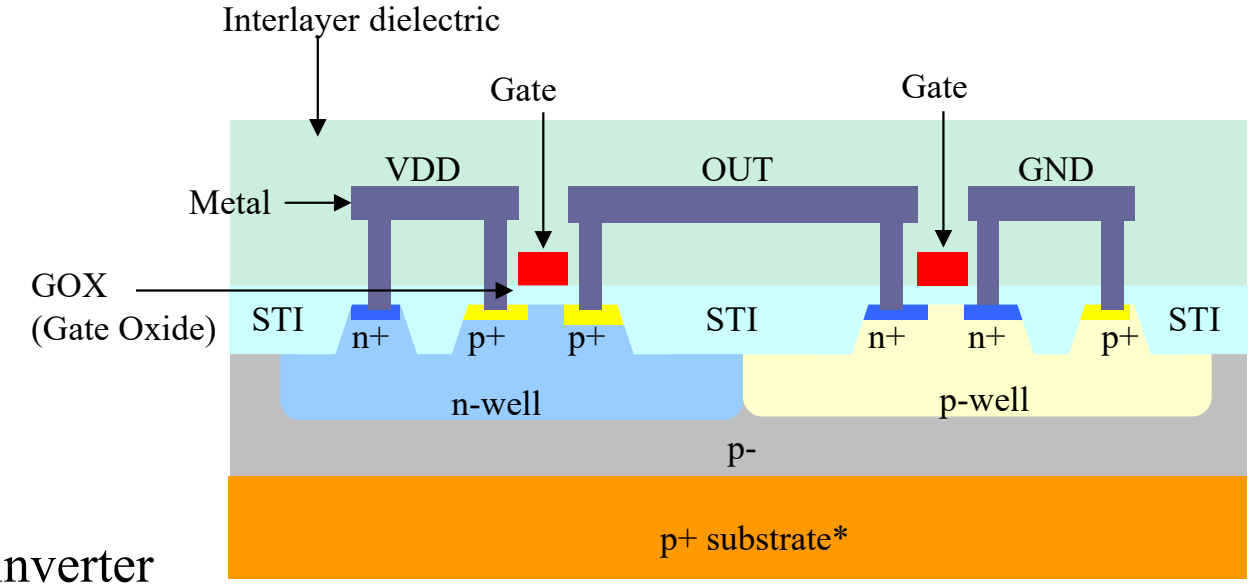
Symbol of inverter CMOS implementation of inverter

Structure of CMOS inverter

- A n-ch MOSFETs and A p-ch MOSFETs are integrated on a wafer.
  - A MOFET is formed in a well (or a tub).
- Electrical isolation between MOSFETs
  - STI (Shallow Trench Isolation) prevents the channel generating between MOSFETs.
  - A reverse bias between a n-well and a p-well provides an electrical isolation.



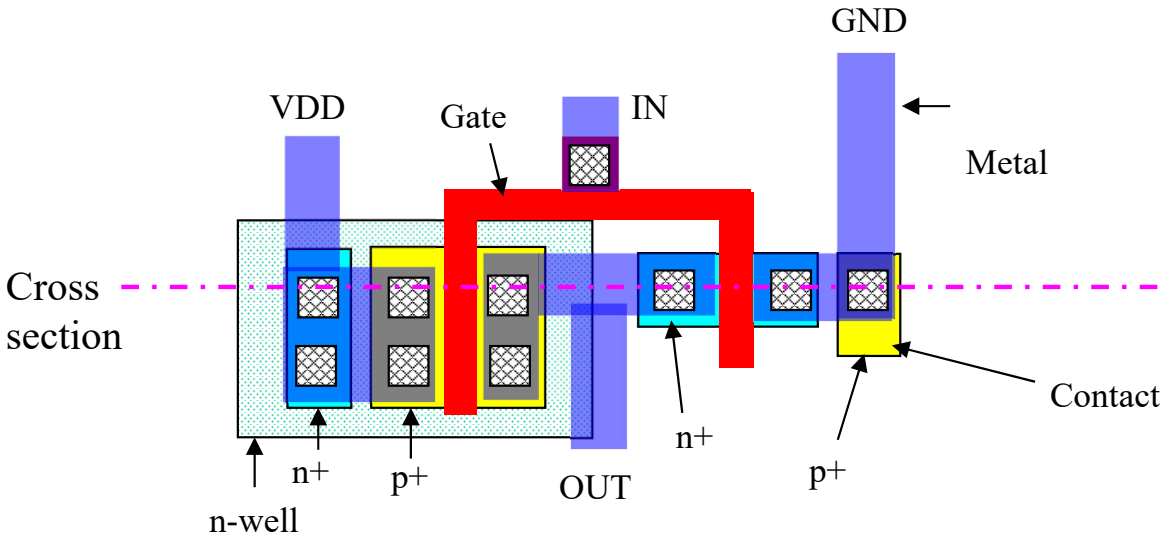
Schematic of CMOS inverter

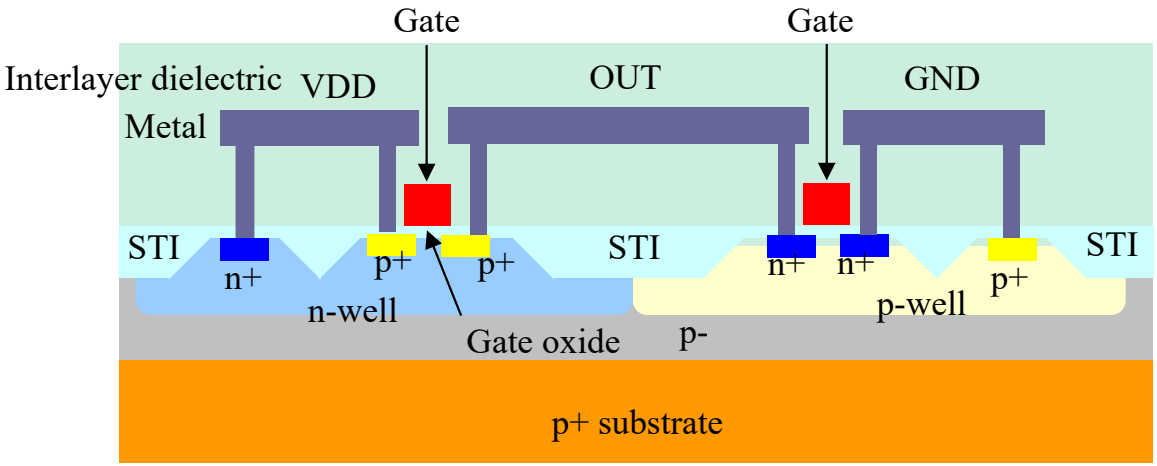


Structure of CMOS inverter (Twin well process)

* A silicon wafer is called a substrate of IC.

Layout and structure



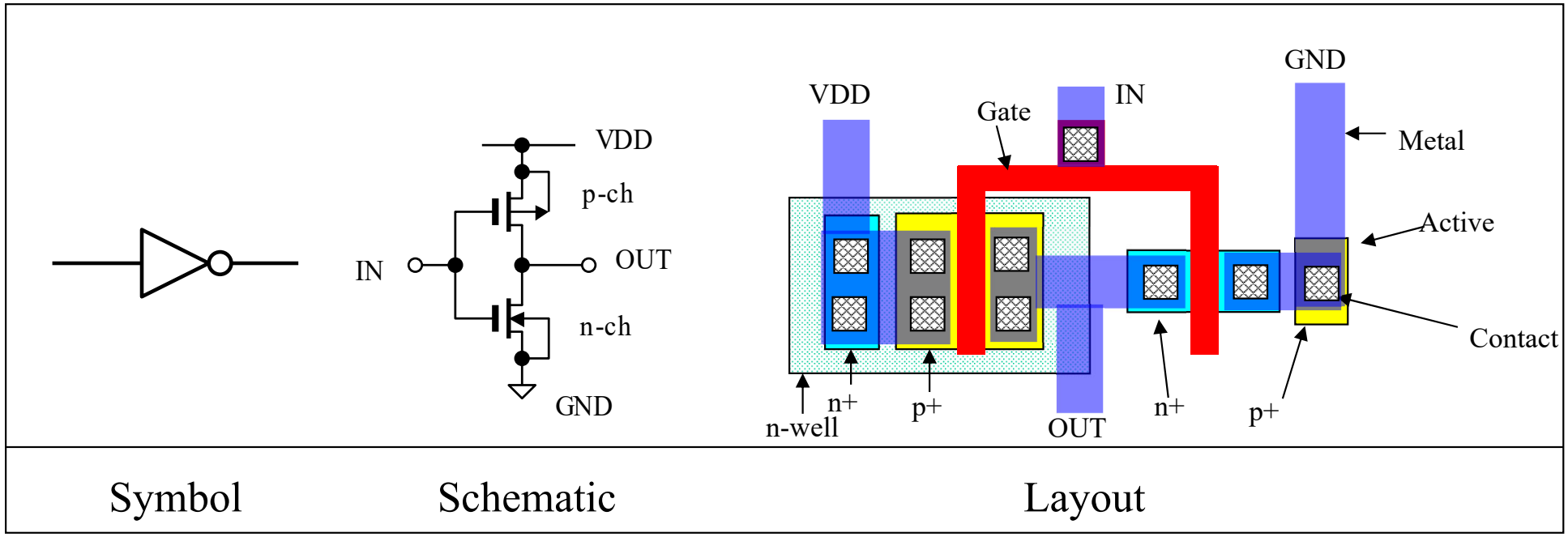


See section 5.1.3 for the details.

Terms

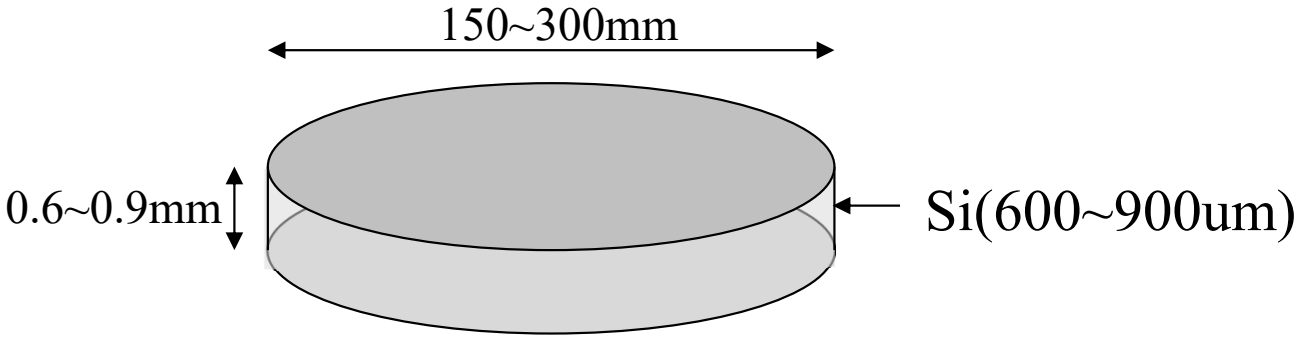
- n+ and p+ (diffusion) = Heavy doped semiconductor region
- Gate = Gate electrode (The common name is poly-Si or gate poly)
- Contact = Electrode between a silicon and a metal
- VIA = Interconnect between metal layers
- Well = n-type or p-type semiconductor region of a body area

Cell library

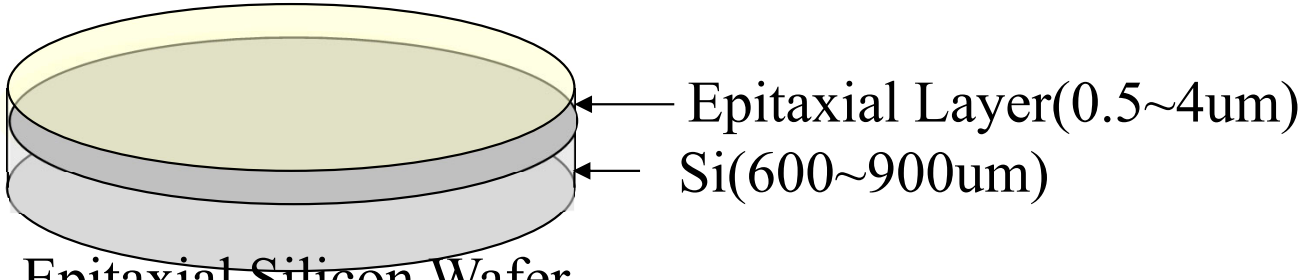


A database including a symbol, a schematic, a layout, logic function, and electrical properties such as propagation delay is called a cell library. A cell library is CAD software such as cell library is used in logic synthesis and place-and-rout.

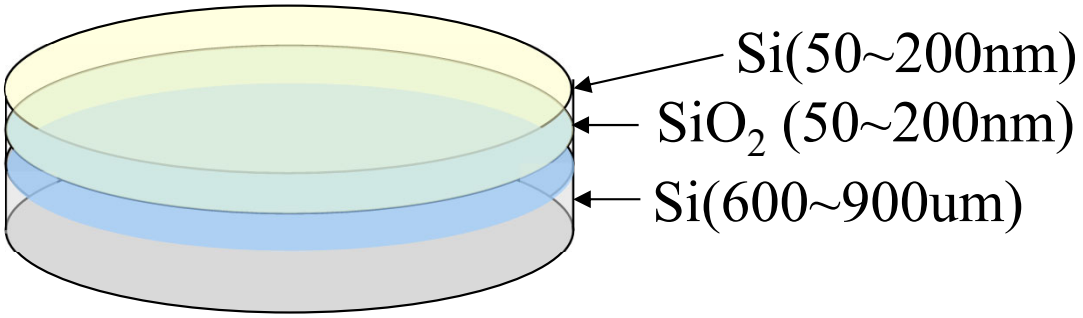
Structure of Si wafer



Bulk Polished Silicon Wafer



Epitaxial Silicon Wafer

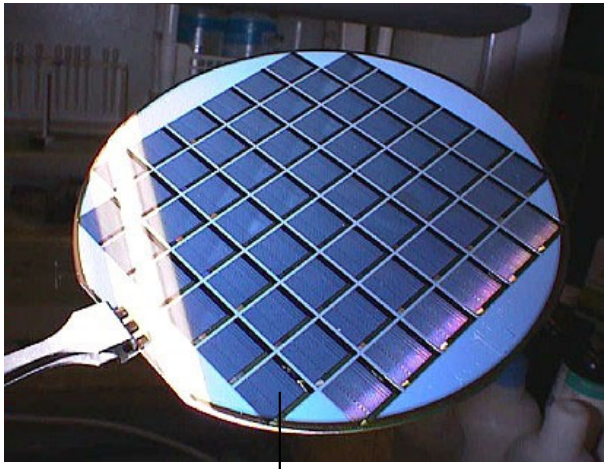


SOI Wafer (Silicon On Insulator)

SOI (Silicon on Insulator) wafer

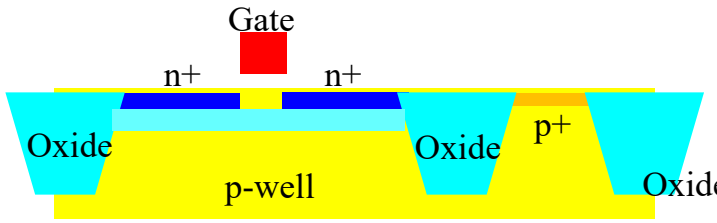
- Advantages of SOI structure
  - No well necessary for isolation between MOSFETs
  - High voltage operation (if needed)
  - Small parasitic (*i.e.* High speed)
  - Controllability of V_T (FD-SOI)

Thin film transistors
fabricated on the quarts wafer

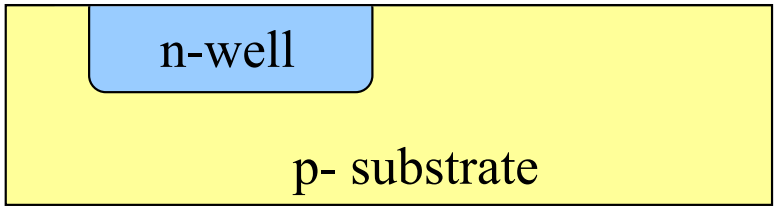


FD-SOI transistors fabricated on the single crystalline silicon wafer with buried SiO_2

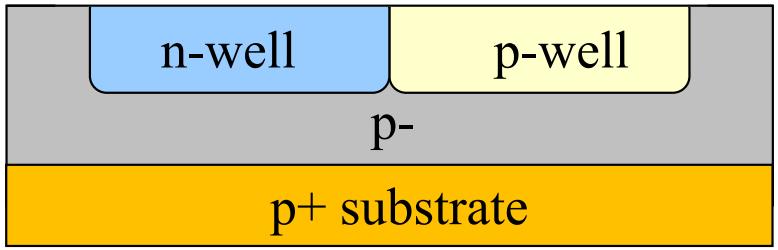
FD-SOI (Fully-Depleted Silicon on Insulator)



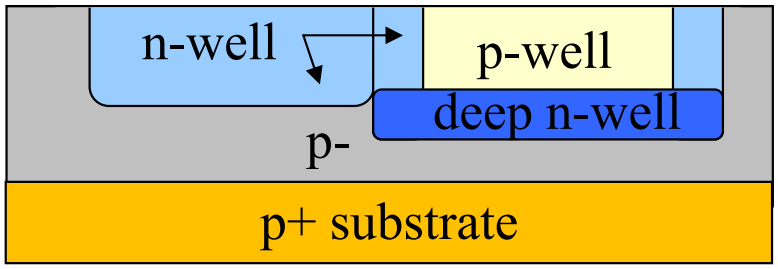
Well



n-well (Single well)
(The n-ch MOSFET is fabricated on the p-substrate.)

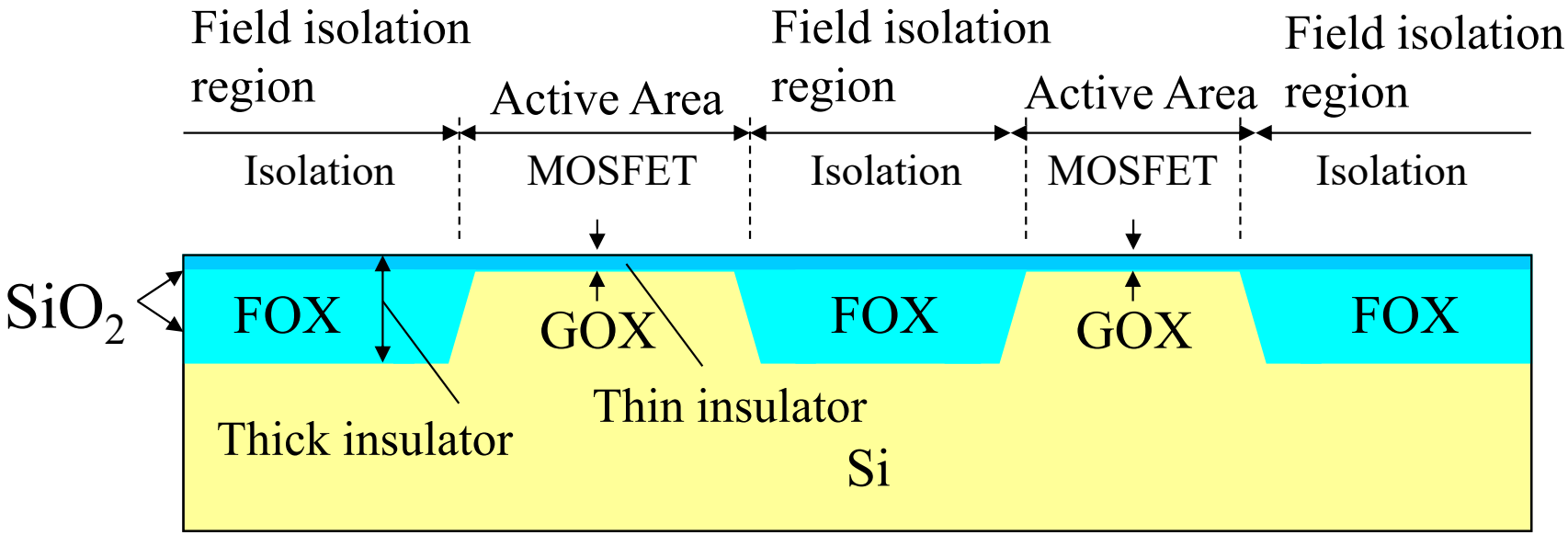


Twin-well
(The p-wells are not isolated.)



Triple-well
(The deep n-well isolates the p-well or retrograde p-well.)

Isolation



Field Oxide (FOX): Thickness = 100nm

Gate Oxide (GOX): Thickness = nanometer scale**

- The thick SiO_2 of FOX prevents the channel generating.
- The thin SiO_2 of GOX can produce the channel.

* FOX is formed by STI (Shallow trench isolation) process (described below)

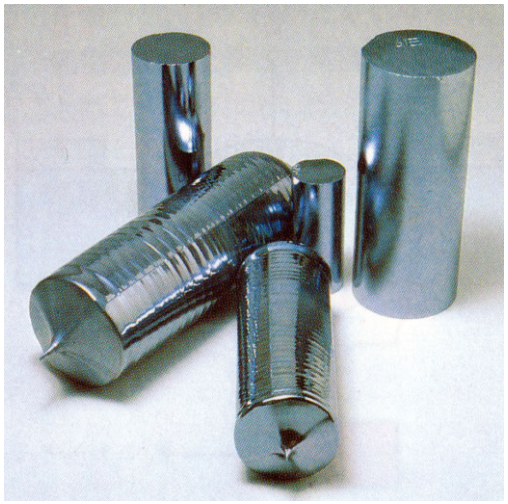
** High-k dielectrics are used in advanced technology where they are usually used to replace a silicon dioxide gate dielectric.

5.1.2 LSI process

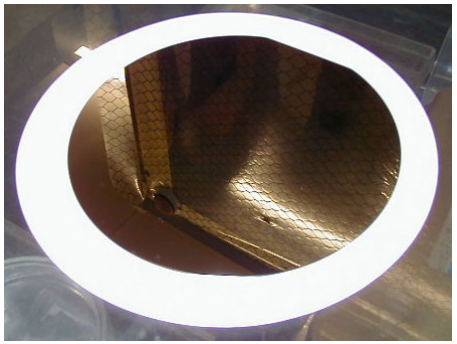
Advantages of single crystal Si

- Low cost
  - Main constituent elements of the earth
  - Low production cost
- Easy processing
  - Easy to purify (Si atoms are strongly bonded together.)
  - Large-diameter single crystal(*)
  - High mechanical strength
  - High melting point ~1410 degrees Celsius
- Good homogeneity
  - Highly level of uniformity of MOSFET characteristics

  - **Single crystal: A material in which the crystal lattice of the entire sample is continuous and unbroken to the edges of the sample, with no grain boundaries.**

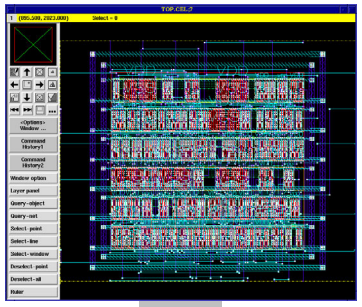


Si ingots



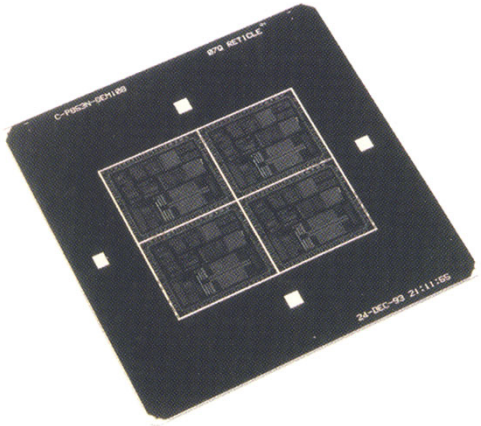
Si wafer

Outline of process flow



Design data

Photomask



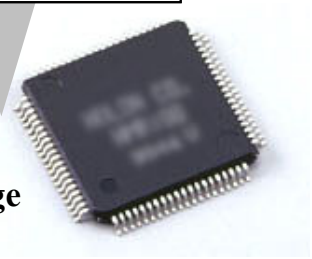
Photomask (Reciticle) :
an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. They are commonly used in photolithography.

Microfabrication
（微細加工）

Test（良品選別）

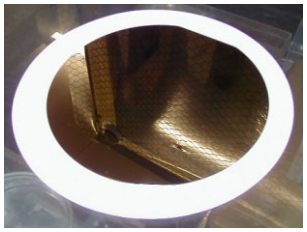
Dicing（チップ切断）

Packaging

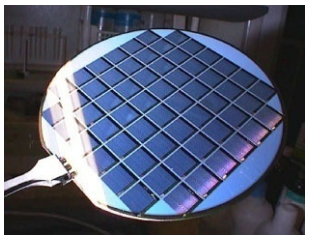


Package

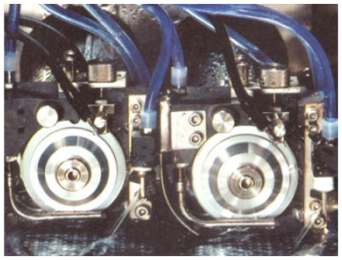
Si wafer



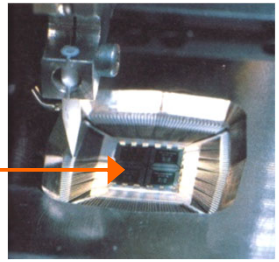
Si wafer



Processed wafer



Dicing



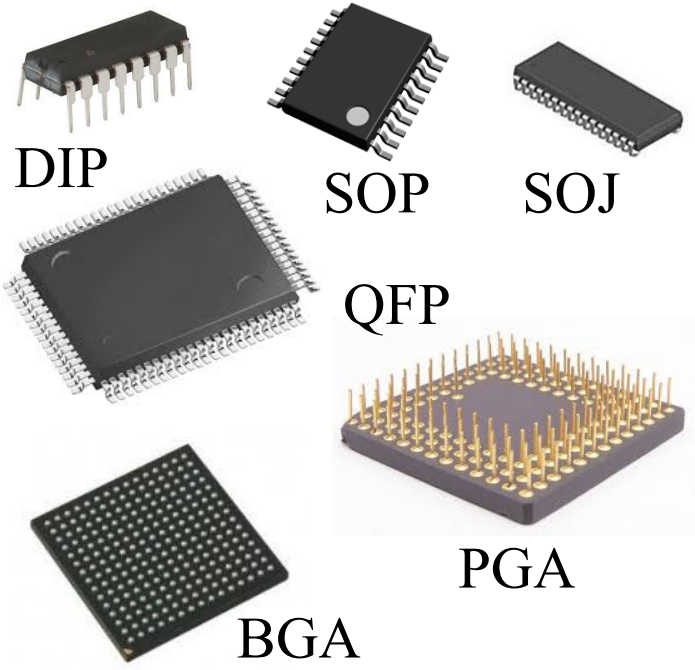
Chip

Wire bonding

LSI packages

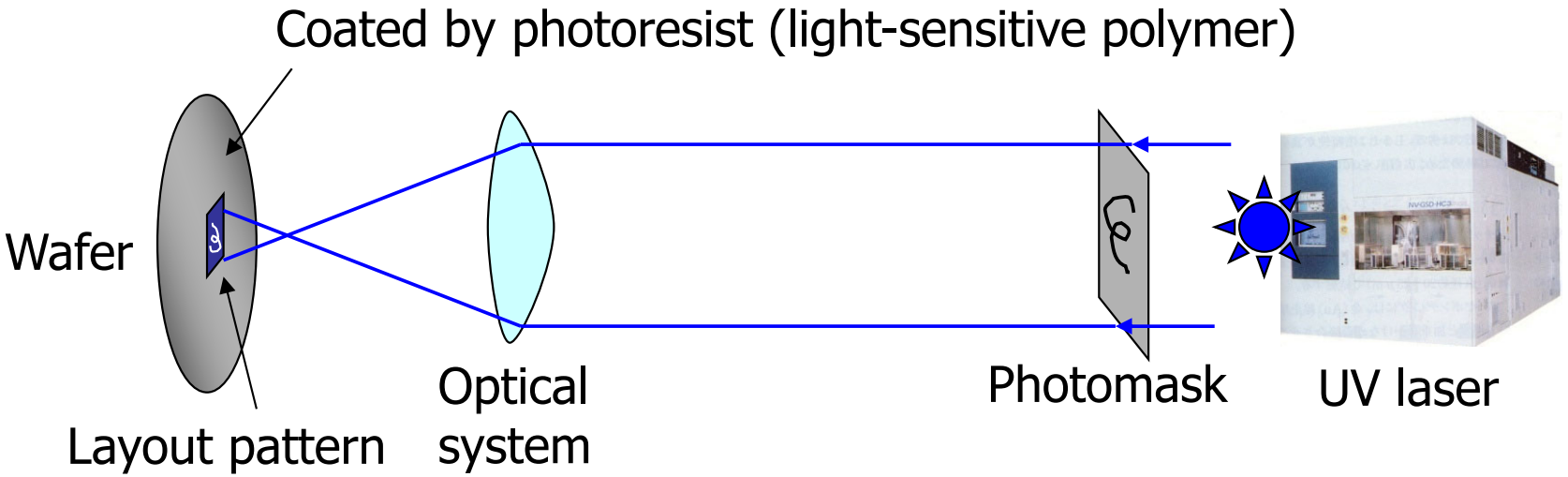
The circuit simulation or the electromagnetic field analysis of the chip including the package is performed for the high-speed or RF IC.

High-pin-count

Abbrevi-ation	Name	Pictures
DIP	Dual in-line package	
SOP	Small out-line package	
SOJ	Small out-line J-lead package	
QFP	Quad flat package	
PGA	Pin grid array	
BGA	Ball grid array	
CSP	Chip size package	

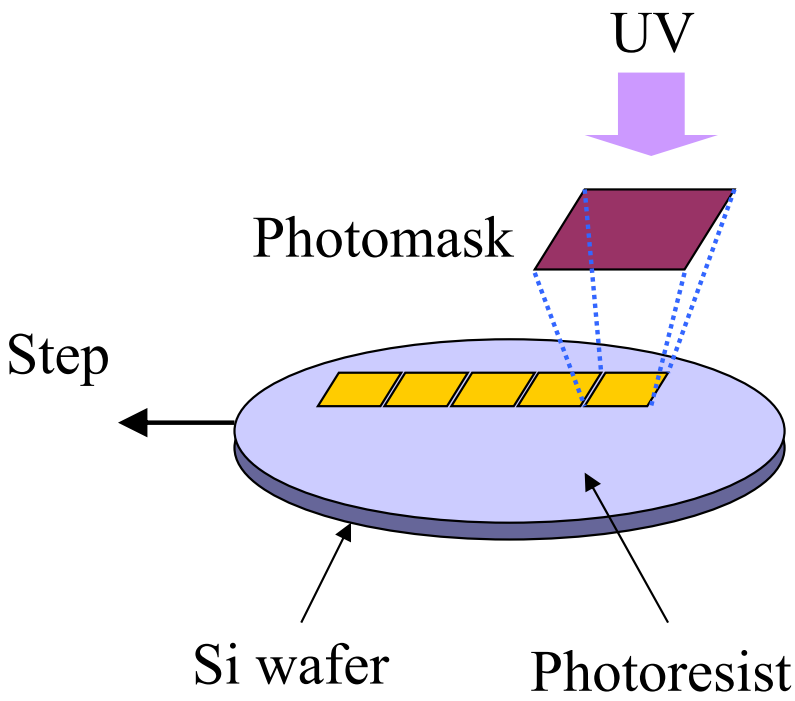
Photolithography

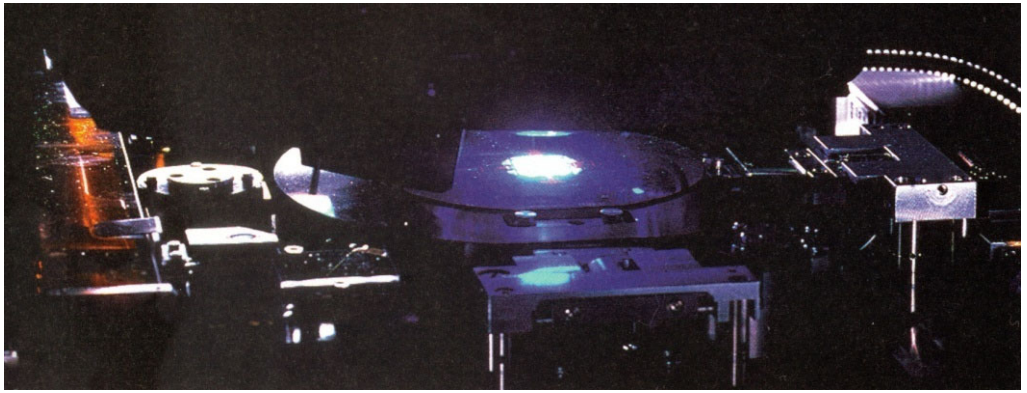
- The mask features are on a larger scale (e.g. 4X or 10X) relative to the features exposed on the wafer surface.
- The reduced size projection is accomplished with a projection stepper.



Stepper

- The pattern of the chip is transferred, and the array of the chip is formed on the entire surface of the wafer by step-and-repeat method.



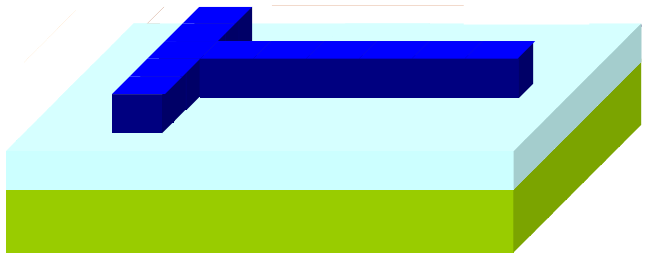


Stepper

Principle of microfabrication 1

- Backend-of-the-line (Interconnect)

Animation



Metal
Dielectric
Si wafer

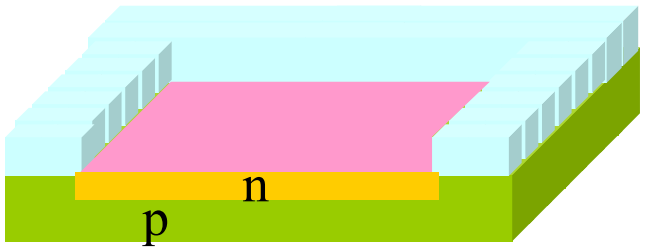
- Pre-metal dielectric deposition
- Metal film deposition
- Photoresist coating
- UV irradiation through photomask
- Developing (Metal definition by the photoresist pattern)
- Metal etching by reactive ion
- Photoresist plasma ashing

Complete

Principle of microfabrication 2

- Frontend-of-the-line (pn junction)

Animation



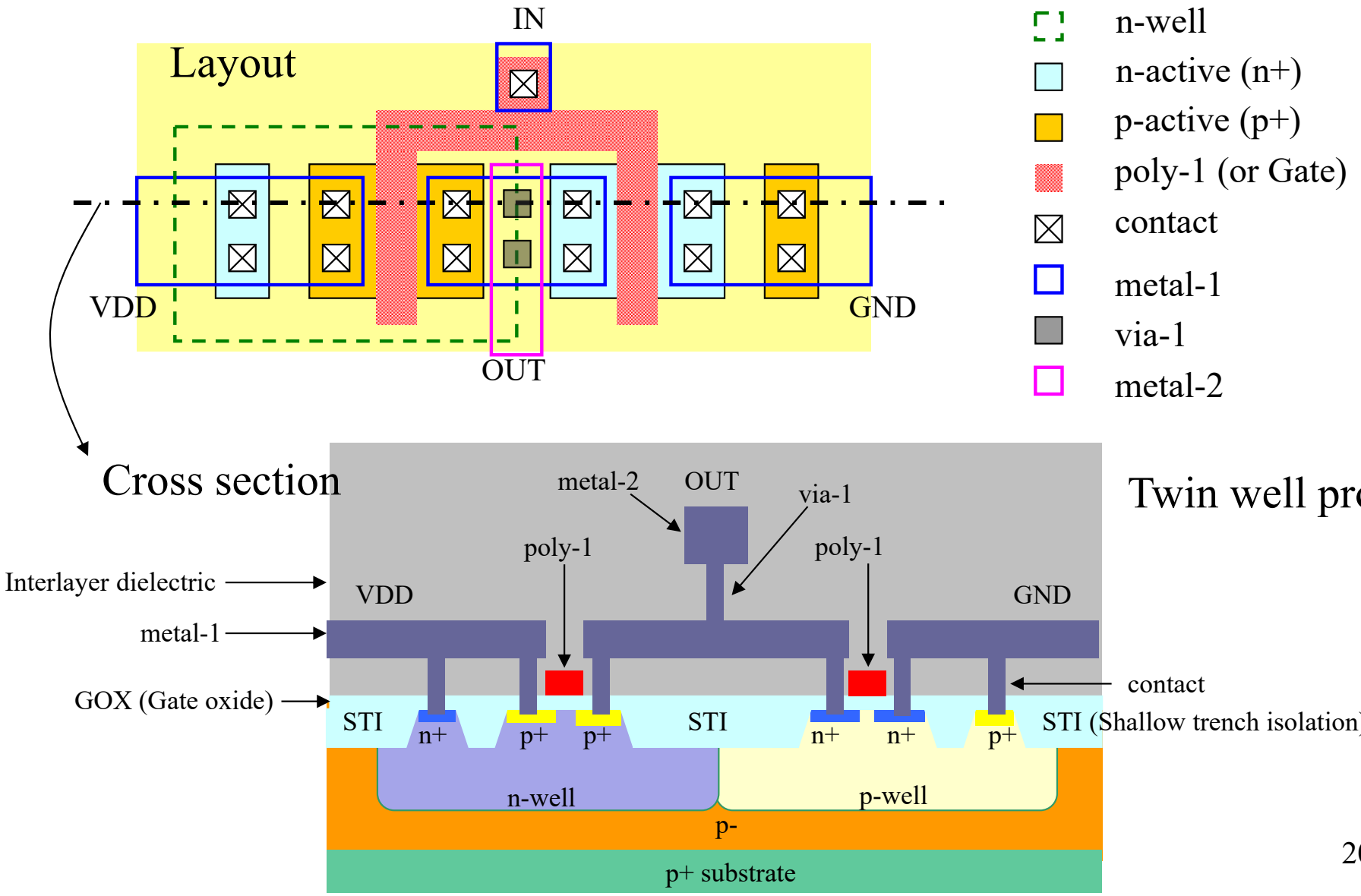
Dielectric
Si wafer

- Dielectric deposition
- Photoresist coating
- UV irradiation through photomask
- Developing (n+ definition)
- Dielectric etching by reactive ion
- Photoresist plasma ashing
- Ion implantation
- Annealing (Impurity activation)

Complete

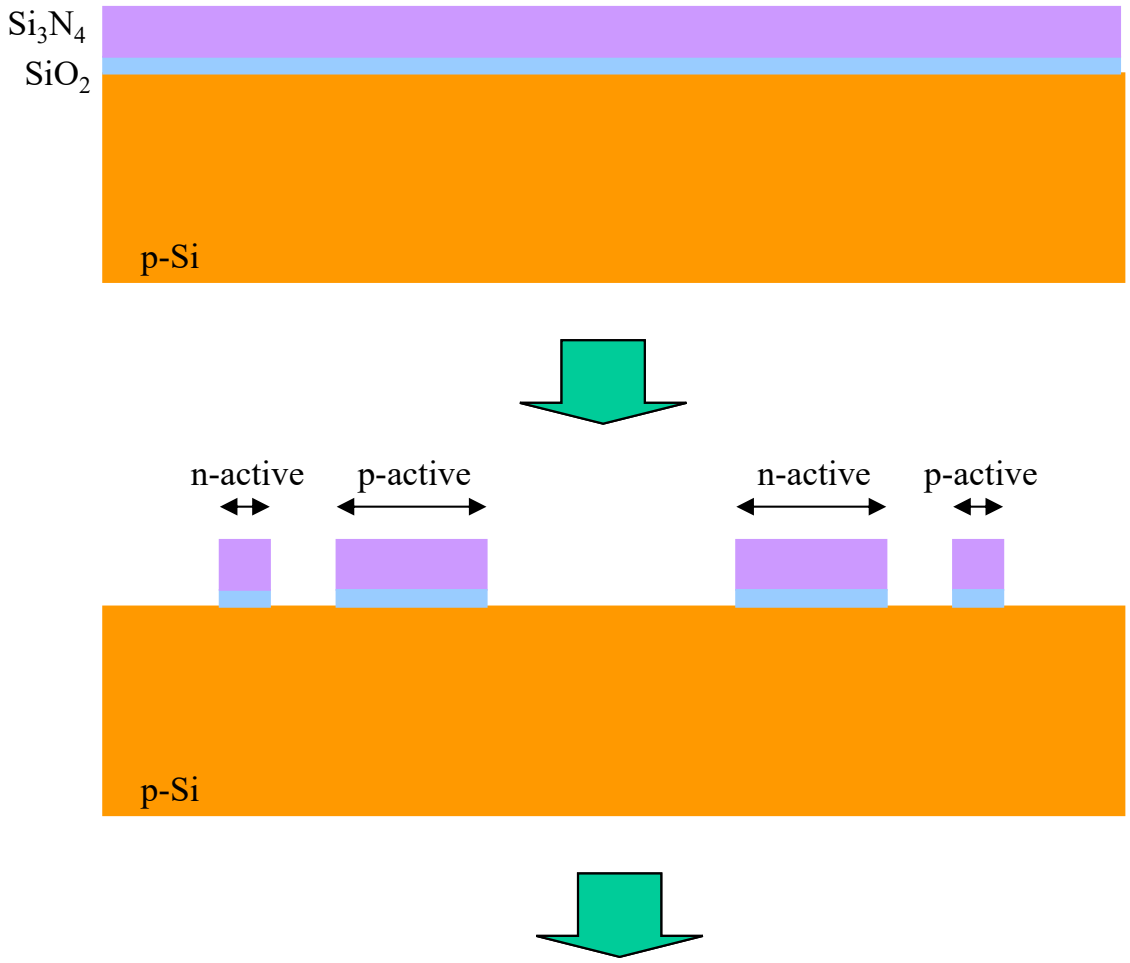
5.1.3 CMOS Process integration

Design example of inverter



Shallow trench isolation module 1

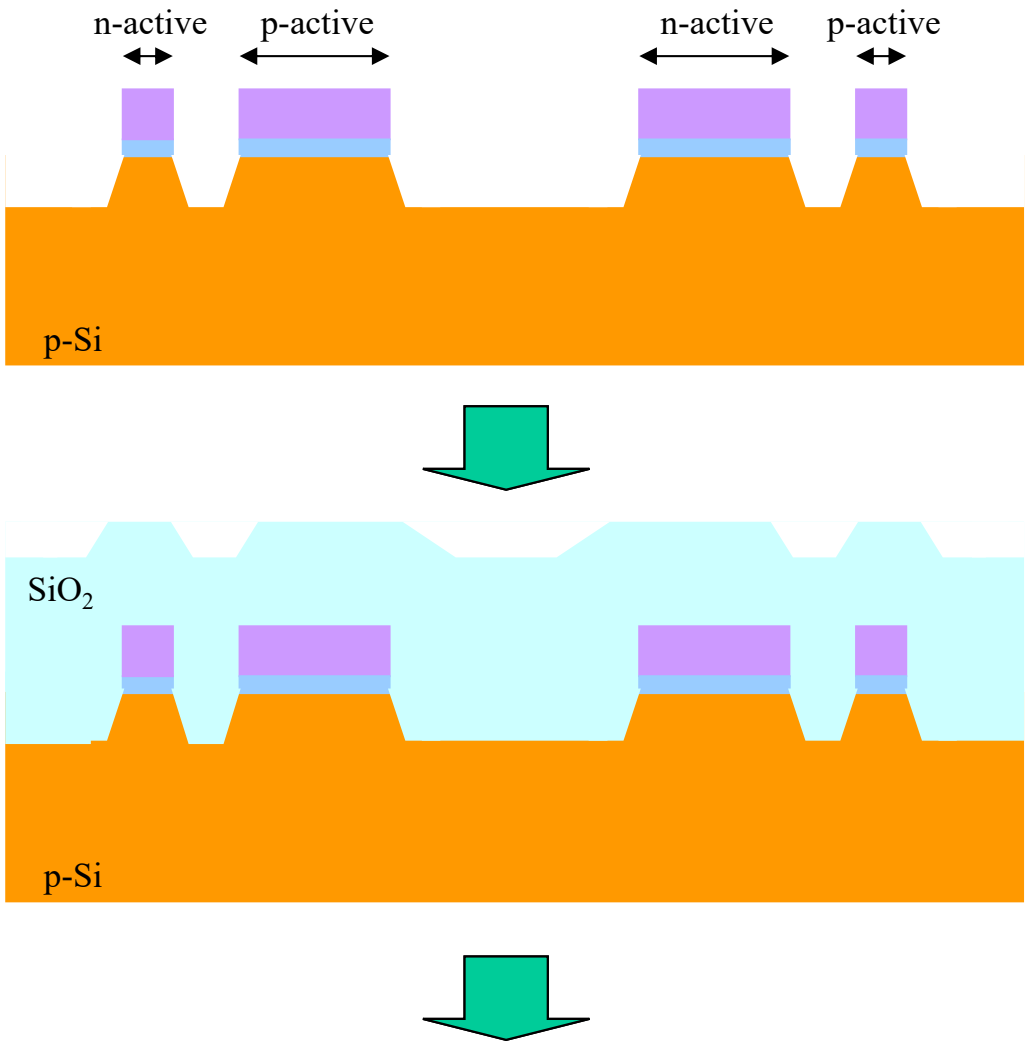
Process flow



p-/p+ Epitaxial grown layer on bulk Si (p-Si),
Deposition of Si_3N_4/SiO_2
(The SiO_2 is thermally grown.)

Active area definition by Si_3N_4/SiO_2

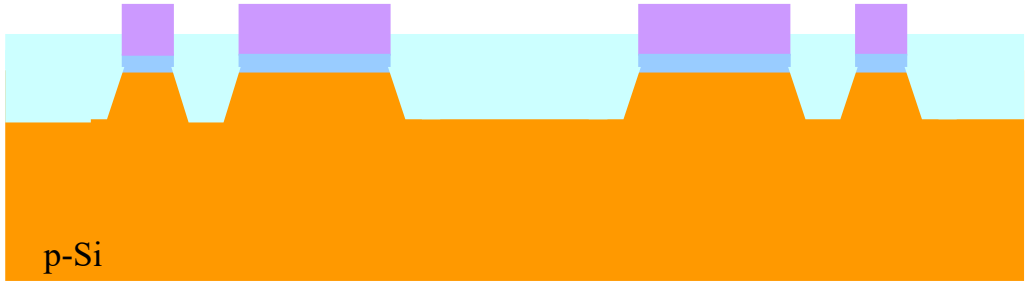
Shallow trench isolation module 2



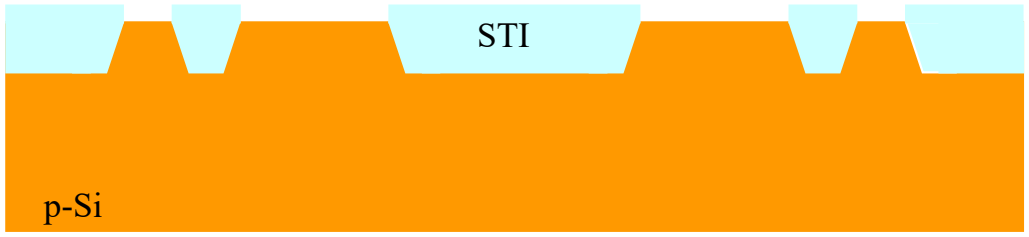
Timed silicon trench outside of Si_3N_4/SiO_2 by reactive ion etching

SiO_2 deposition

Shallow trench isolation module 3

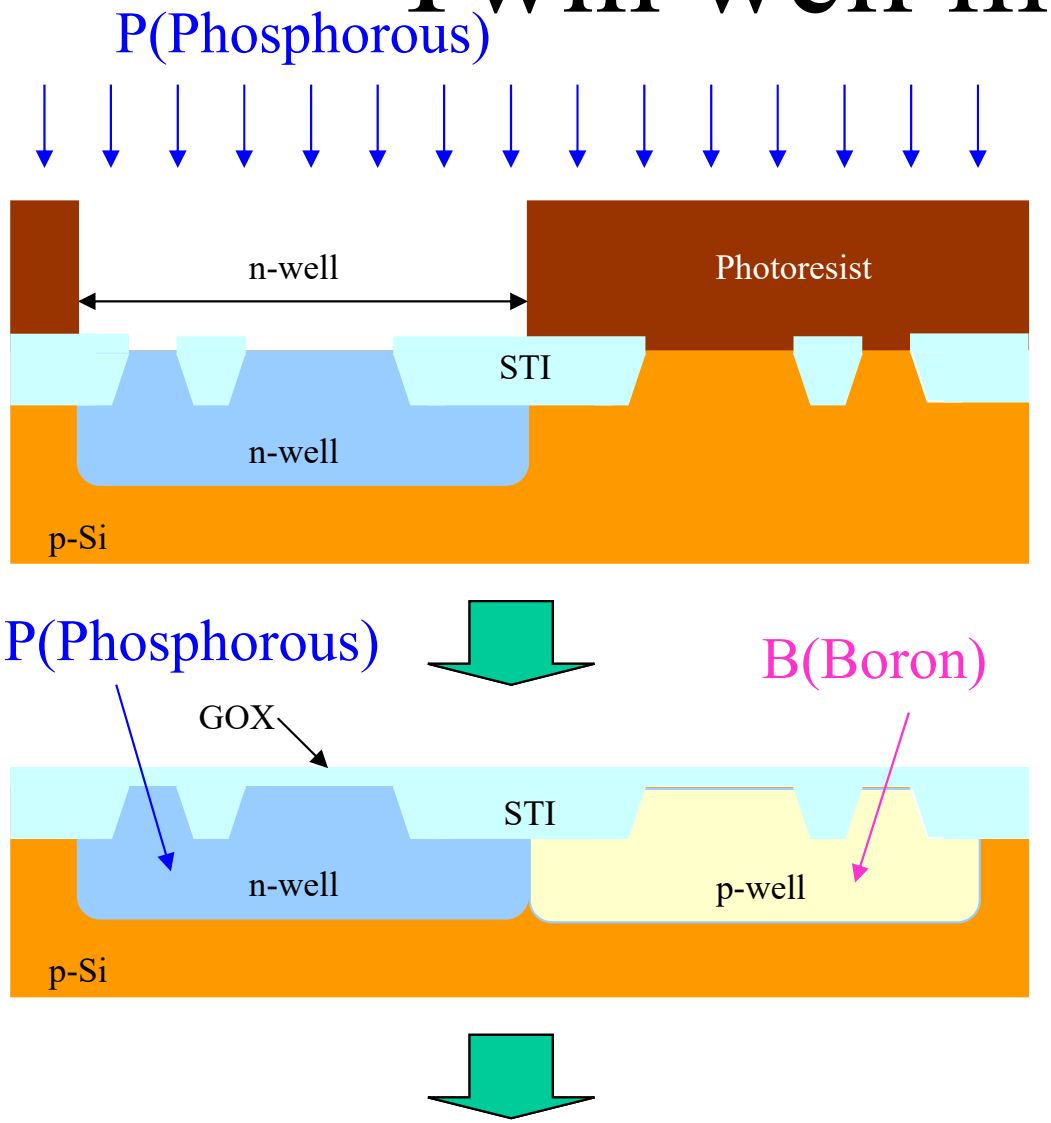


Removal of Si_3N_4/SiO_2 using CMP (Chemical-Mechanical Polishing)



Si_3N_4/SiO_2 etching STI (Shallow Trench Isolation) is formed.

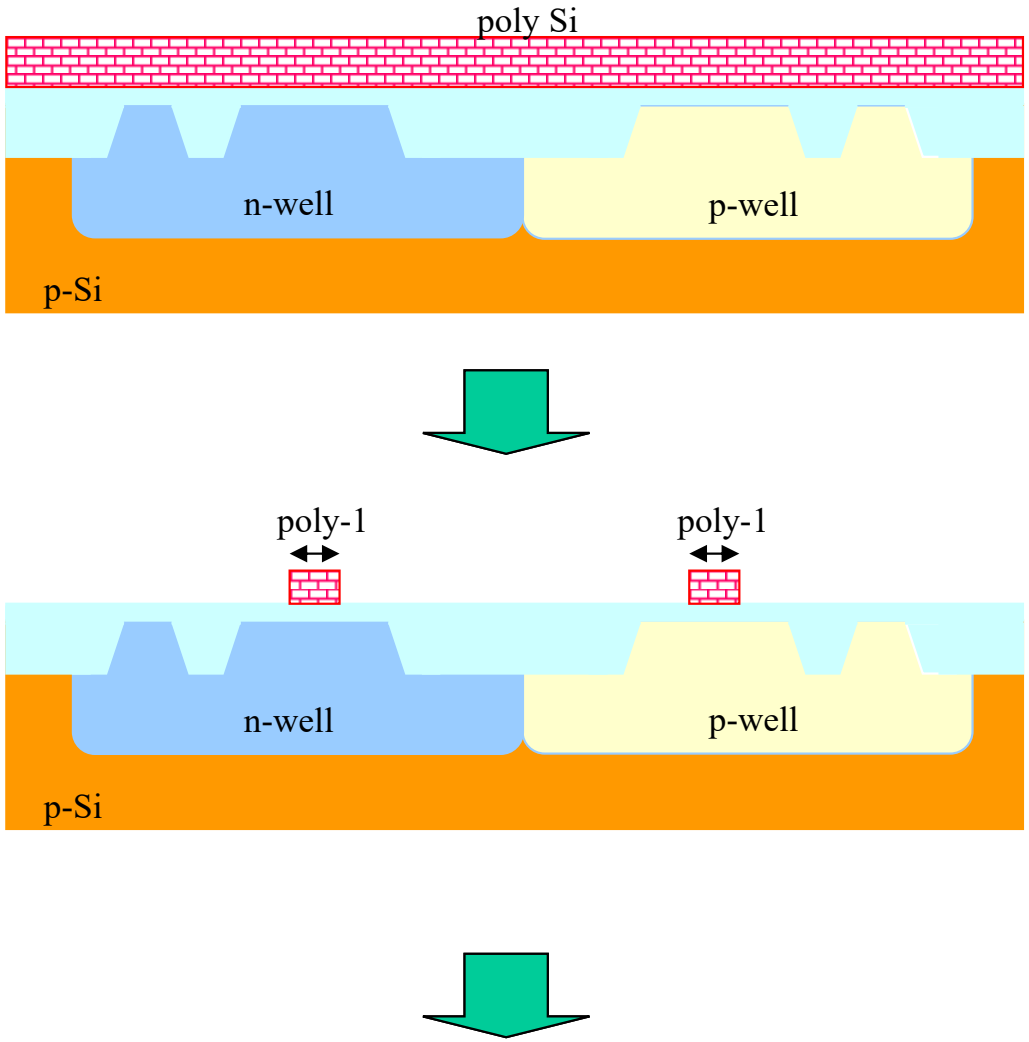
Twin well module



n-well definition by photoresist,
Phosphorus implantation,
Photoresist plasma ashing,
Drive-in diffusion of phosphorous,
p-well formation in the same way of n-well

Gate dielectric (GOX) formation using dry oxidation

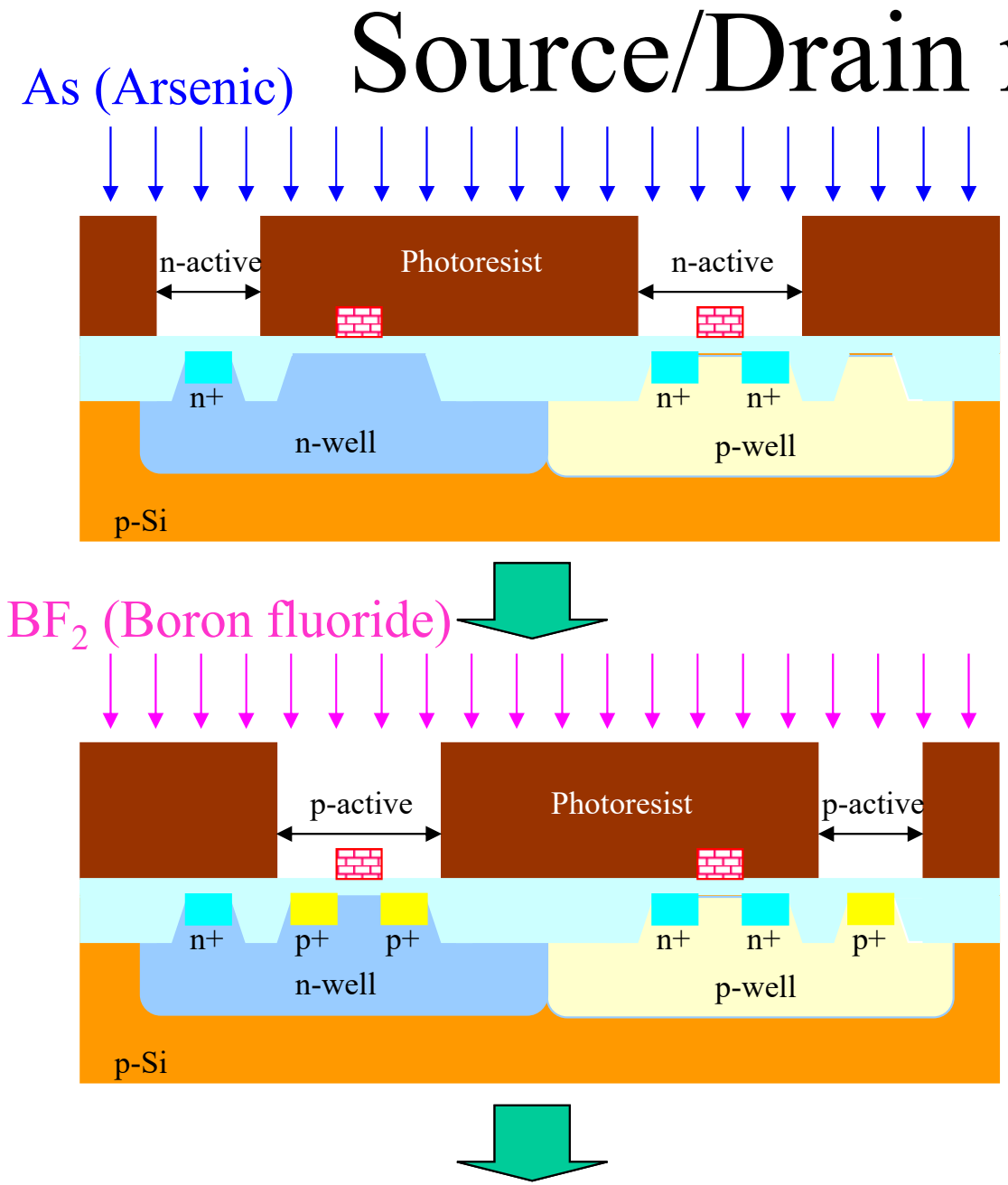
Gate module



Polysilicon deposition

Gate electrode and local interconnect photolithography and polysilicon reactive ion etching

Source/Drain module

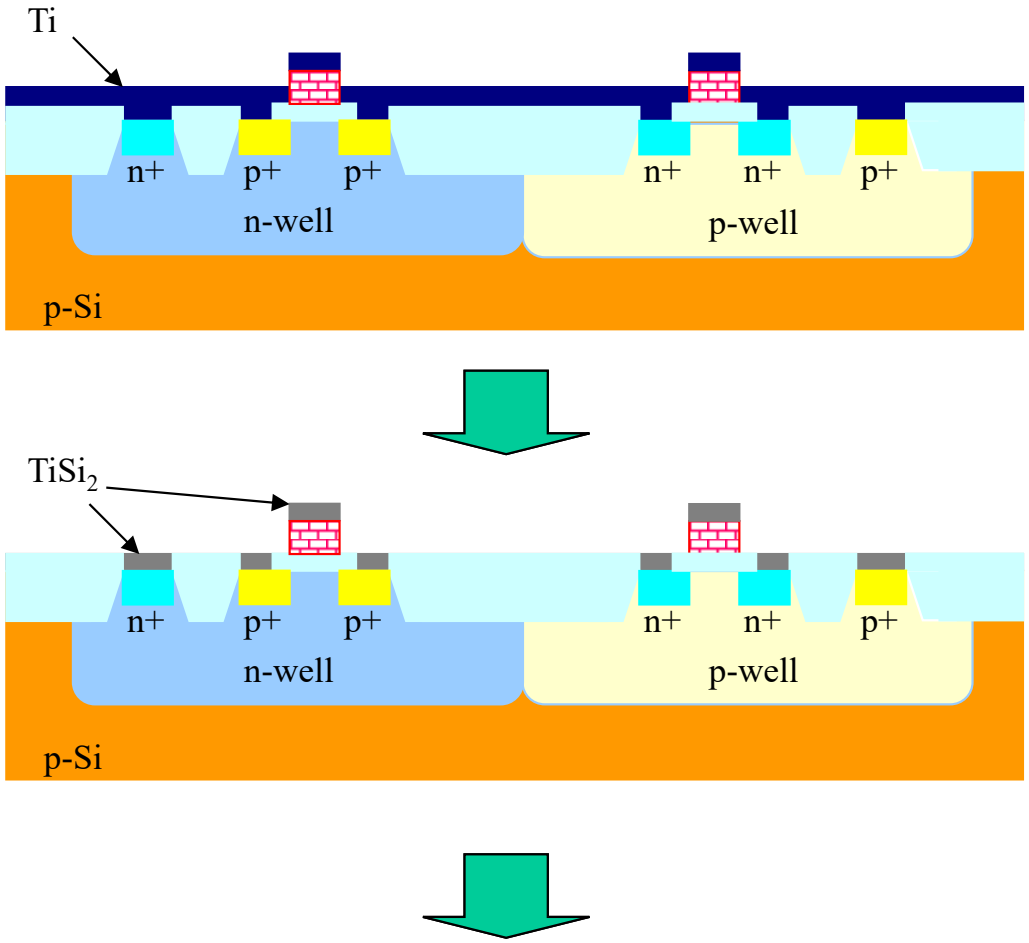


n+ source/drain formation using a low energy, high dose implantation of As

The polysilicon blocks the implantation, and automatically source and drain are formed on both side of the gate (Self-Alignment process)

p+ source/drain formation using a low energy, high dose implantation of BF_2

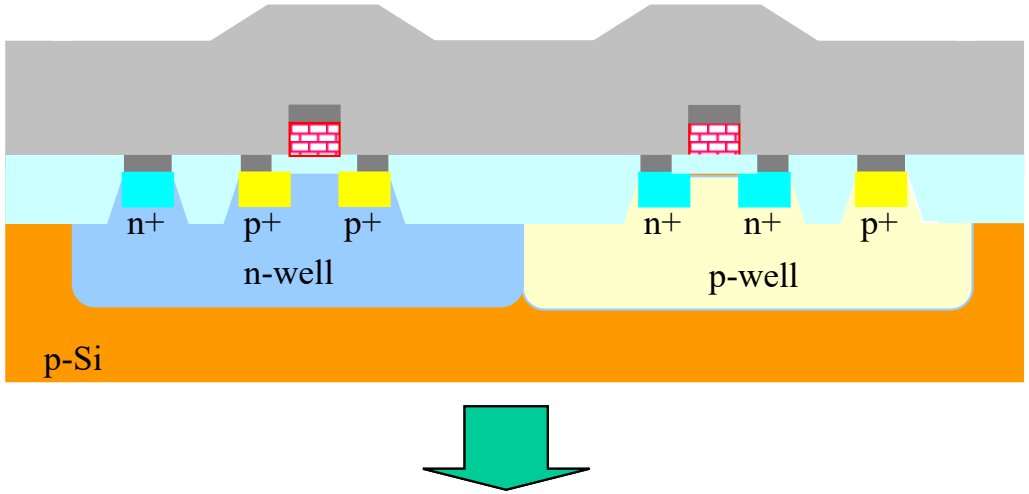
Self-aligned silicide module



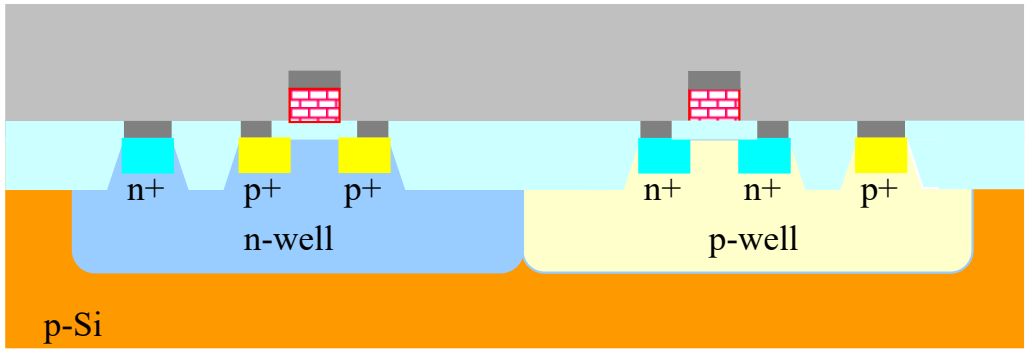
Removal of the oxide on the source and the drain,
Ti（チタン）deposition

Low resistivity $TiSi_2$（チタン・シリサイド）is formed by RTA (Rapid thermal annealing),
Removal of Unreacted Ti,
Self-aligned silicide = Silicide process

Pre-metal dielectric

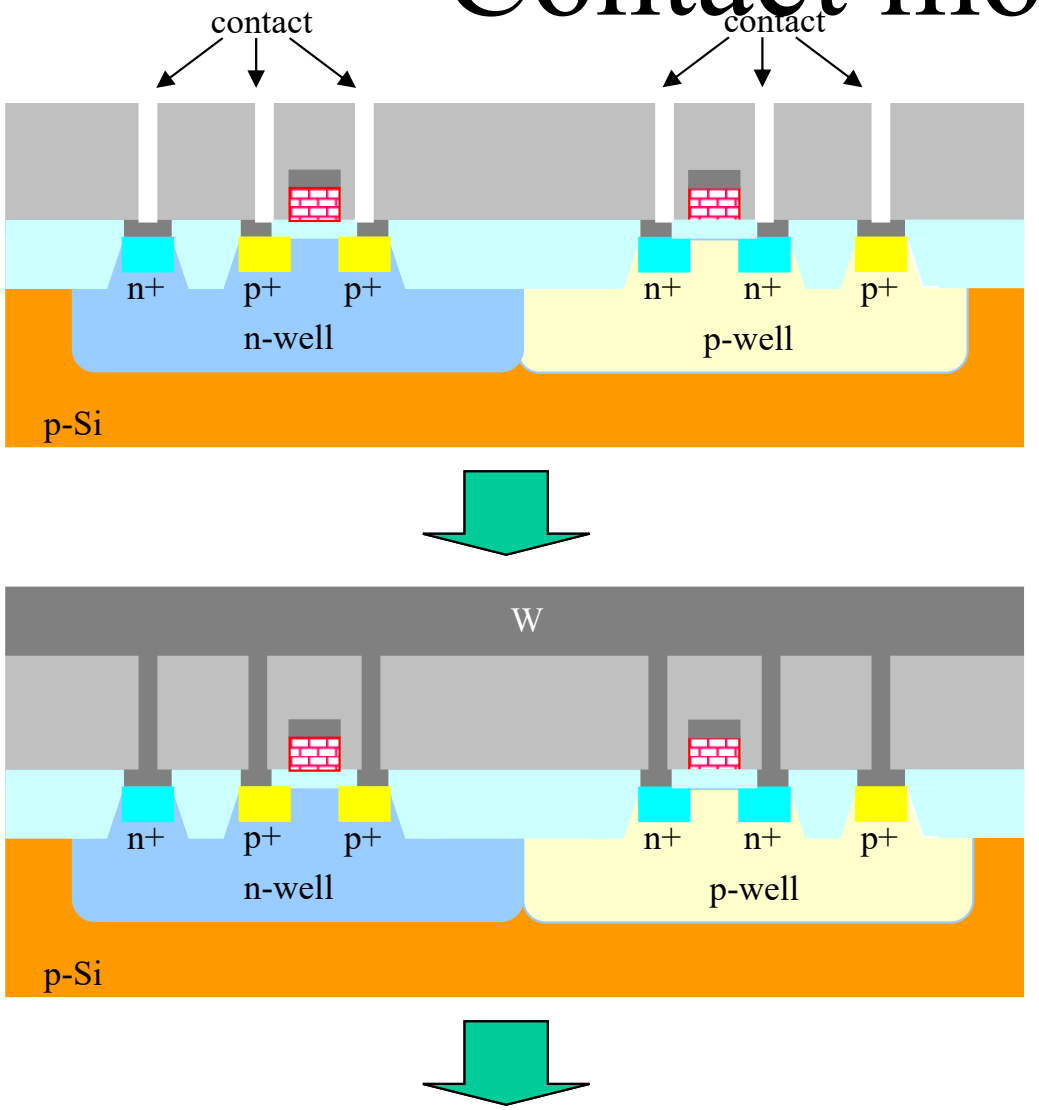


SiO_2 or PSG (Phosphosilicate glass) deposition,
This layer is called PMD (Pre-metal Dielectric).



Planarization using CMP (Chemical-Mechanical Polishing)

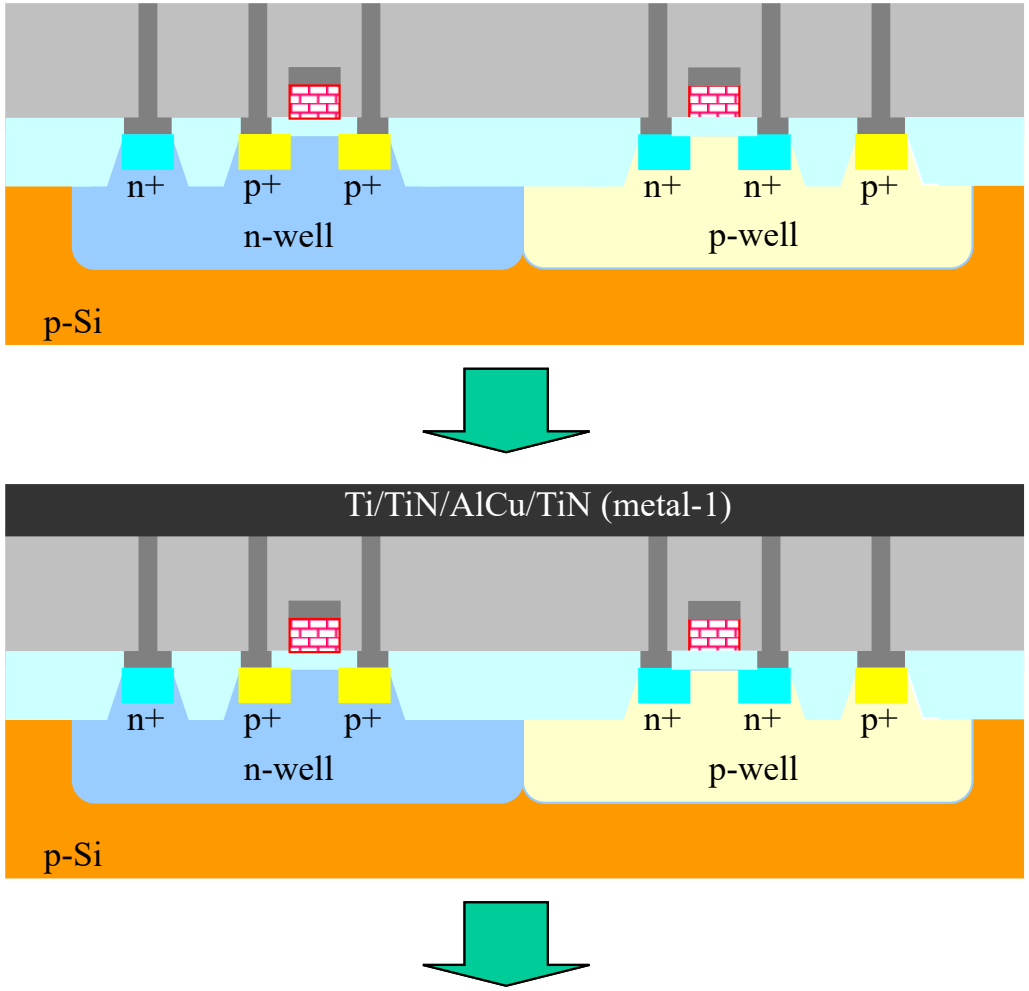
Contact module



Opening contact hole in the PMD layer

W（タングステン）deposition

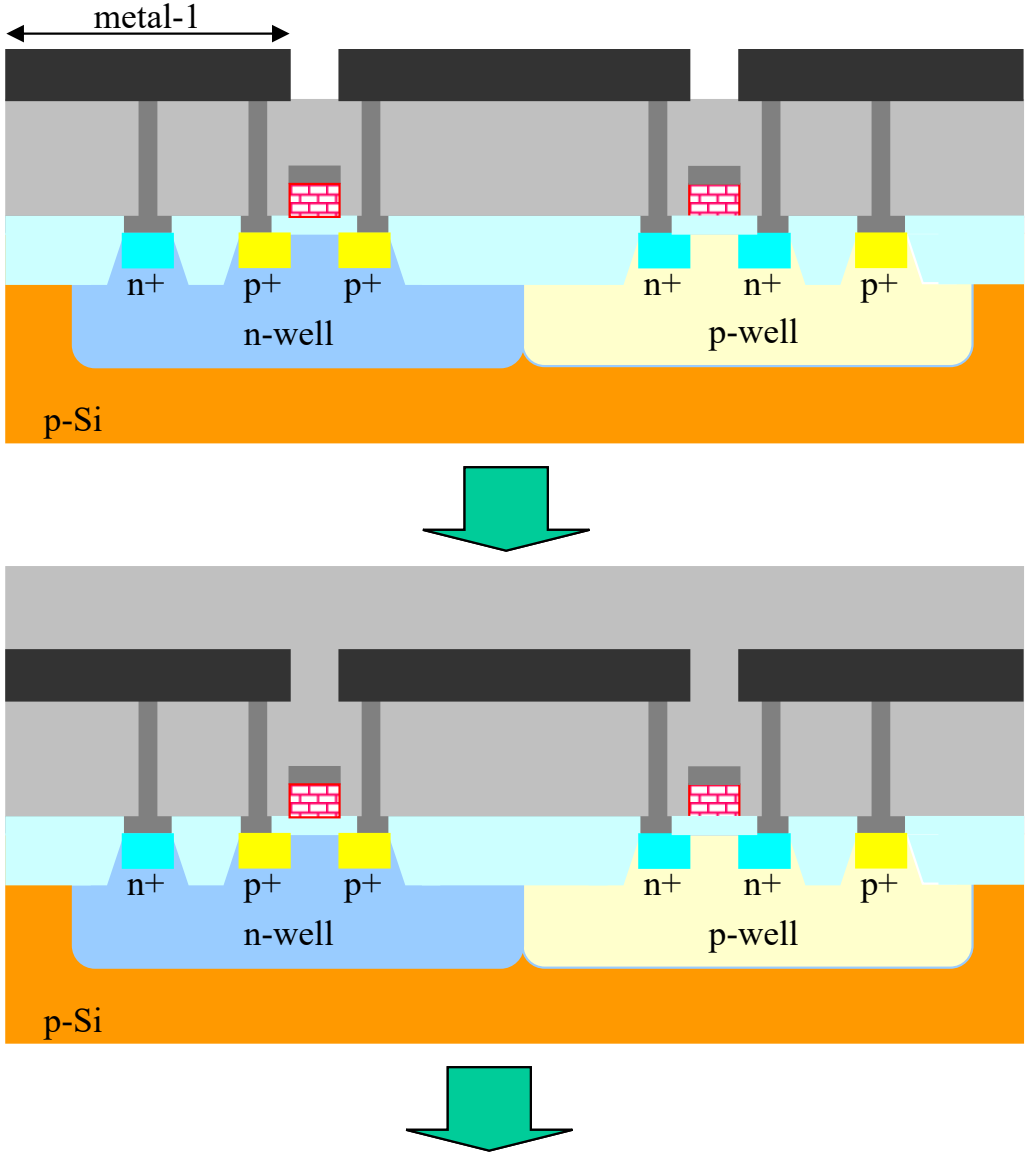
Metallization 1



W CMP to form defined contacts

Metal-1 stack deposition (Ti/TiN/AlCu/TiN)

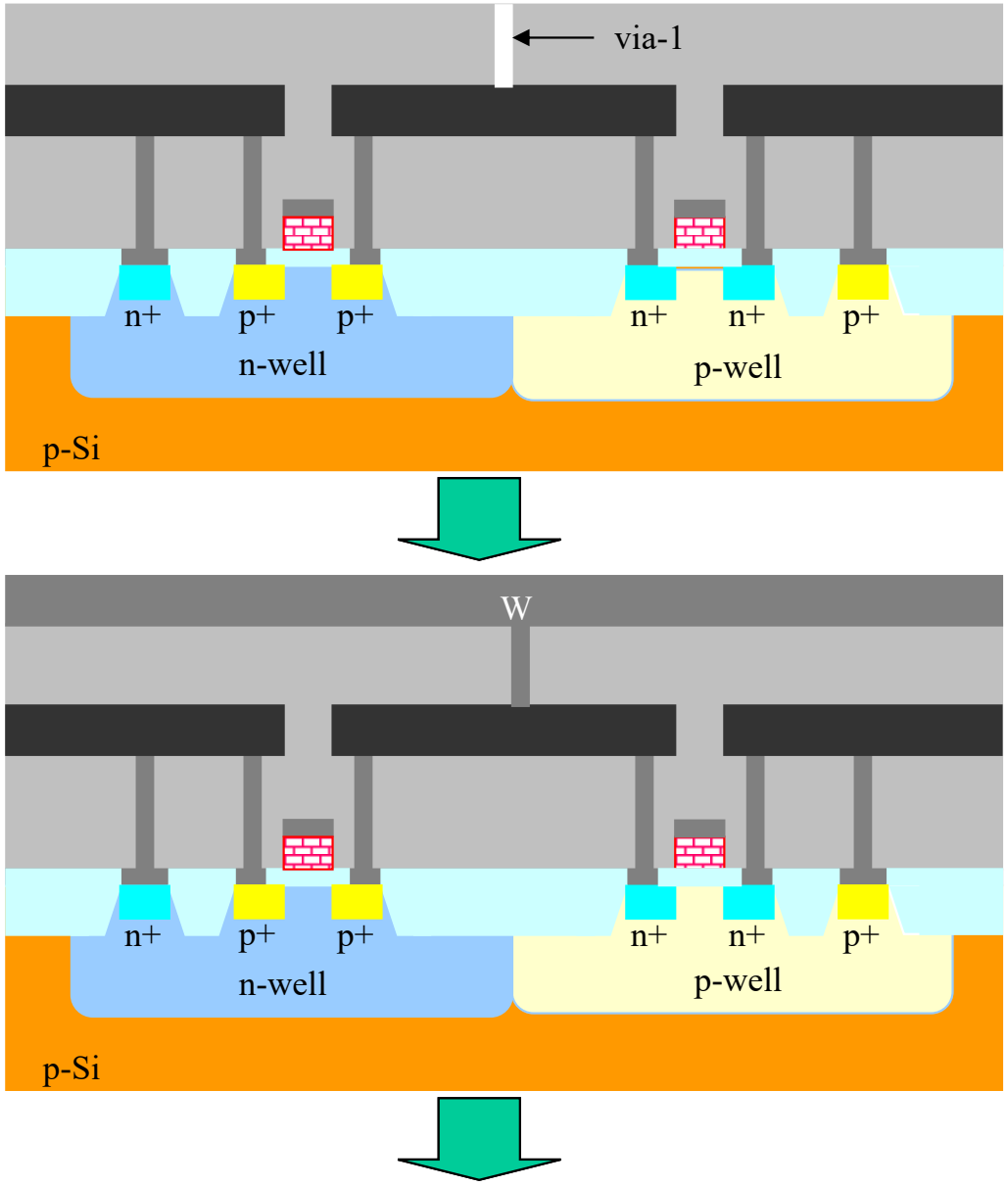
Intra-metal dielectric 1 deposition



Metal-1 definition using photolithography and dry metal etch

SiO_2 or BPSG (Boron-phosphoresce silicate glass) deposition (IMD: Intra-metal Dielectric), Planarization using CMP

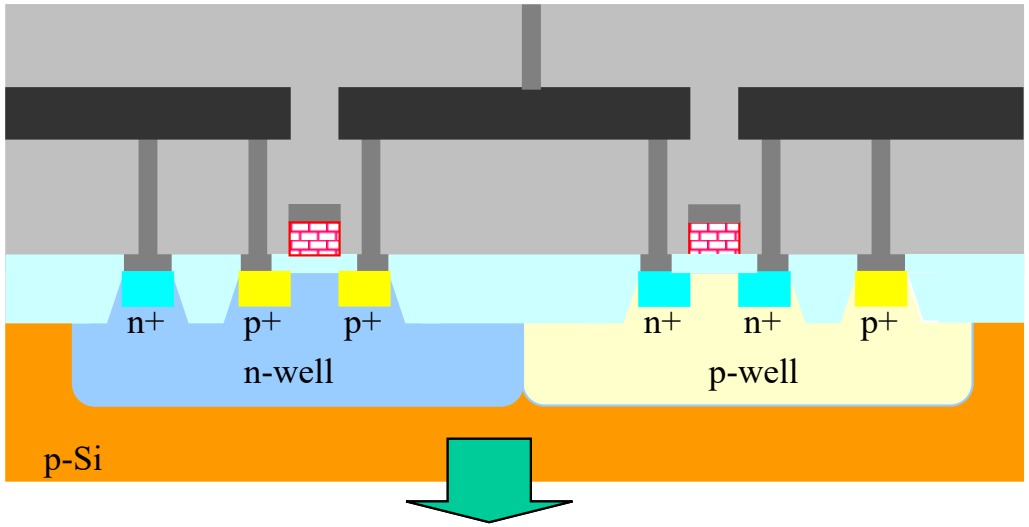
Via 1 module



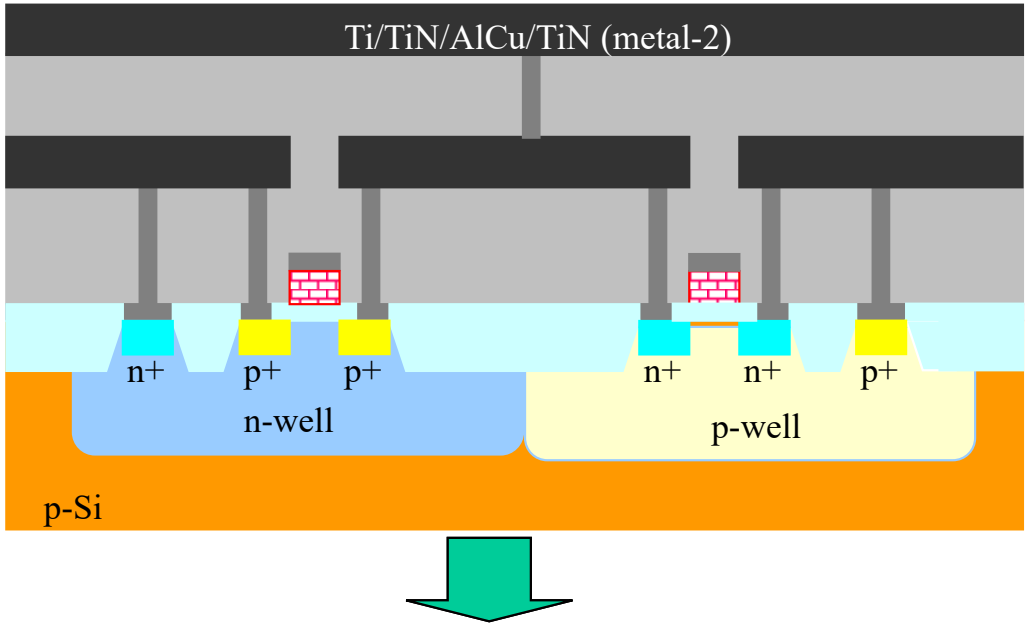
Via-1 definition using photolithograph and dry IMD etch

W via fill deposition

Metallization 2

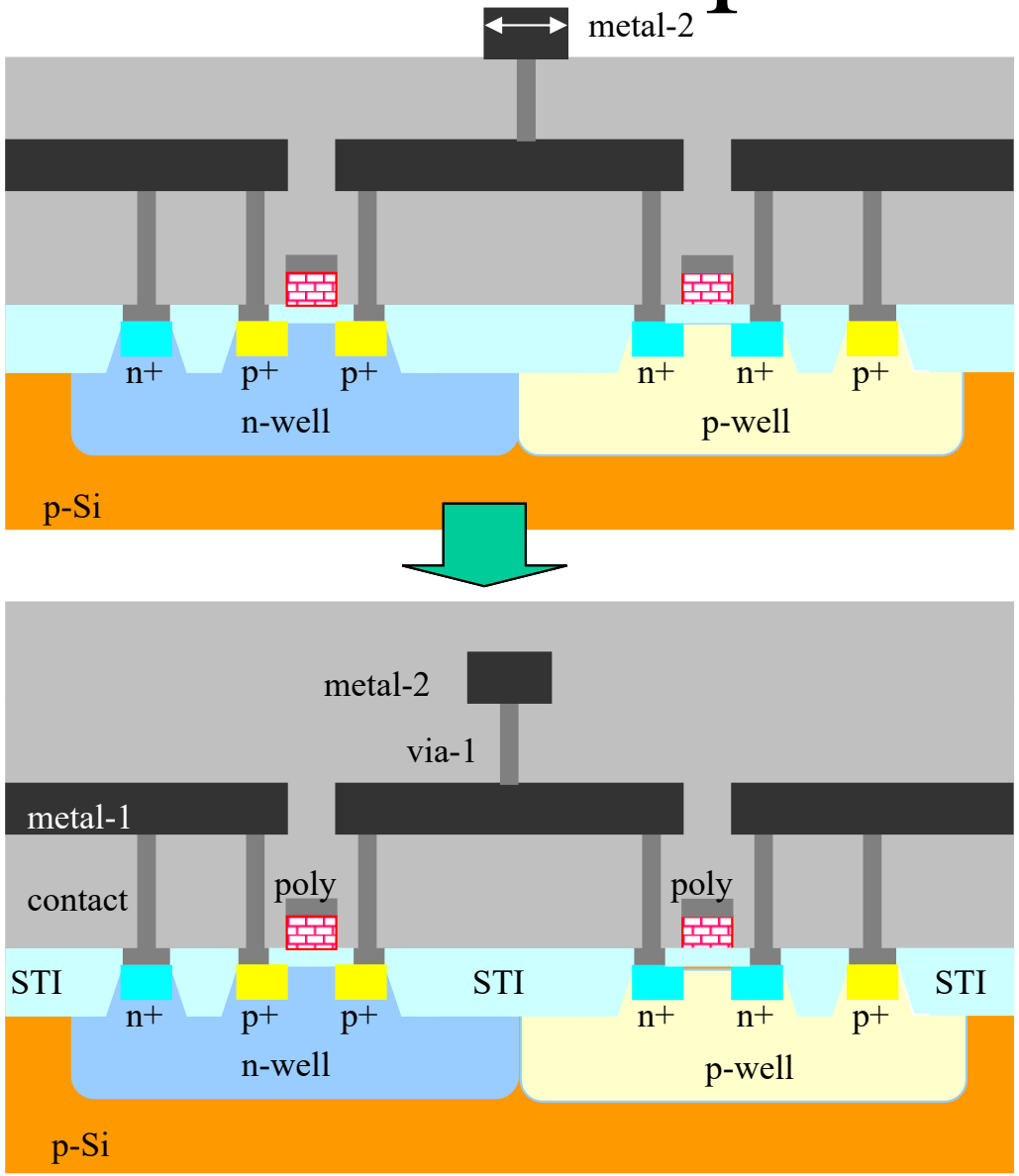


W CMP to form defined vias



Metal-2 stack deposition (Ti/TiN/AlCu/TiN)

Final passivation



Metal-2 definition using photolithography and dry metal etch

Deposition of passivation layer, Bond pad definition using dry etch of passivation film.

The actual process is more complicated in order to improve the electrical reliability.

Profiles of impurity concentration

The depth of pn junction is controlled by an acceleration energy of ion implantation and a time of drive-in diffusion.

$N_{eff} = N_D - N_A$

N_A : Concentration of accepters

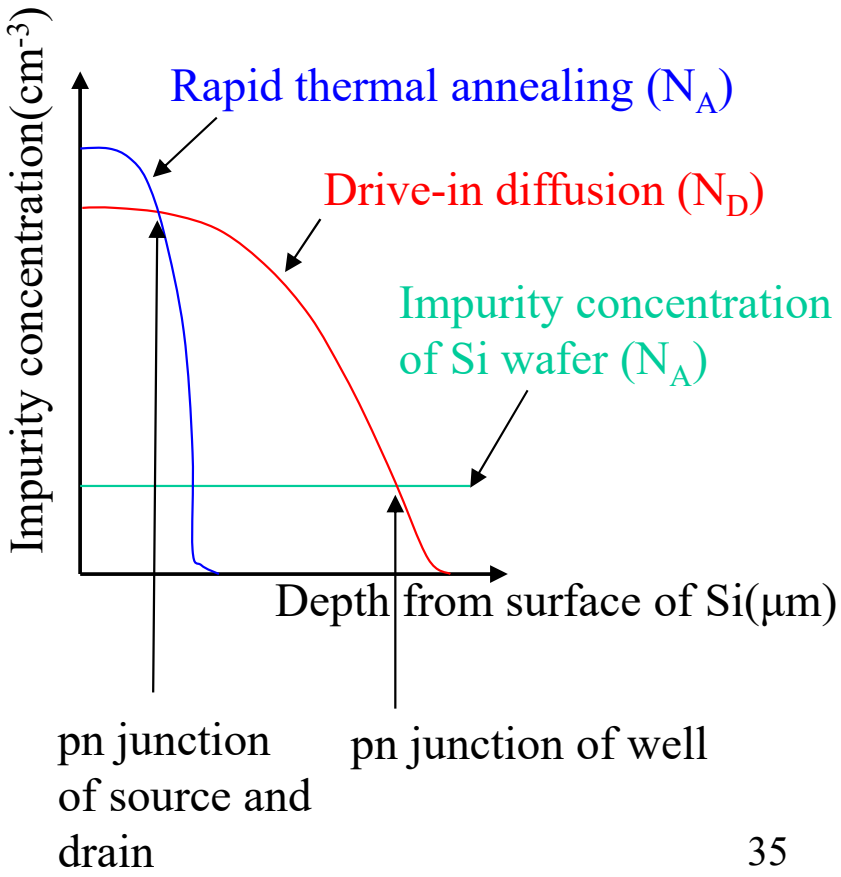
N_D: Concentration of donors

If both impurities of donor and accepter are doped,

If $N_{eff} > 0$, then n-type

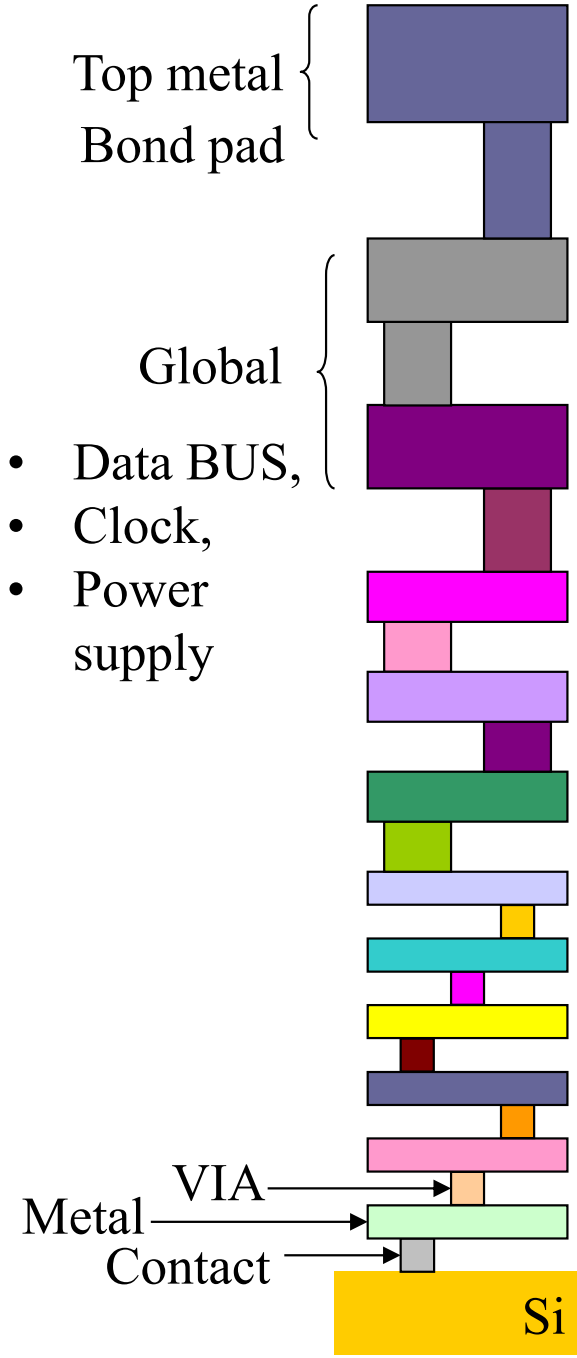
If $N_{eff} < 0$, then p-type

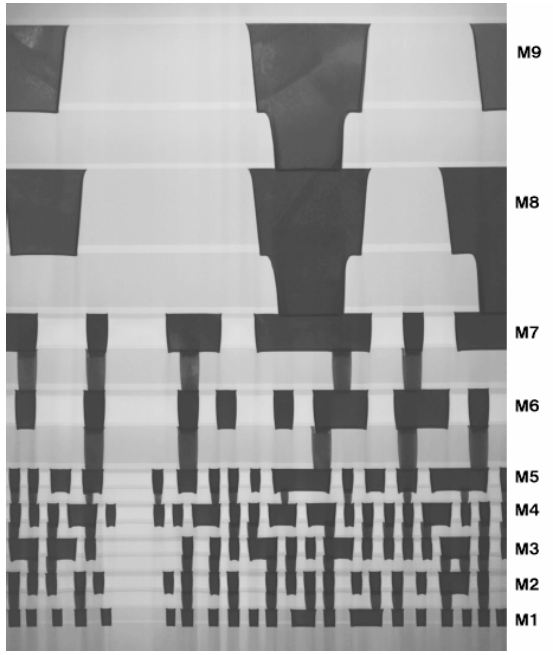
If $N_{eff} = 0$, then pn junction



5.1.4 Interconnect

Multilayer interconnection

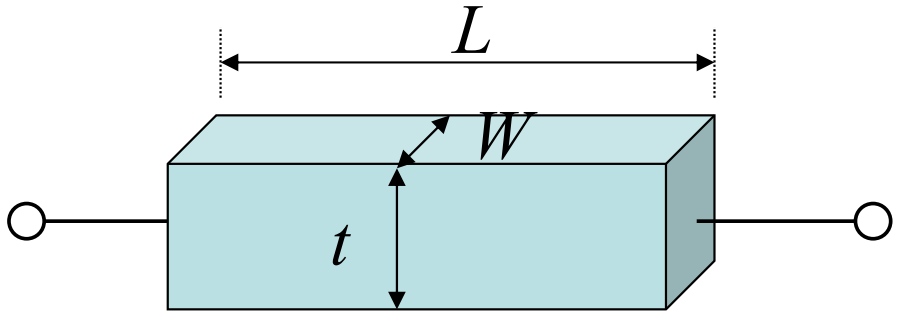




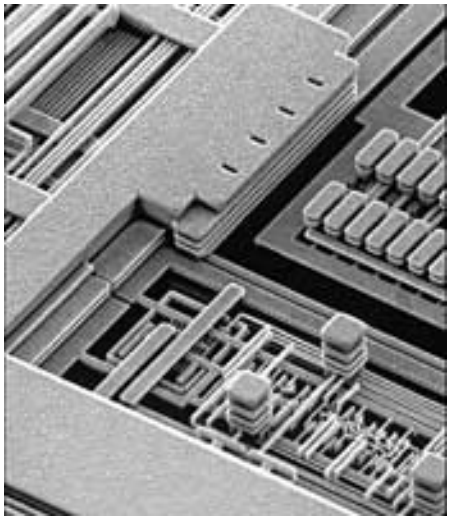
Electron micrograph of cross section

Example of 12-layer interconnect

Resistivity of metals



$$R = \rho \frac{L}{t \cdot W}$$ ρ(Ωm): Resistivity



0.2μm Cu interconnect
(Source: IBM)

$$E(\mathrm{V/m}) = \rho(\Omega m) J(\mathrm{A/m^2})$$

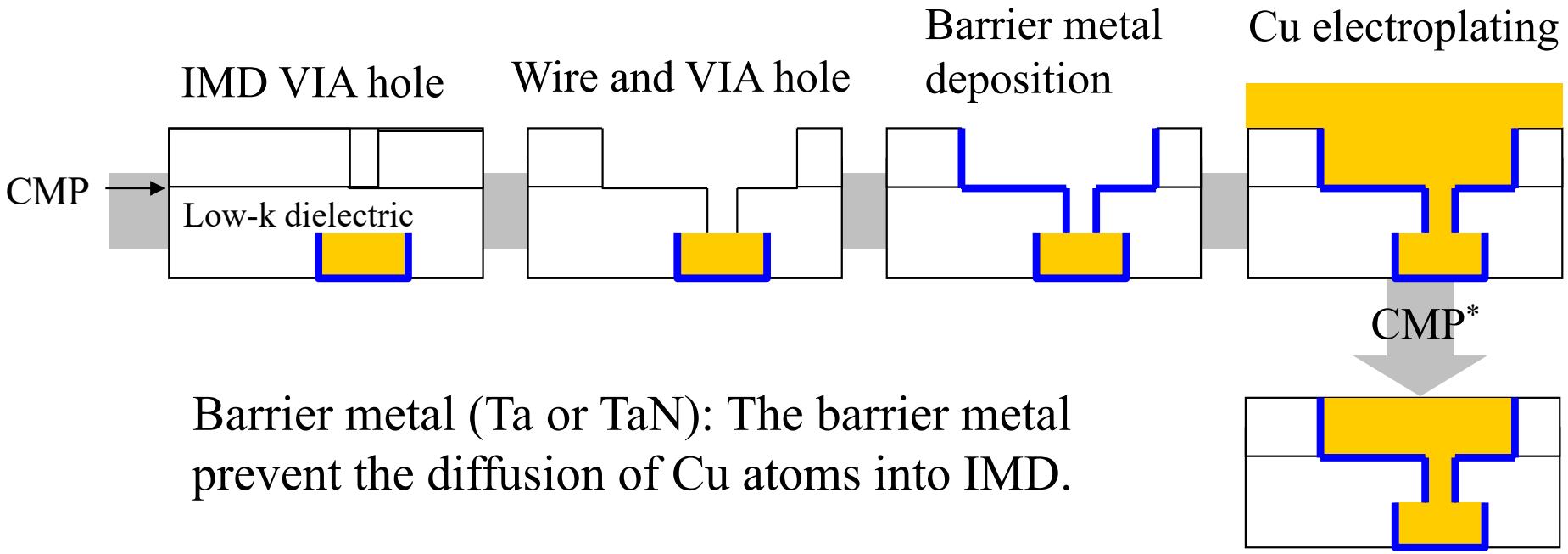
Material	Al	Cu
Resistivity ρ	3.3 μΩcm	2.23 μΩcm

Advantages of Cu wire

- Low resistivity
- High maximum current density

Dual damascene process

The performance of Cu wire is higher than the wire of Al, however, it is hard to process Cu wires by dry etching. The embedded Cu wire is formed by the dual damascene process.



Barrier metal (Ta or TaN): The barrier metal prevent the diffusion of Cu atoms into IMD.

* CMP (Chemical Mechanical Polishing : 化学機械的研磨)