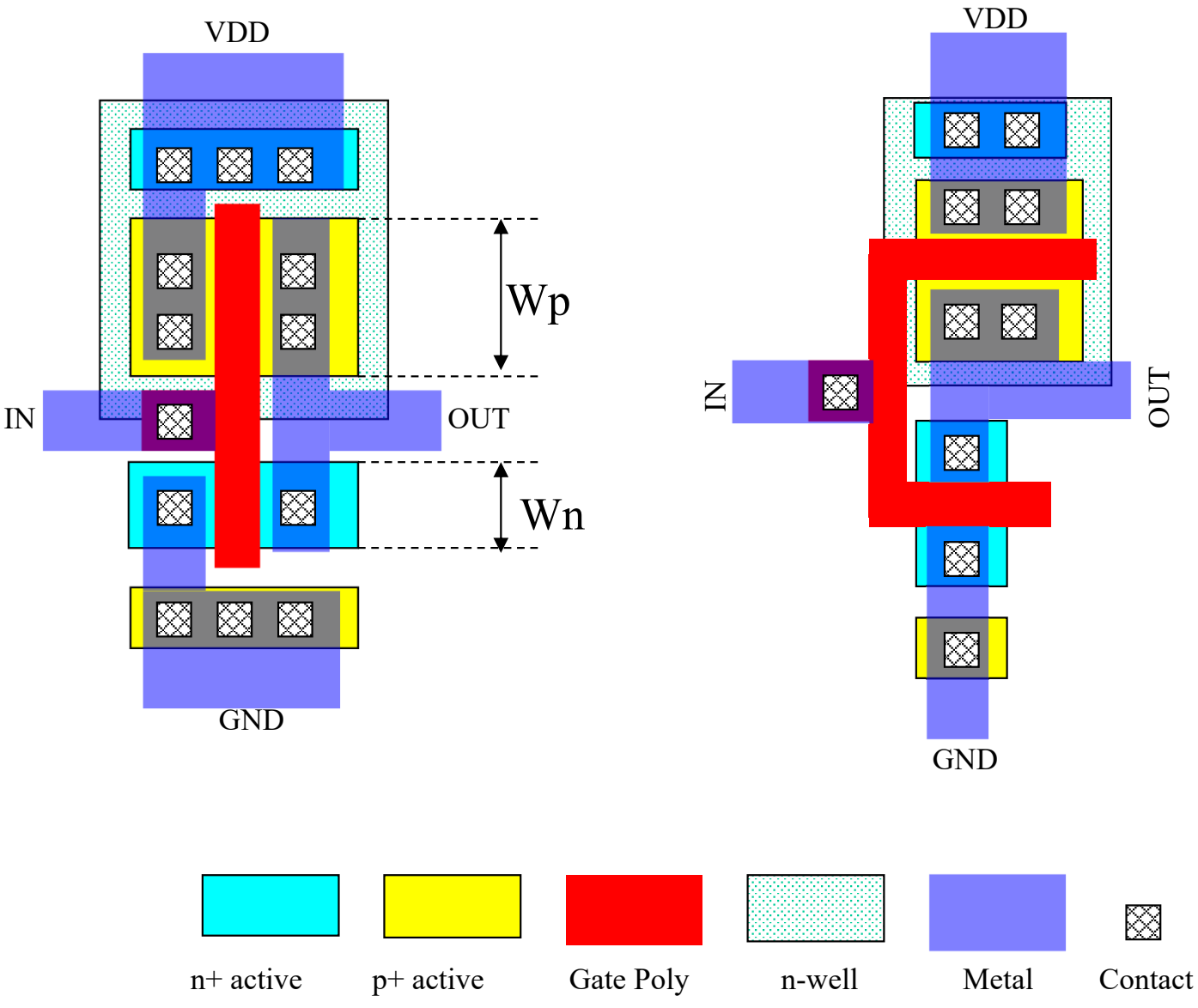
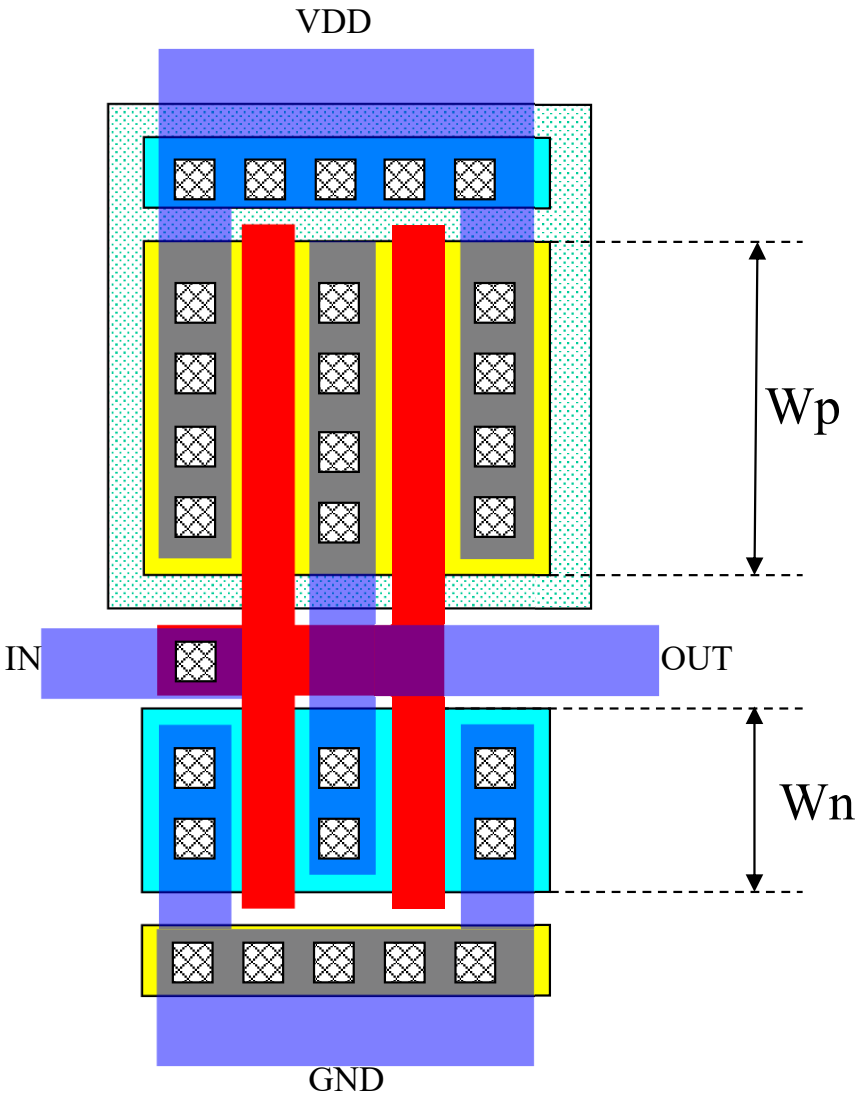
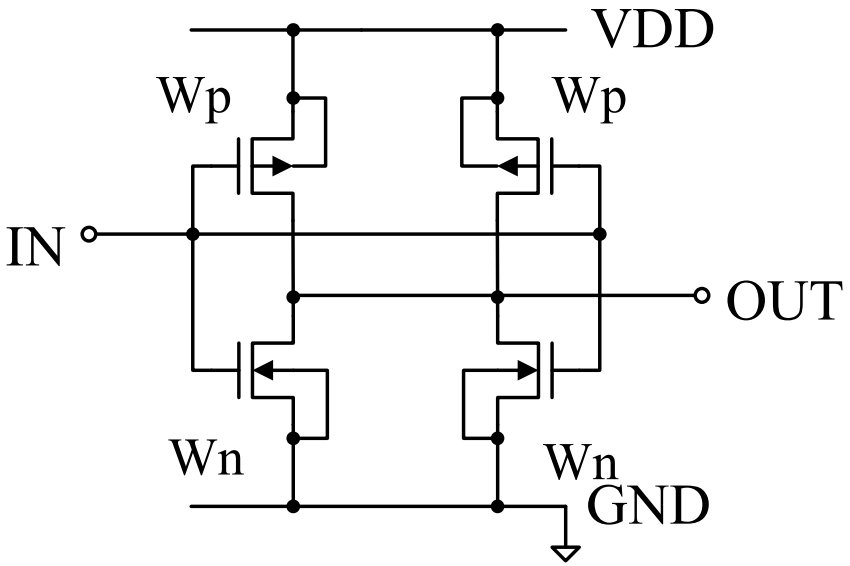
Layout example of inverter



Layout example of inverter (Large W/L)





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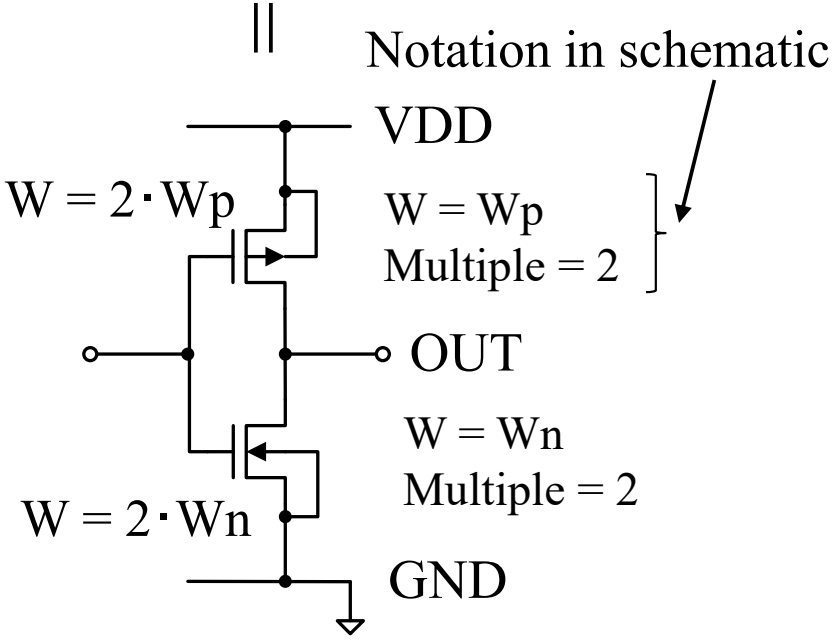
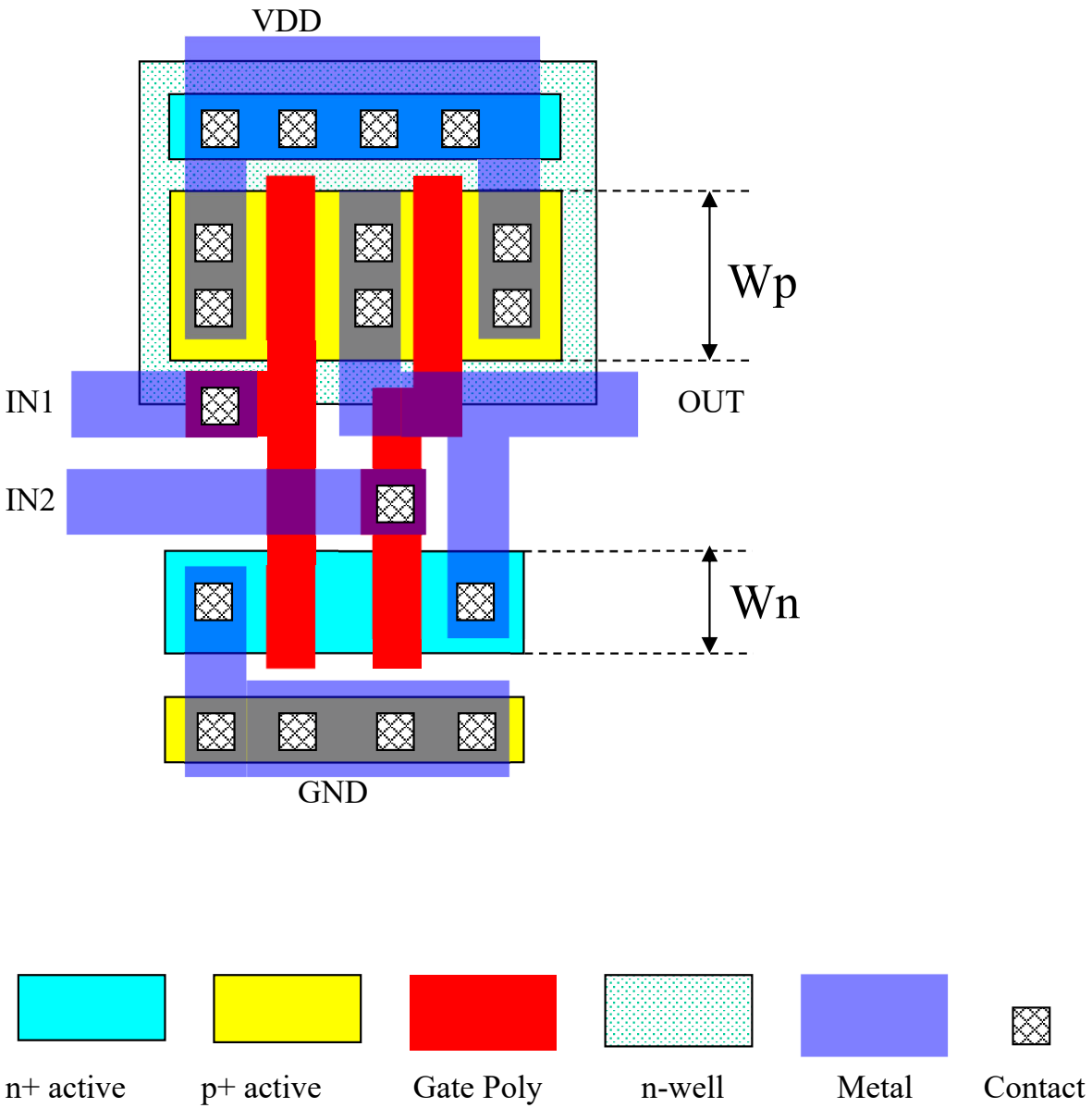
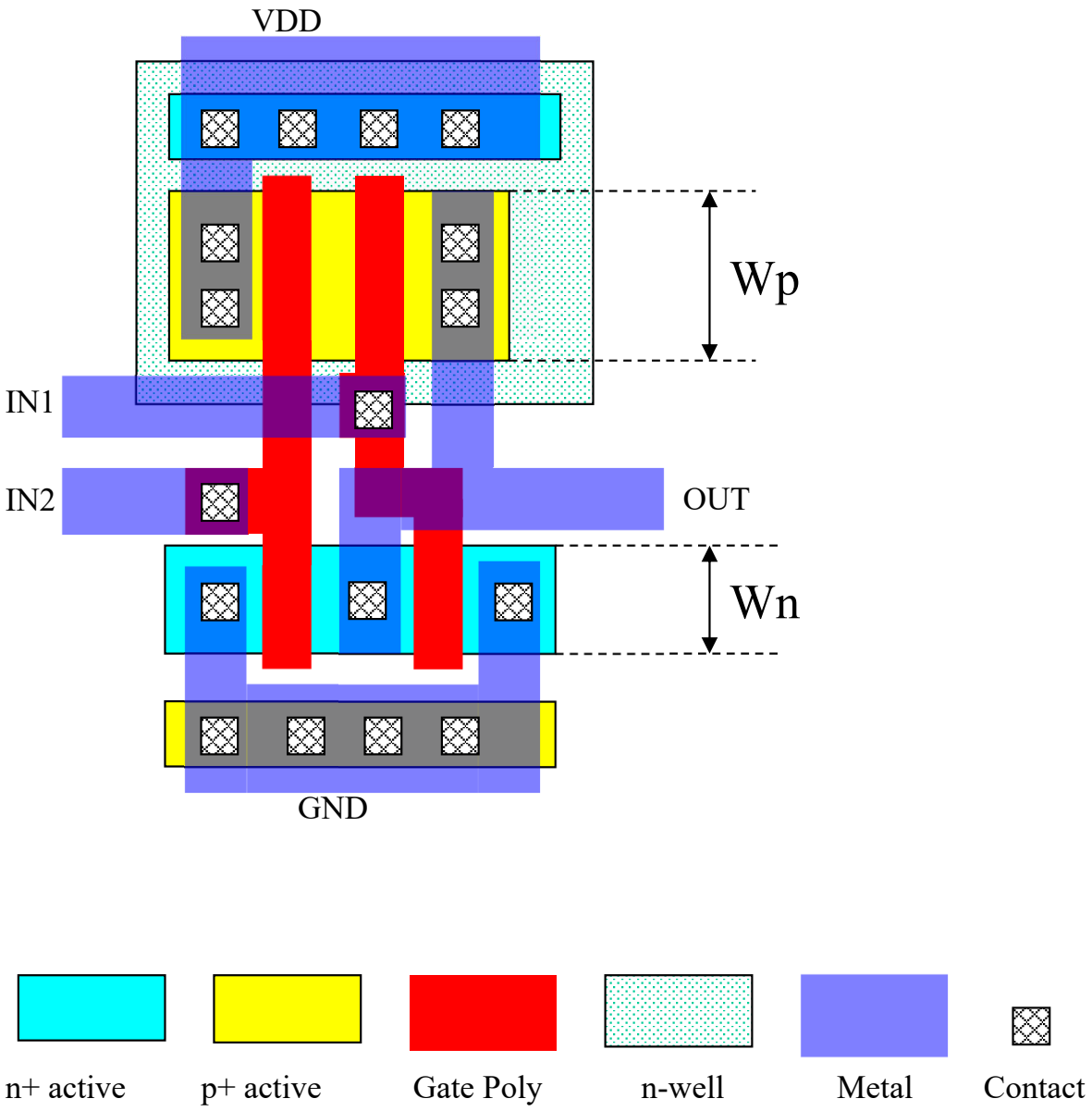


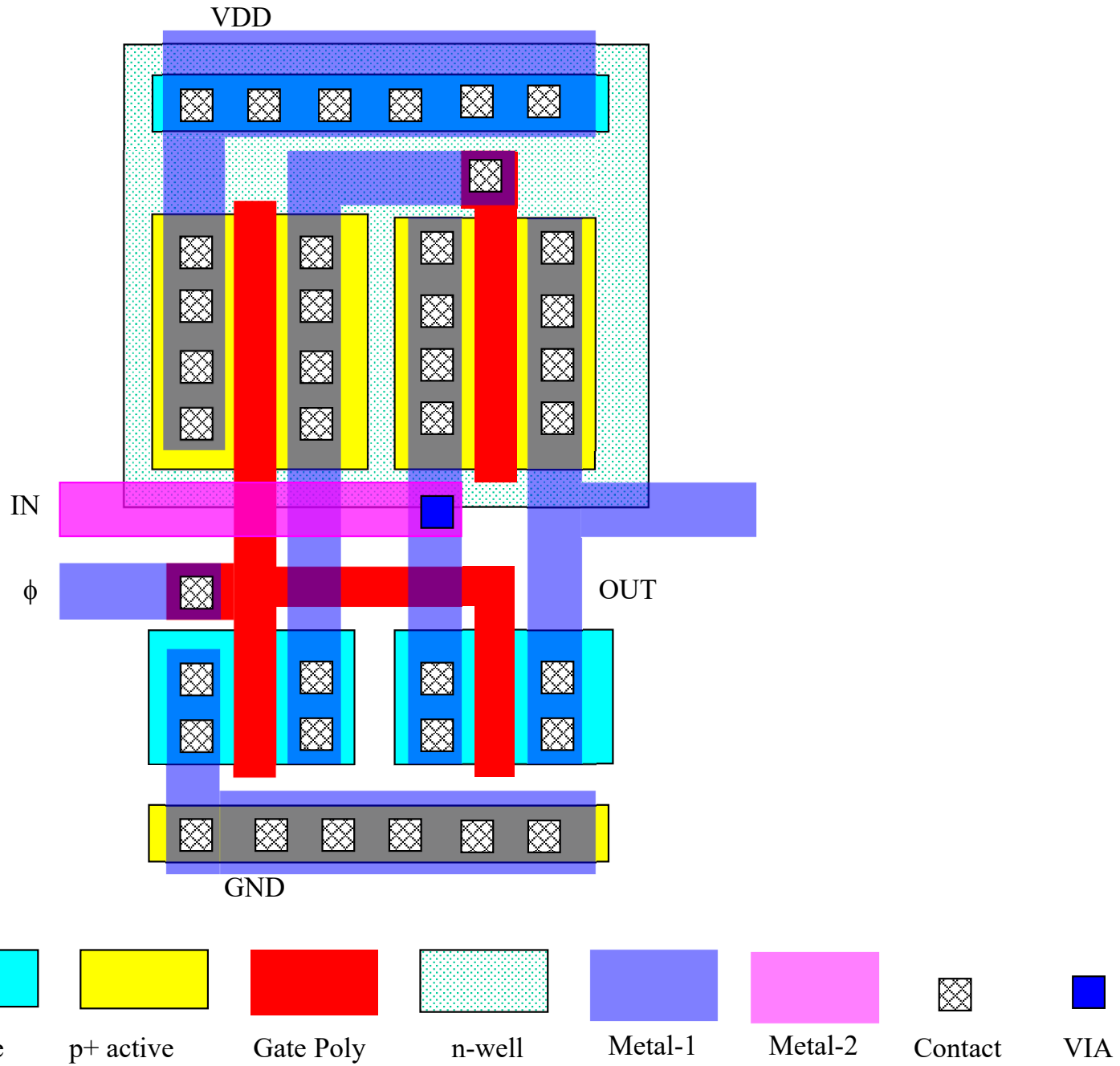
Layout example of NAND gate



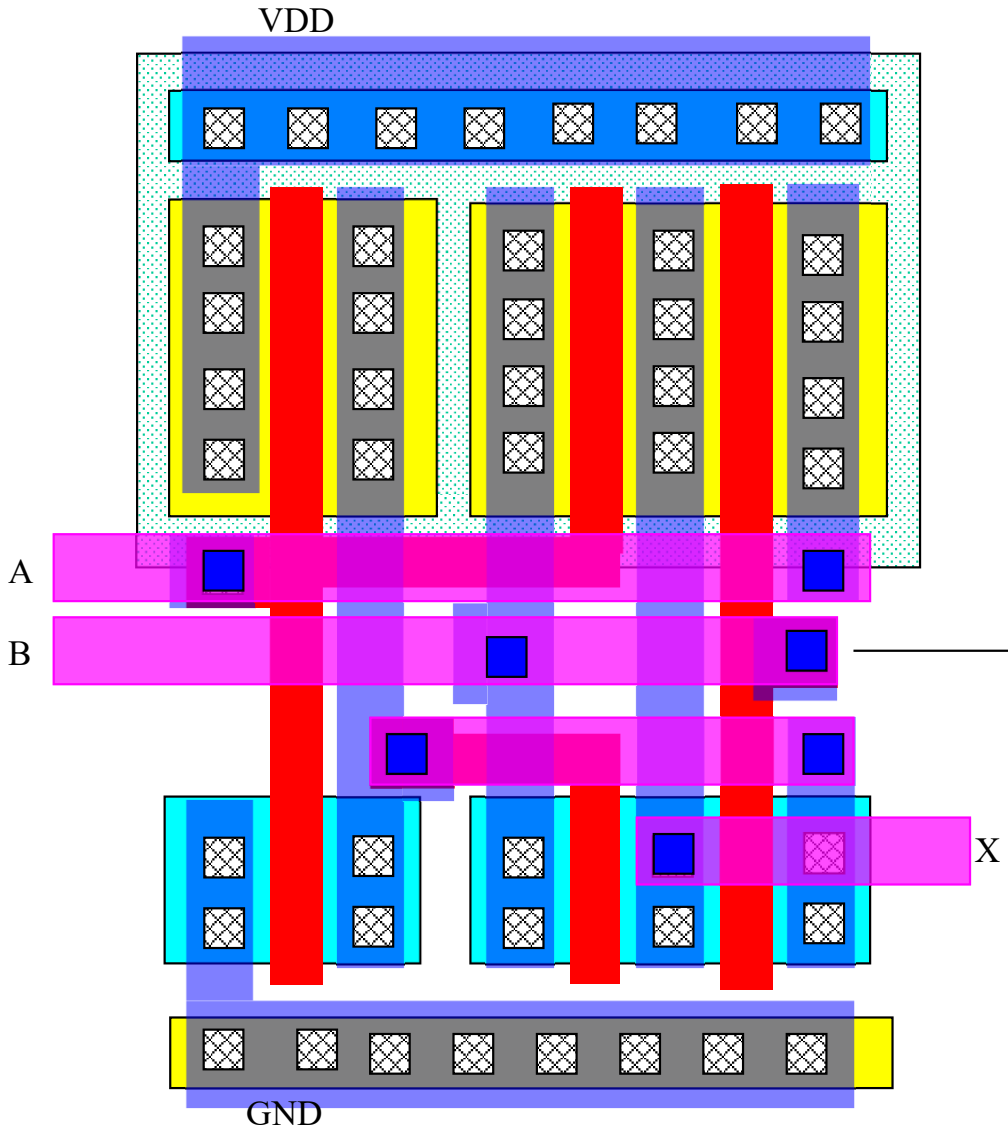
Layout example of NOR gate



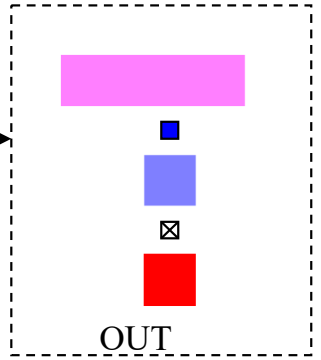
Layout example of TG



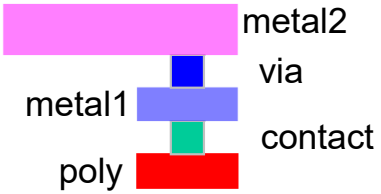
Layout example of EXOR gate



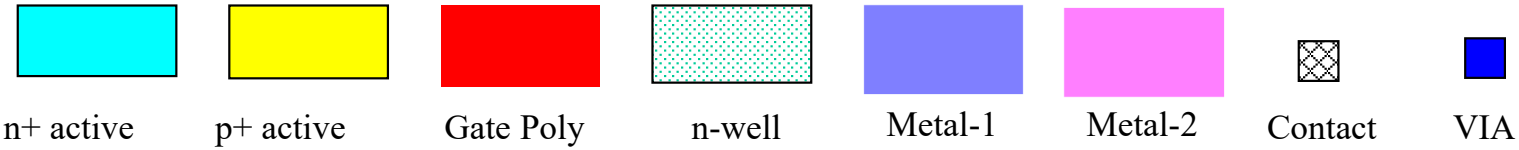
Stack VIA structure



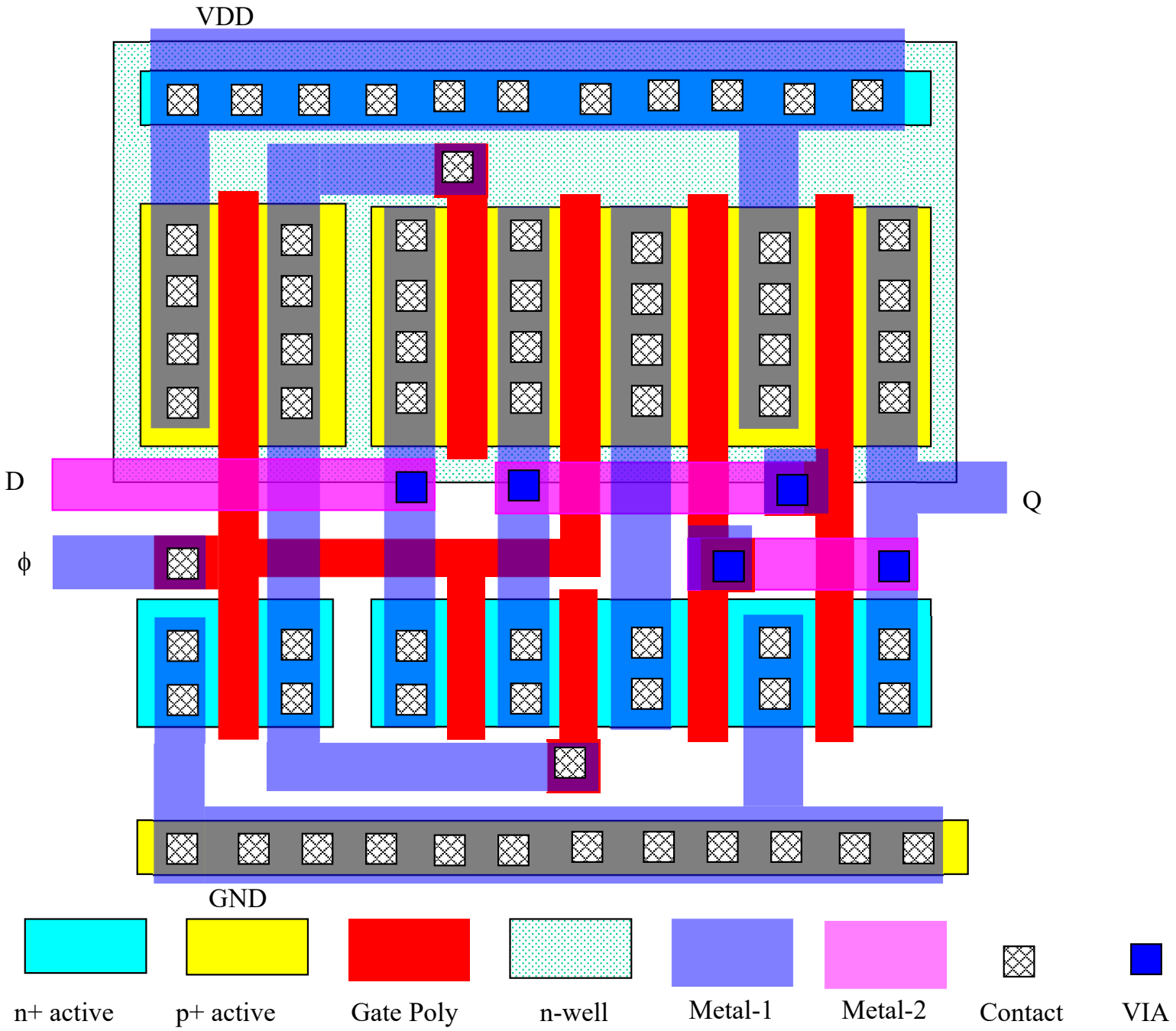
Parts of VIA structure



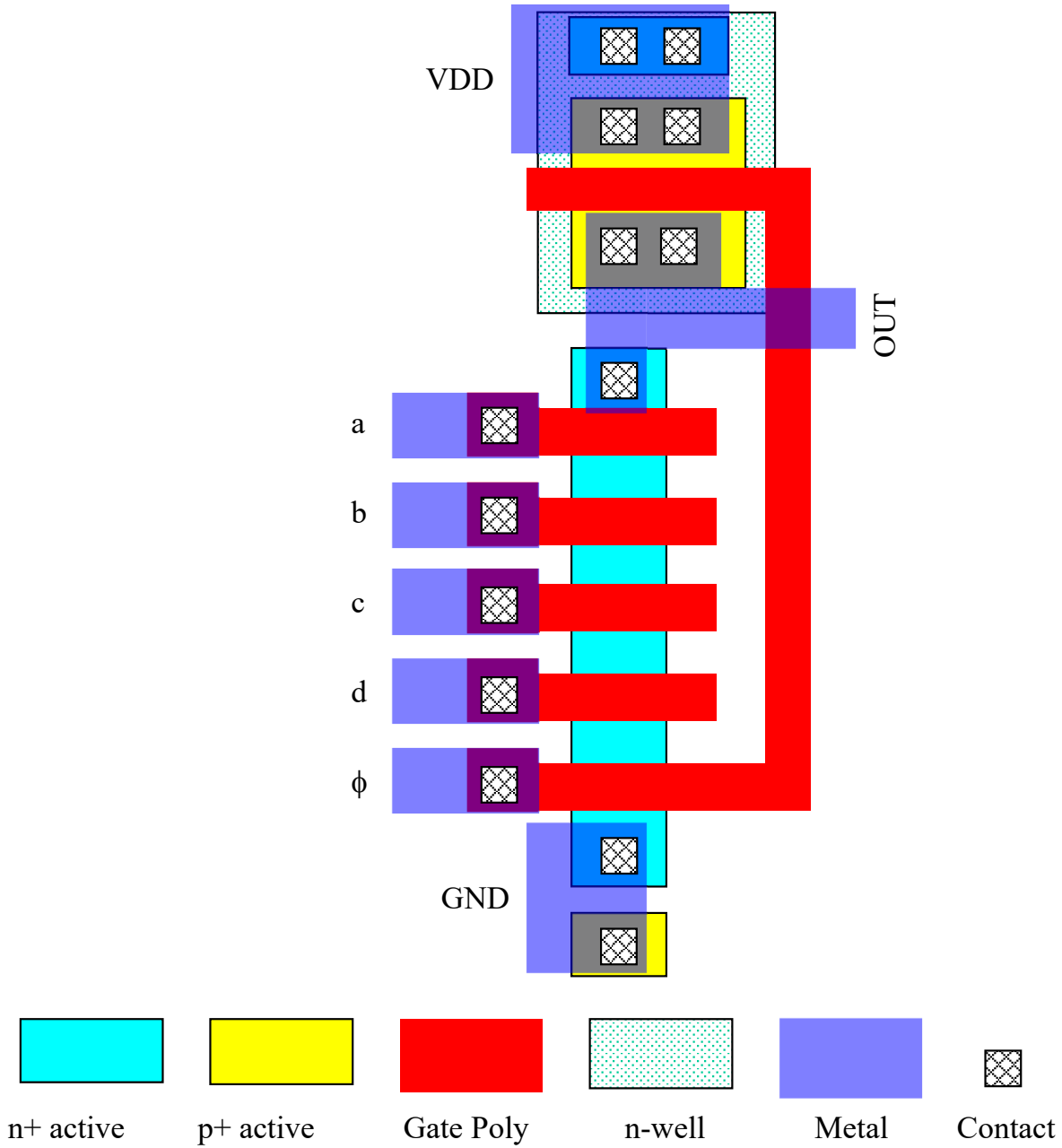
Cross section



Layout example of D-latch



Layout example of NAND designed for dynamic CMOS logic



Layout example of D-FF designed for dynamic CMOS logic