Mixed Signal LSI

Practical design method of CMOS mixed signal circuits

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Microelectronics Research Lab.
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0.1 Introduction

Books of reference

- For students who wants to learn the practical CMOS analog circuit design (*)
  - R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 4th Edition, ISBN 978-1119481515, Wiley-IEEE Press (2019)
  - R. Jacob Baker, CMOS: Mixed-Signal Circuit Design, 2nd Edition, ISBN 978-0470290262, Wiley-IEEE Press (2008)
  - 松澤昭, はじめてのアナログ電子回路実用回路編, ISBN 978-4-06-156545-6, 講談社 (2016)
- Course wares
  - http://cmosedu.com/

* These books does not cover the RF (Radio-frequency) circuits.
I recommend the following book for RF circuit design：
\- RF Microelectronics, B. Razavi, ISBN 0-13-887571-5, Prentice Hall (1998)

Course policy

1. Download the lecture slide of the on the web site.
   http://jaco.ec.t.kanazawa-u.ac.jp/edu/
2. The course is provided by face-to-face classes.
3. If you have a question in the preparation and the review, post the question on the timeline of LMS. (Click the icon of a pen.)
4. Submit the assignment by the deadline.
   – Academic misconduct and scholastic dishonesty such as a plagiarizing or cheating on examinations can be assigned a penalty based on the University code.

Grading

- Grading policies
  - Regular assignments (100%)
  - The scores of your report taken will become invalidated, if you are late to submit the report. Don’t miss the deadline of the submission.
    - However, even if the submission is delayed, it will be treated as a legitimate submission, when you can prove that you are not responsible. For example, an illness, an official event.

Q & A

- During class
  - Feel free anytime in the class.
- Office hours
  - 5th period on Friday
  - Request for an appointment.
- Timeline on WebClass
  - For questions about the lecture.
- Email
  - For questions about your grading, attendance.
  - kitagawa@merl.jp

Growing information technology toward a real world and an daily life

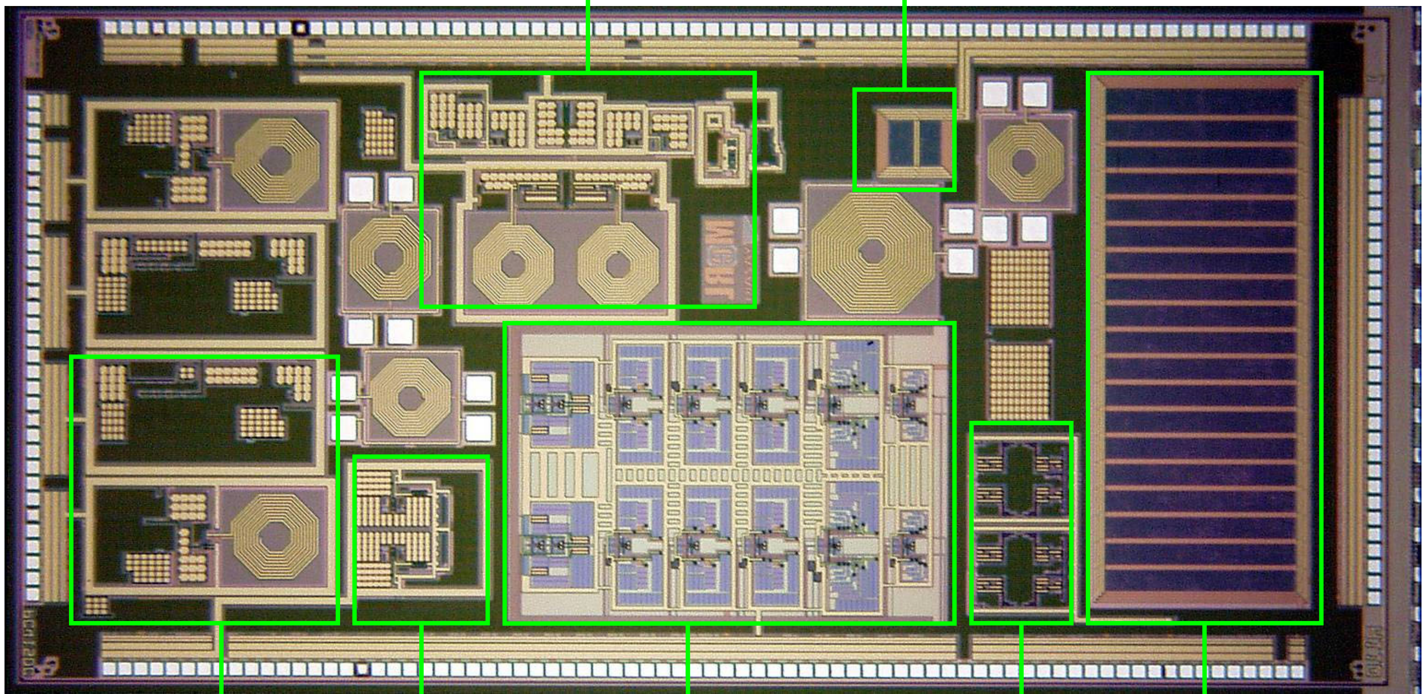
Keywords: Wireless communication, Energy Harvesting, Sensor integration

An analog mixed signal (AMS) LSI is fundamental to advanced cyber-physial systems.

Analog-mixed signal circuits in an IoT Era

- A main part of a digital system consists of digital circuits, however, the information in CPS is represented by an analog signal. For example, electromagnetic wave form in digital communication, light rays or radioactive rays in digital imaging, and chemical substances in medical and pharmaceutical applications.
- An analog-to-digital interface is required for all CPSs, because the analog circuits including the communication systems, sensor system and power controlling systems are controlled by software.
- The high-performance analog circuitry should be packaged in the black box in the mixed-signal systems and be accessed through the software interface from cyberspace.

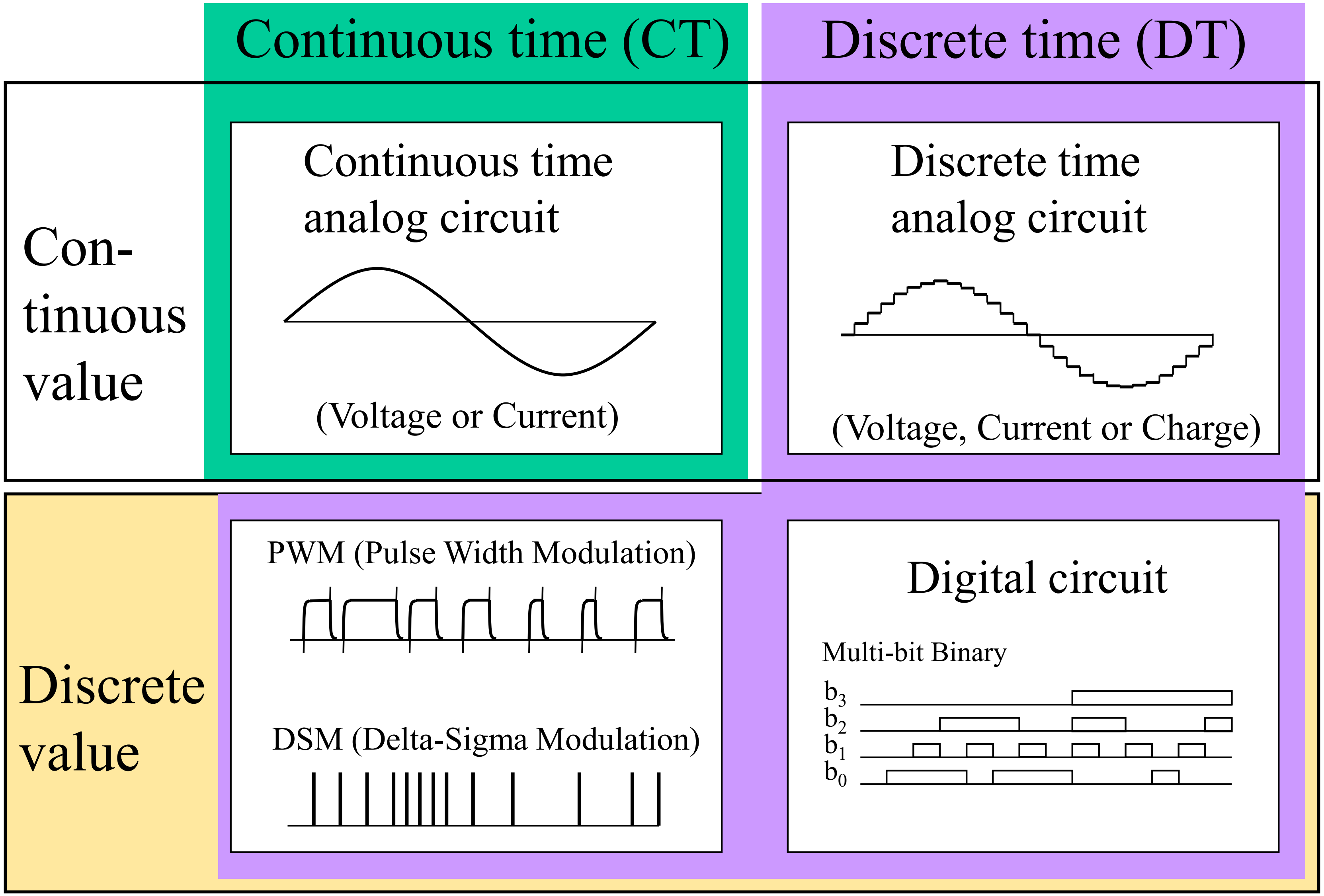
Example of Mixed-Signal LSI



A/D partition in mixed-signal LSI

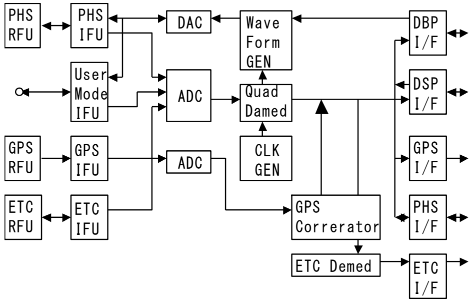
Name of circuit block	Function	Analog/Digital	Remarks
AAF (Anti-Aliasing Filter)	Band-limitation	Analog	feasible only in analog
SF (Smoothing Filter)	Transformation from discrete time to continuous time	Analog	feasible only in analog
LNA (Low Noise Amp.)	Impedance matching	Analog	feasible only in analog
Mixer	Down-conversion and Up-conversion	Analog	for RF signal
		Digital	for BB signal
Power supply circuits (e.g. Regulator, Reference Voltage, Rectifier)	Voltage regulation, DC-DC conversion, Voltage/Current reference	Analog	
ADC (Analog-to-Digital Converter)	Analog-to-Digital conversion	Analog + Digital	
DAC (Digital-to-Analog Converter)	Digital-to-Analog conversion	Analog + Digital	
PLL (Phase Locked Loop)	RF frequency synthesis	Analog or Digital	
DSM (Delta-Sigma Modulator)	Digital frequency control of PLL	Digital	
Memory（Sens-Amplifier, Memory Cell, DLL）	Memory of digital data	Analog + Digital	
Processor (DSP, MCU)	Signal processing, system control	Digital	
Filter	Hardware signal processing	Analog	for RF signal
		Digital	for baseband

Wave forms in mixed signal circuits



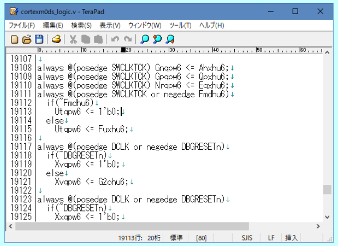
Digital design flow

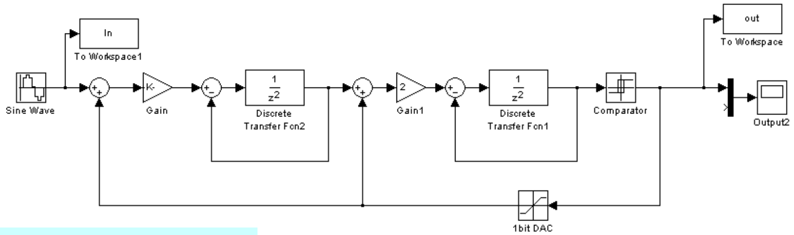
Block diagram of system architecture → Specification sheet for digital block



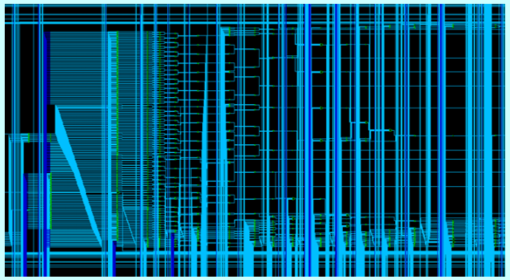
項目	条件	規格値			設計値			単位
		Min.	Typ.	Max.	Min.	Typ.	Max.	
電源電圧		1.8	3.3	3.5	1.8	2.1	3.3	V
消費電流		—	—	2.2				mA
利得		—	15	—				dB
周波数		300	426	475				
雑音指数（NF）		—	2	—				dB
1dBｺﾝﾌﾟﾚｯｼｮﾝﾚﾍﾞﾙ		—	0	—				dBm
ｲﾝﾀｾﾌﾟﾄﾎﾟｲﾝﾄ（IIP3）		—	9.6	—				dB
入力ｲﾝﾋﾟｰﾀﾞﾝｽ		—	50	—				Ω
出力ｲﾝﾋﾟｰﾀﾞﾝｽ		—	500	—				Ω
端子間ｱｲｿﾚｰｼｮﾝ（OUT→IN）				20				dB

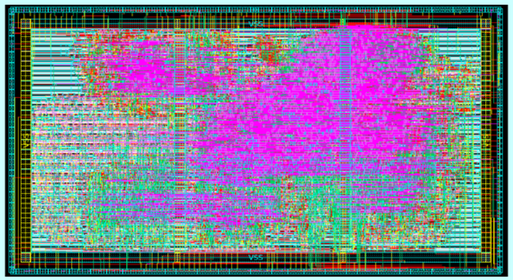
HDL (Hardware Description language) ← Signal flow and transfer function





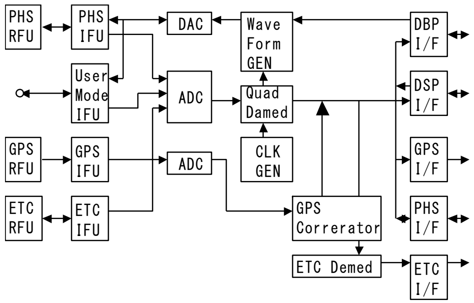
Logic Synthesis → Place and Route → Marge to analog blocks





Analog design flow

Block diagram of system architecture → Specification sheet for analog block



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入力ｲﾝﾋﾟｰﾀﾞﾝｽ		—	50	—				Ω
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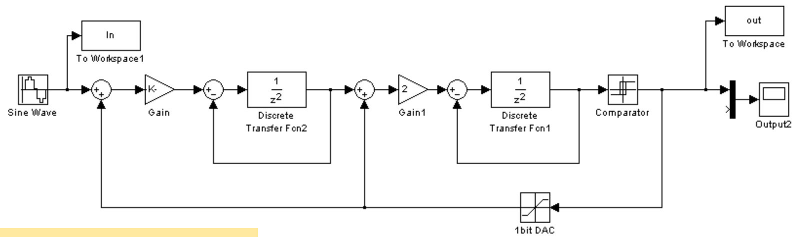
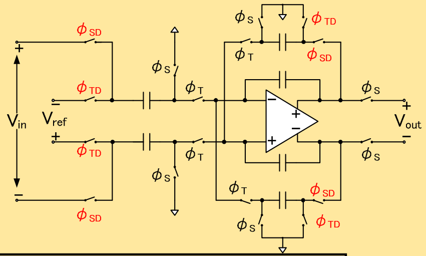
端子間ｱｲｿﾚｰｼｮﾝ (OUT→IN)				20				dB

↓

Signal flow and transfer function → Circuit schematic with behavior models



Circuit schematic with behavior models



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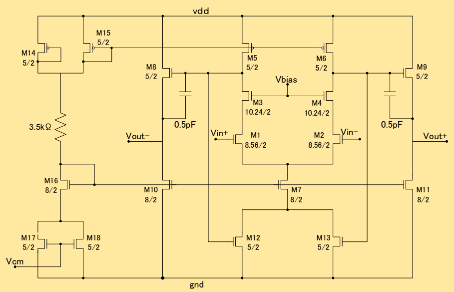
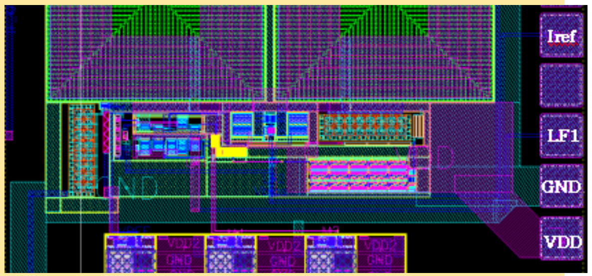
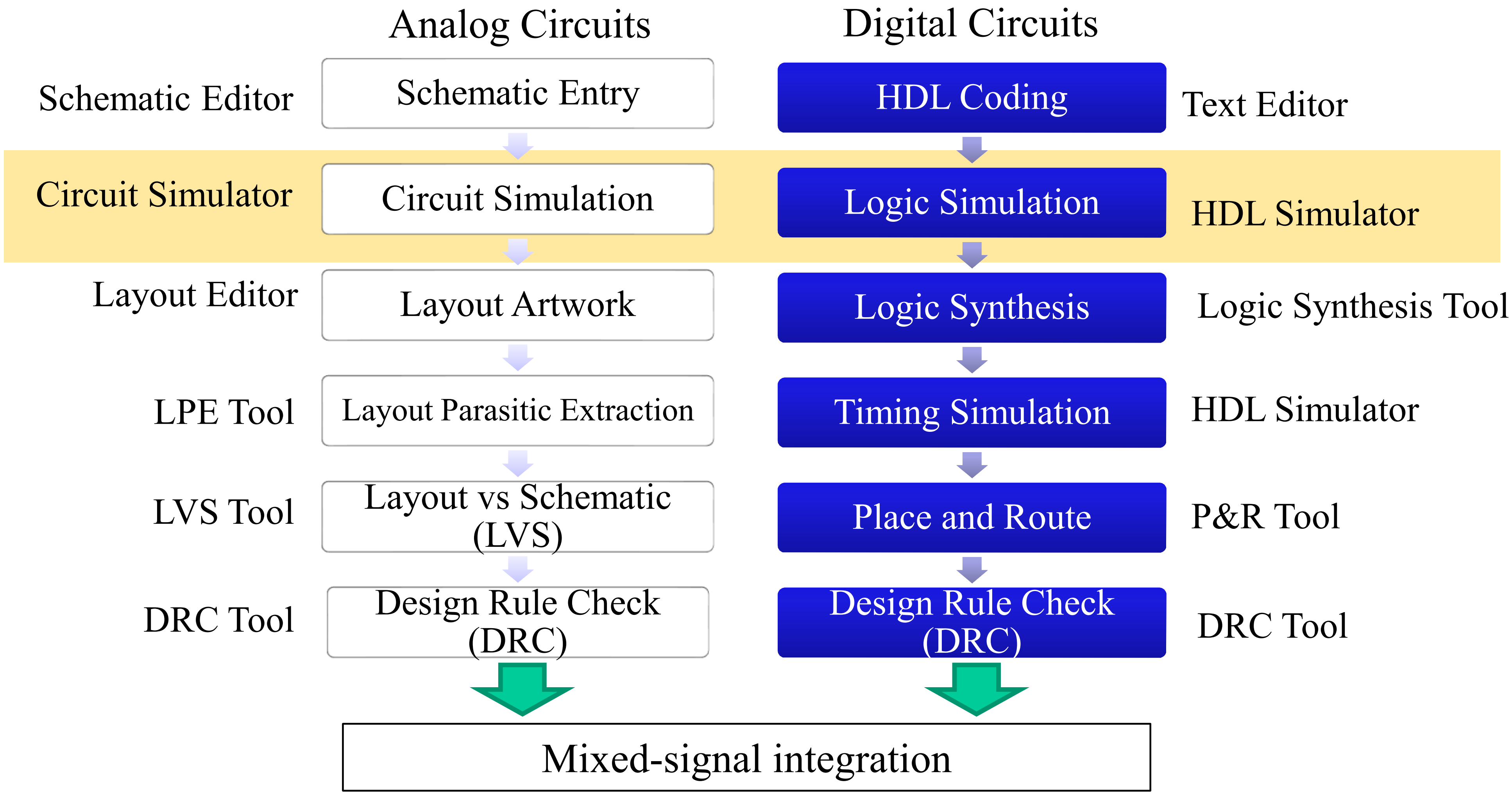
Circuit schematic with Transistors → Layout artwork → Marge to digital blocks

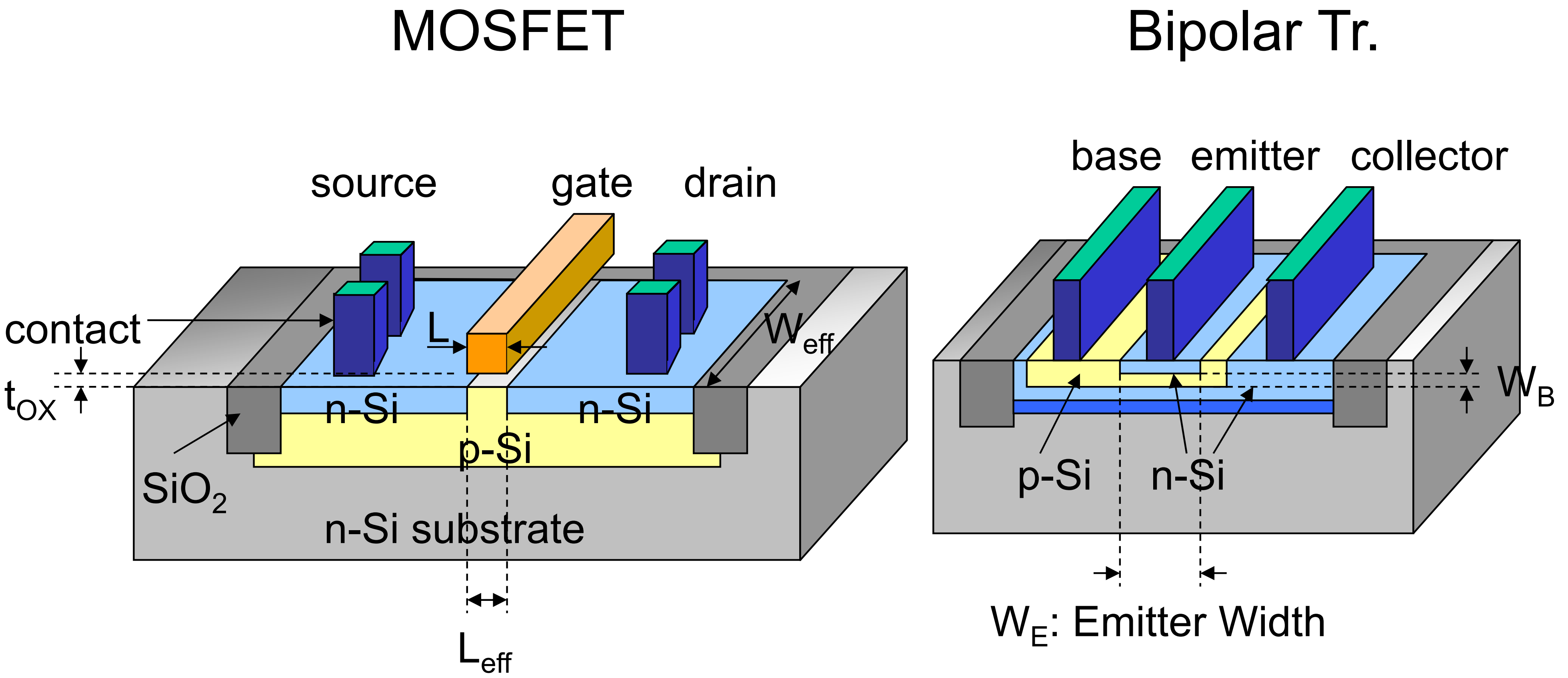




CAD software



Structure of MOSFET and Bipolar Tr.

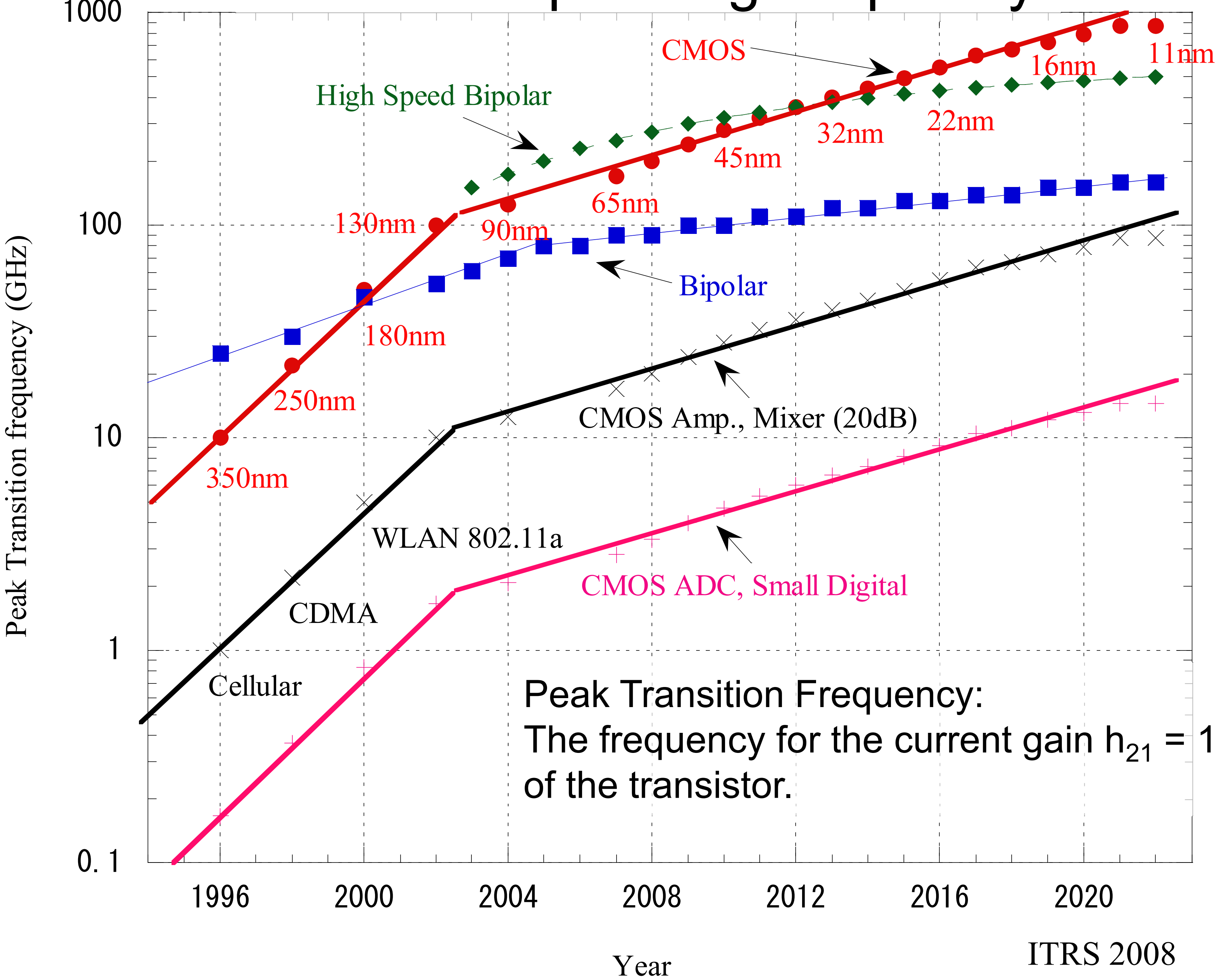


Transition frequency f_T depends on L_{eff}.

Transition frequency f_T depends on W_B.

NOTE: The peak transition frequency of bipolar transistor also depends on the base width W_B and the base resistance (small W_E is better).

Trends of operating frequency

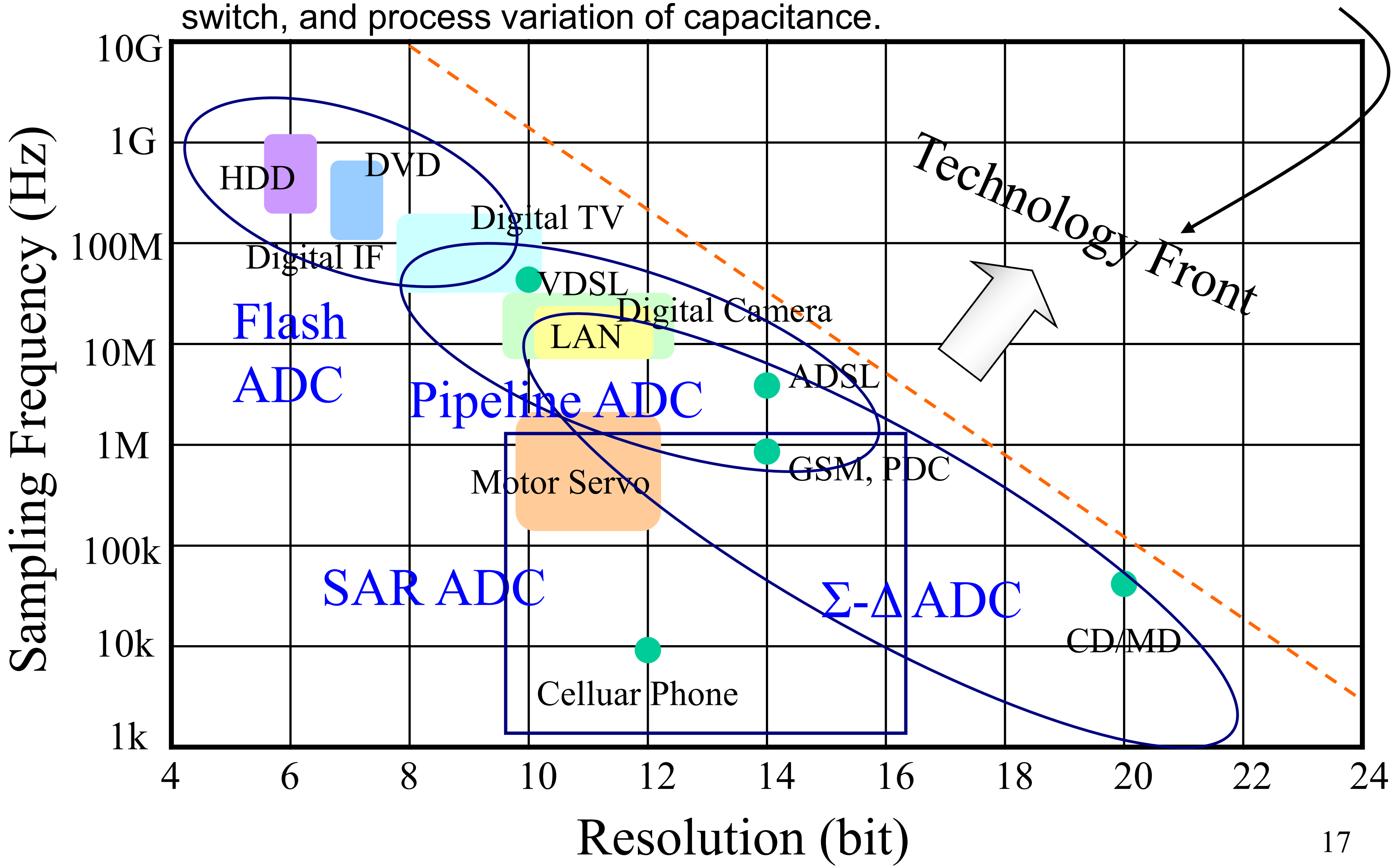


Peak Transition Frequency:
The frequency for the current gain h_{21} = 1 (0dB) of the transistor.

ITRS 2008

Performance of ADC architecture

Technology front is limited by GBP of amplifier, switching speed of CMOS-switch, and process variation of capacitance.



Advantages and disadvantages of technology scaling

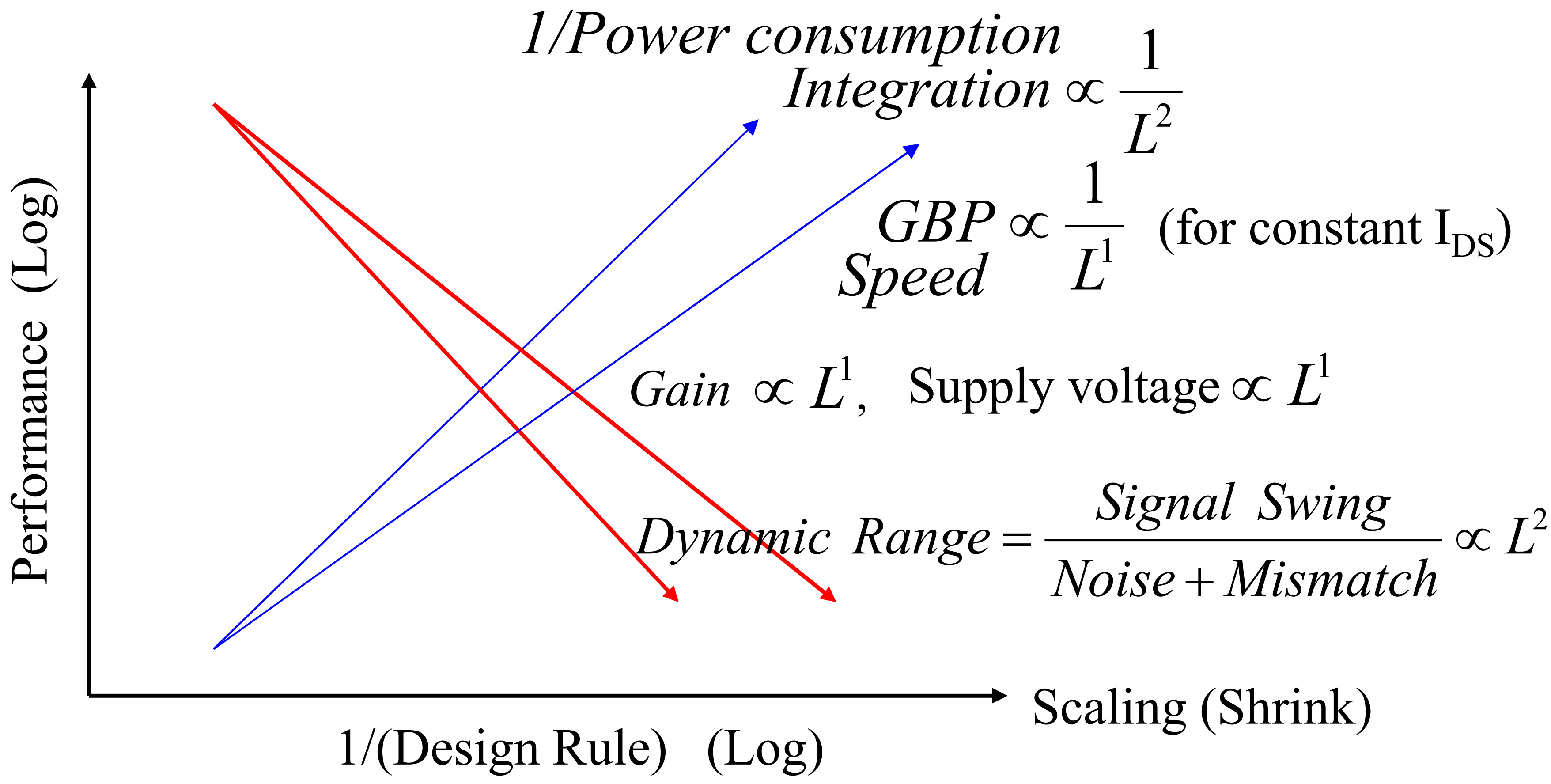


Figure of merit (FOM) of analog circuits

- Before ITRS2004 edition:

  FOM was defined for each category of circuits.
  - LNA: Low noise amplifier
  - VCO: Voltage controlled oscillator
  - PA: Power amplifier
  - ADC: Analog-to-Digital converter
  - SerDes(SERializer/DESerializer)

$$FOM_{LNA} = \frac{G \cdot IIP3 \cdot f}{(NF - 1) \cdot P}$$

$$FOM_{VCO} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\} \cdot P}$$

$$FOM_{PA} = P_{out} \cdot G_p \cdot PAE \cdot f^2$$

$$FOM_{ADC} = \frac{(2^{ENOB_0}) \cdot f_S}{P}$$

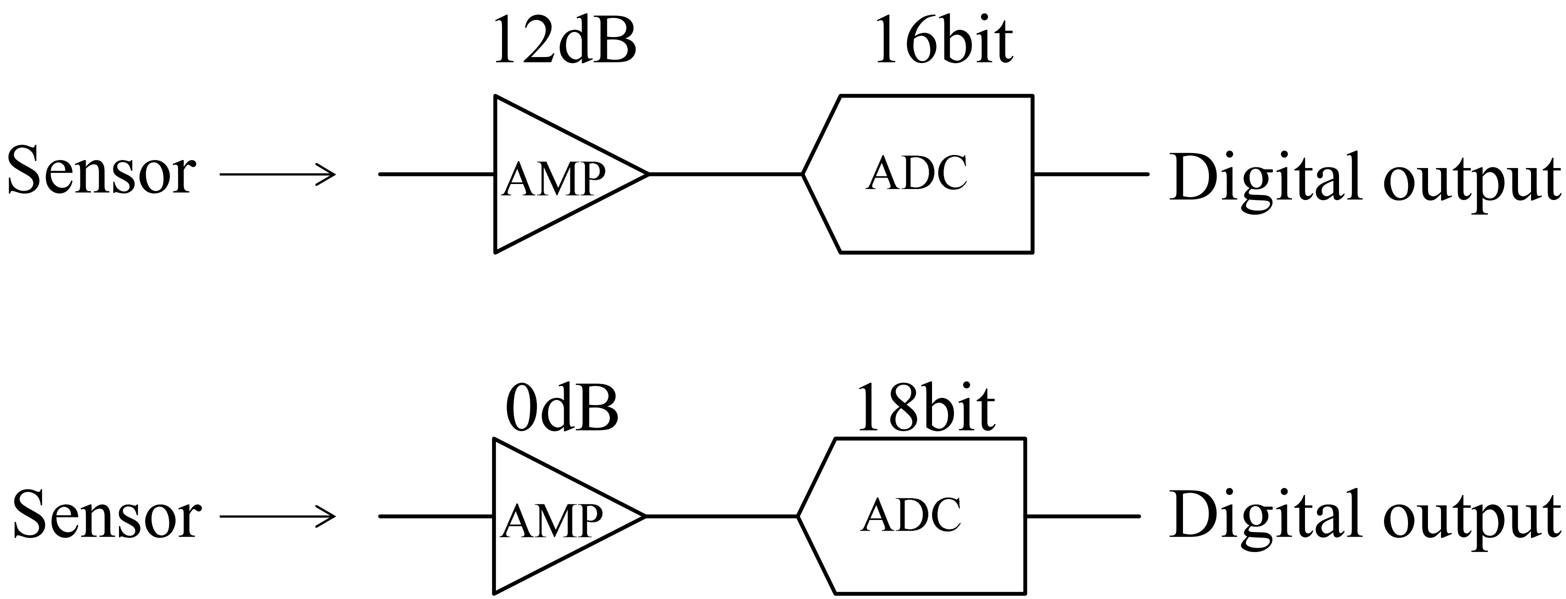
$$FOM_{SerDes} = \frac{R_B \cdot R_{MuxDeMux}}{P}$$

P : Power consumption
IIP3: Third Order Input Intercept Point
NF : Noise figure
L: Spurious power
PAE: Power efficiency

$ENOB_0$: Effective number of bits
f_S : Sampling frequency
R_B: Data Rate
$R_{MuxDeMux}$: Bit count of parallel data

Quiz

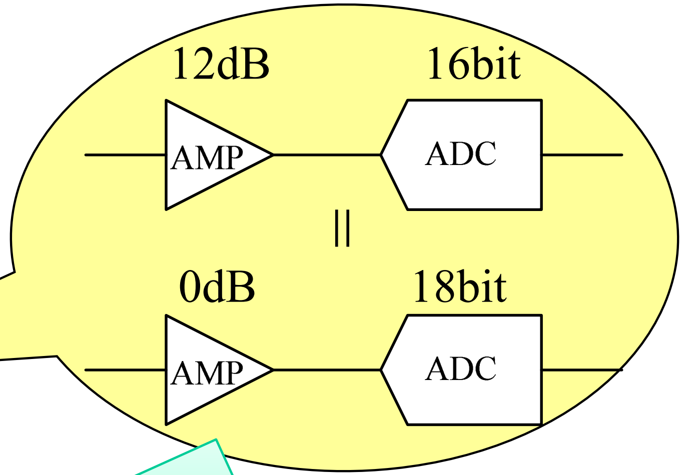
Which circuit is better for a sensitivity?



Suggested answer

Equivalent gain for LSB

$$1\text{bit} \cong 6.02\text{dB}$$



0dB amplifier = No amplifier (no noise)

Why is the increment of 1bit equivalent with the amplification of 6dB (2 times)?

Suggested answer

Maximum number of N-bit binary code = 2^N -1
Dynamic range of N-bit binary code system
= Maximum signal/Minimum signal = (2^N -1)/1
Maximum number of (N+1)-bit binary code = 2^{N+1} -1
Dynamic range of (N+1)-bit binary code system = (2^{N+1} -1)/1

The amplitude of signal that is equivalent for the differential dynamic range between (N+1)-bit and N bit system is corresponding to (2^{N+1} -1)/ (2^N -1) ≒ 2 ≒ 6.02dB

Note that this calculation is made under the condition that no oversampling. More precise analysis is shown in next slide.

Speed - Accuracy - Gain

SNR for quantization noise and ENOB(Effective number of bits) in oversampling condition

$$SNR_{\max}[dB] = 6.02 \cdot N + 1.76 - 20 \cdot \log[\frac{\pi^M}{\sqrt{2 \cdot M + 1}}] + (20 \cdot M + 10) \log OSR$$

$$ENOB[bit] = 1 + \frac{1}{6.02}[(20 \cdot M + 10) \log OSR - 20 \log(\frac{\pi^M}{\sqrt{2 \cdot M + 1}})]$$

M : Order of noise-shaping transfer function

OSR: Oversampling ratio

Example

Speed → Accuracy → Gain

M = 0, OSR = 128, then ENOB = 4.5[bit], ΔSNR_{max} = 27[dB]

M = 1, OSR = 128, then ENOB = 10.6[bit], ΔSNR_{max} = 64[dB]

NOTE: The theoretical base will be discussed later.