1. Tools and simulation model

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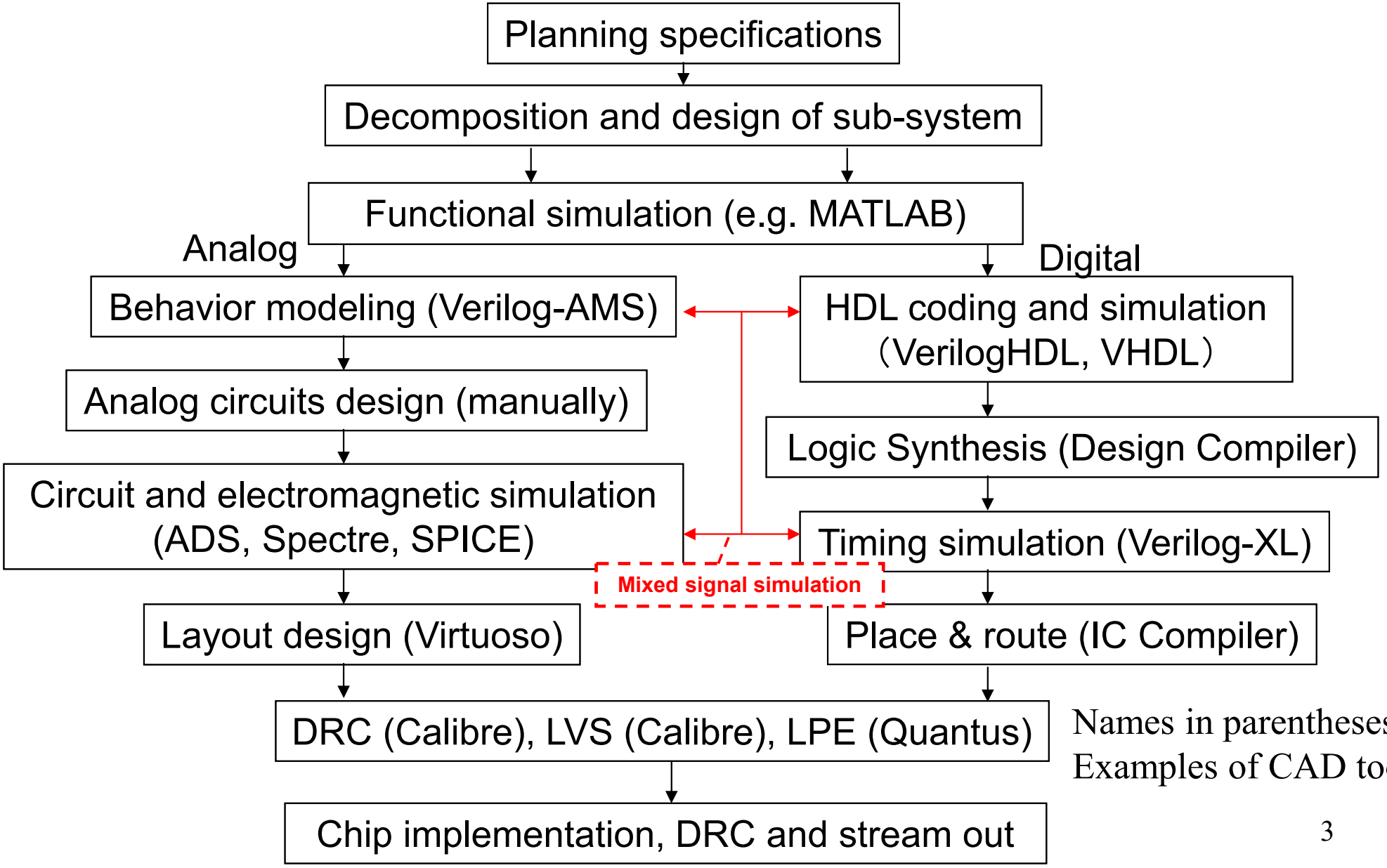
1.1 Mixed signal design flow

Design flow of mixed signal LSI



Names in parentheses:
Examples of CAD tools

Tools for mixed signal design

Signal form	Tools	Tools supported by VDEC
Digital	HDL simulator	Verilog-XL (Cadence) NC-Verilog (Cadence)
	Logic synthesizer	Design compiler (Synopsys)
	Place and Rout tool	IC Compiler (Synopsys) SOC Encounter (Cadence)
	Layout editor	Virtuoso layout suite GXL (Cadence)
Analog	Circuit simulator	Virtuoso MMSIM (Cadence) HSPICE RF (Synopsys) ADS (Keysight)
	Schematic editor	Virtuoso schematic editor XL (Cadence)
	Layout editor	Virtuoso layout suite GXL (Cadence)
	Layout verification tool	Calibre (Mentor Graphics), Quantus (Cadence)

Expressive form of circuits

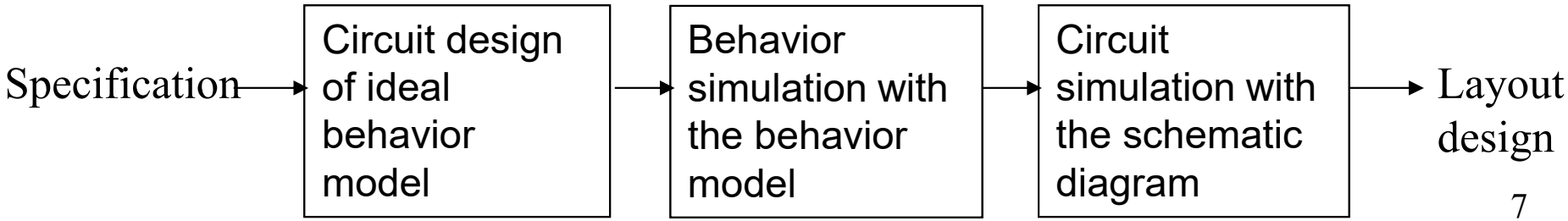
Signal form	Level of description	Standard language
Digital	Behavioral (Resister Transfer level HDL)	VerilogHDL (Verilog-D) VHDL
	Structural (Output from logic synthesizer)	VerilogHDL VHDL
	Transistor circuit (provided by a semiconductor company)	SPICE Netlist
	Physical layout	GDS-II (or stream)
Analog	Behavioral (Analog mixed signal HDL)	Verilog-A Verilog-AMS (Upper compatible to Verilog-A) VHDL-AMS
	Transistor circuit	SPICE Netlist
	Physical layout	GDS-II (or stream)

1.2 Simulation model of circuits

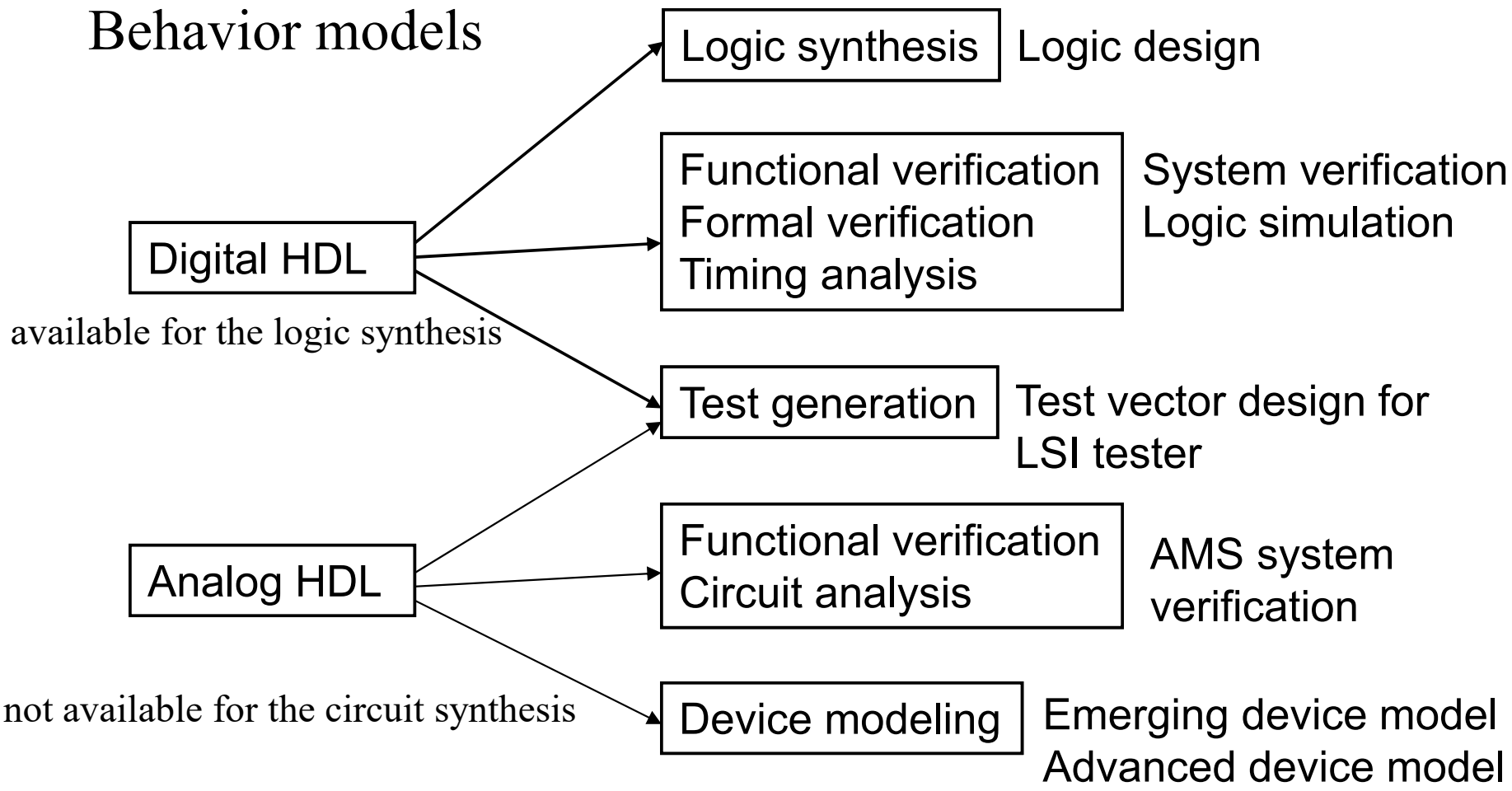
Circuit schematic vs. Behavior model

- Circuit schematic description (e.g. SPICE netlist)
  - Description using the interconnections between MOSFET and passive elements
  - High accuracy based on the physical MOSFET model
  - Taking long time for the simulation (several days ~ several week)
- Behavior description (e.g. Verilog-AMS)
  - Description using the mathematical expression of the function or electrical characteristics of the circuits
  - Expressive ability on the ideal characteristic of the circuits
  - Simulation ability on the deviation between the ideal and non-ideal characteristic
  - Taking short simulation time for the simulation (several minute ~ several hour)

Design flow of analog circuit block



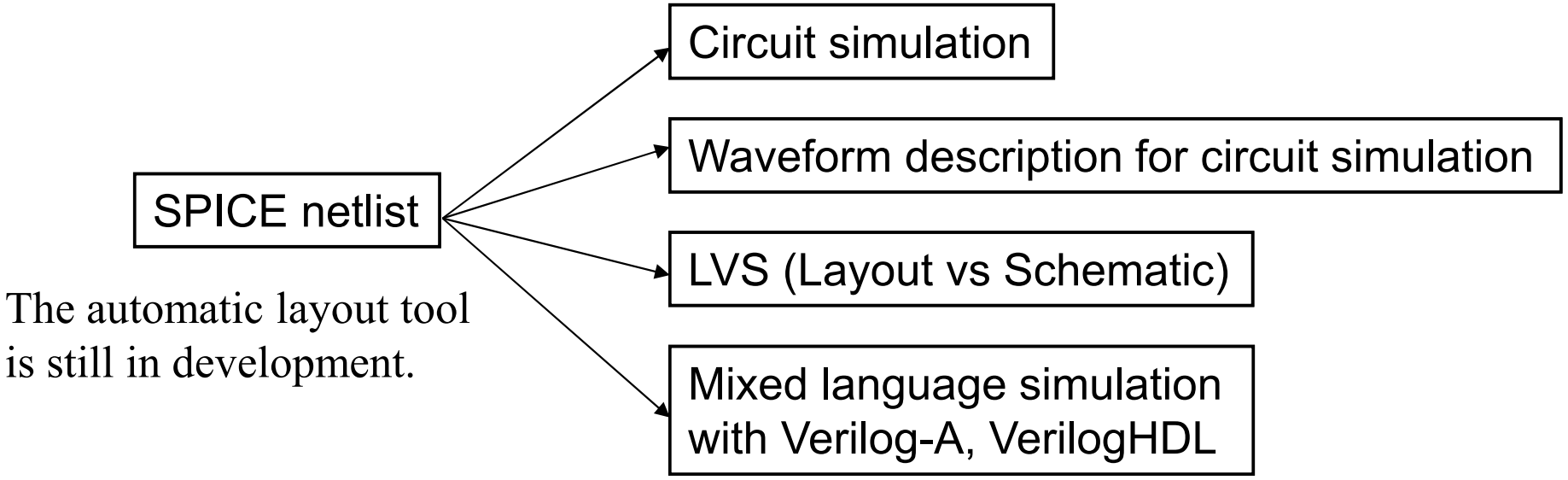
Purpose of behavior modeling



Purpose of circuit schematic

- Circuit schematic
  - SPICE Netlist (generated by the netlister from schematic diagram)
  - SPICE device model (provided by each semiconductor company)

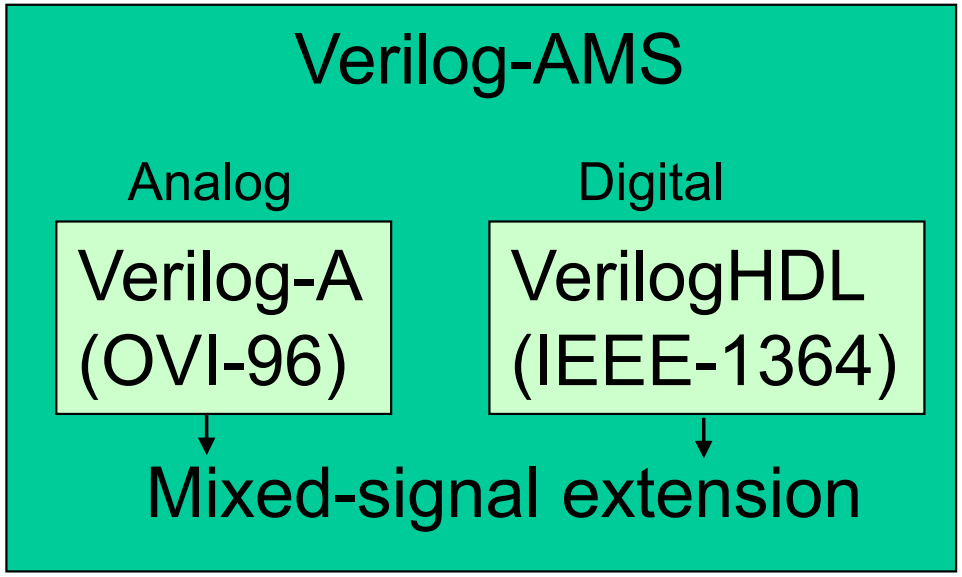
NOTE: The analog HDL can descript the circuit in the transistor level, but the simulation time is longer in compare with the circuit simulator.



Mixed signal description language

- VerilogHDL (Digital behavior description)
- Verilog-A (Analog behavior and electrical characteristic description)
- SPICE（Transistor circuit schematic description）

Mixed



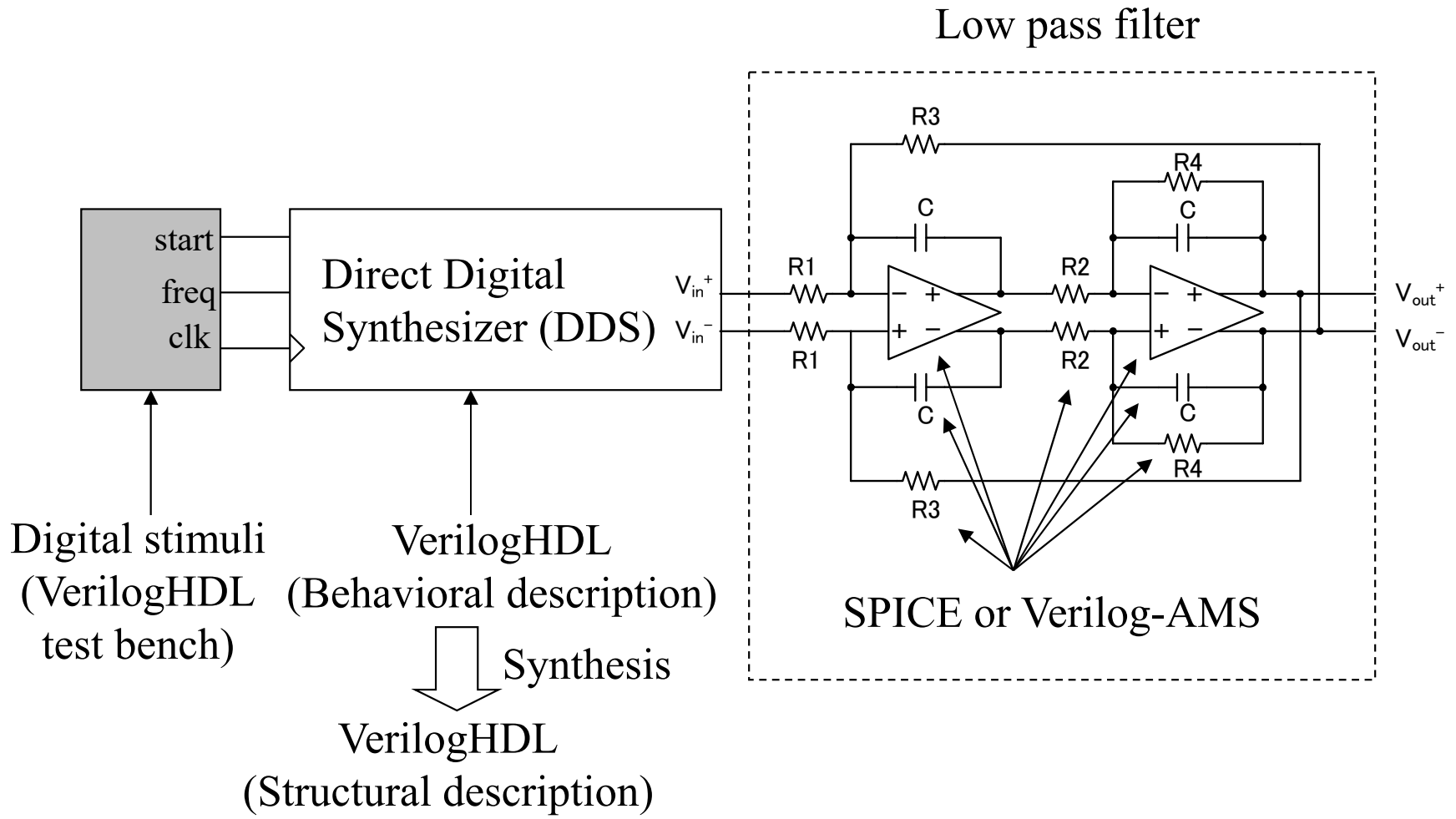
OVI: Open Verilog International

Examples of Mixed language simulators:

- Cadence: Spectre-Verilog
- Silvaco: Harmony (free for evaluation)
- Dolphin: SMASH (free for evaluation)

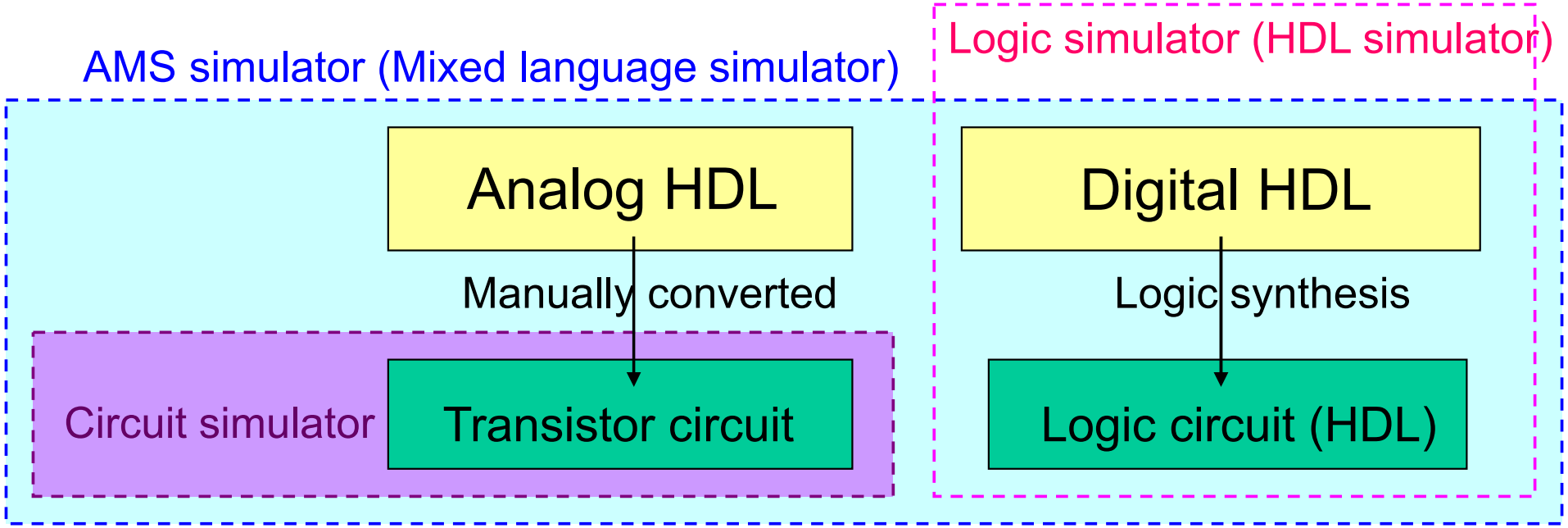
NOTE: Digital modules are should be separately described from analog modules, because the analog HDL code usually can not be recognized by a logic synthesizer.

Example of mixed language description



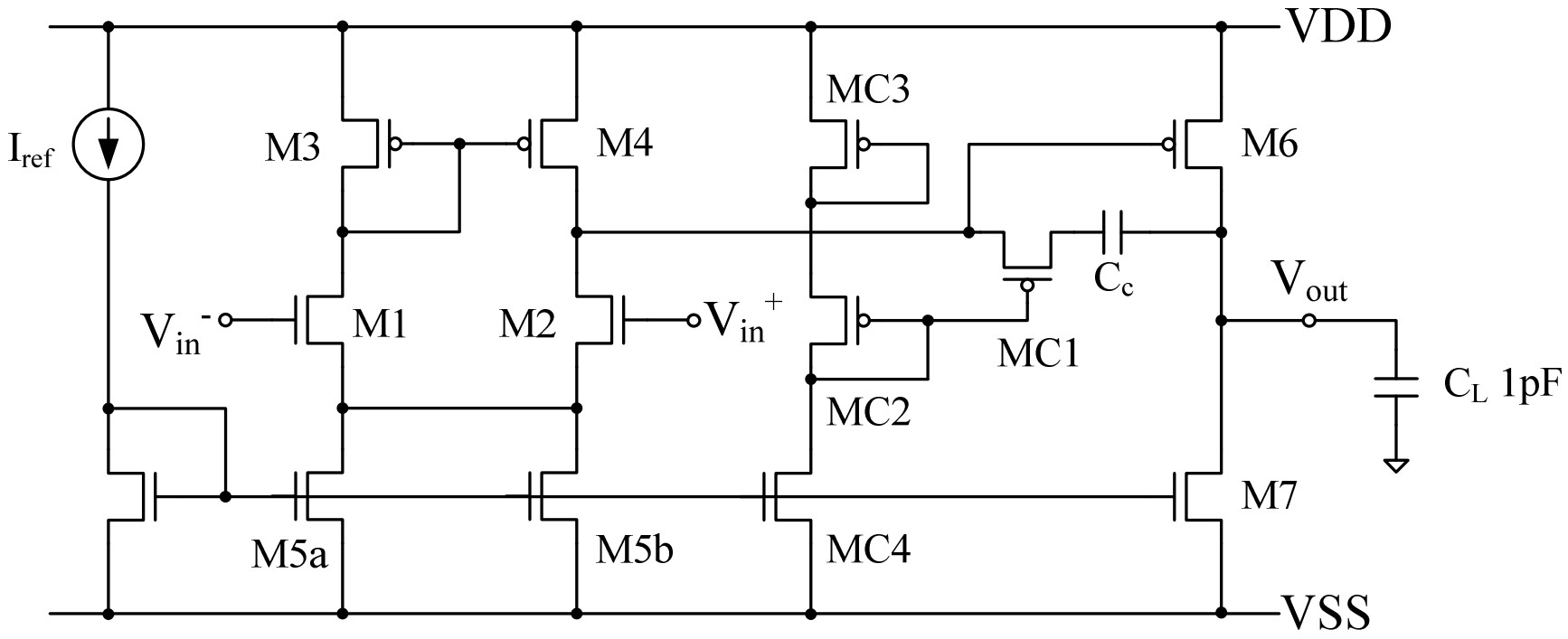
Mixed language simulation

- HDL is useful to analyze and verify the whole system or the sub-module including the analog and digital sub-system.
- If you need to analyze with the accurate simulation with the physical MOFET model, you can carry out the mixed language simulation with HDL and schematic using the mixed language simulator.



NOTE: The categorization of the circuit simulator depends on the CAD software vender.

Example of transistor circuit (Netlist)

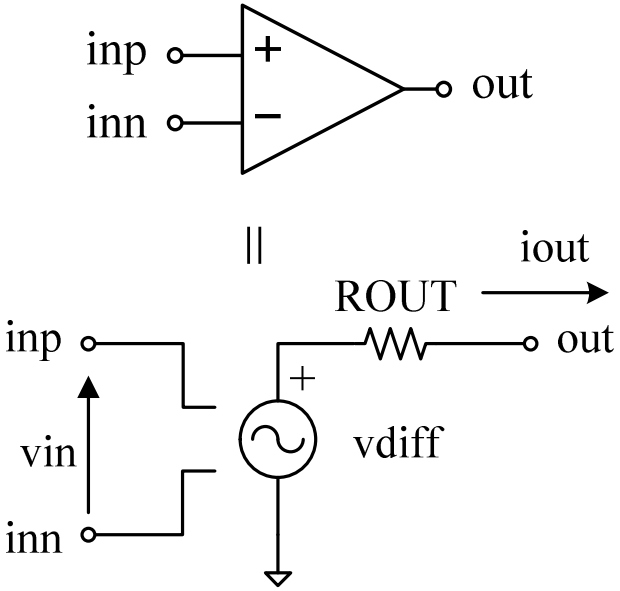



```
M1 N001 VIN-  N002 VSS N_1u l=1u w=5u ad=15p as=15p pd=11u ps=11u m=1
M2 N003 VIN+ N002 VSS N_1u l=1u w=5u ad=15p as=15p pd=11u ps=11u m=1
M3 N001 N001 VDD VDD P_1u l=1u w=15u ad=45p as=45p pd=21u ps=21u m=4
M4 N003 N001 VDD VDD P_1u l=1u w=15u ad=45p as=45p pd=21u ps=21u m=4
....
```

Transistor model name Transistor model parameters

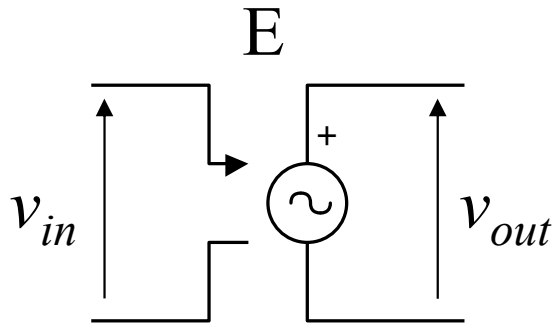
Example of Verilog-A behavior model

```
module opa_01(inp, inn, out);
   inout inp, inn, out;
   electrical inp, inn, out;
   parameter real GAIN      = 10000 from (0:inf),   // dc gain
                  ROUT      = 100 from (0:inf),     // output R
                  POLE_FREQ = 1M from (0:inf);      // pole frequency
   real vin, vdiff, vout, iout;

   analog begin
      // monitoring the nodes
      vin   = V(inp, inn);
      vout  = V(out);

      // dc gain and 1st pole
      vdiff = laplace_nd(GAIN*vin, {1},{1,1/(`M_TWO_PI*POLE_FREQ)});

      // output resistance
      iout  = (vdiff - vout)/Rout;

      // output  current
      I(out) <+ -iout;
   end
endmodule
```



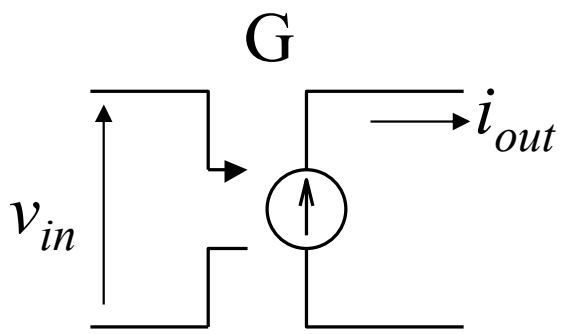
Principle of Behavioral description of amplifiers

- Function of Amplifiers described by using controlled voltage/current source
  - Voltage controlled voltage source (VCVS) (SPICE-reserved char: E)
  - Voltage controlled current source (VCCS) (SPICE-reserved char: G)
  - Current controlled voltage source (VCVS) (SPICE-reserved char: F)
  - Current controlled current source (VCCS) (SPICE-reserved char: H)



Voltage gain = v_{out}/v_{in}

Voltage Amplifier

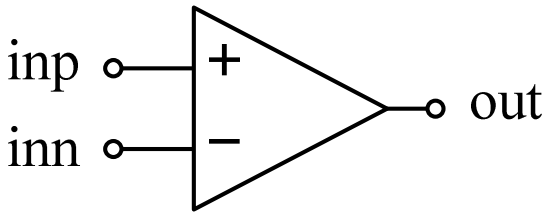


Trans-conductance= i_{out}/v_{in}

Transconductance Amplifier

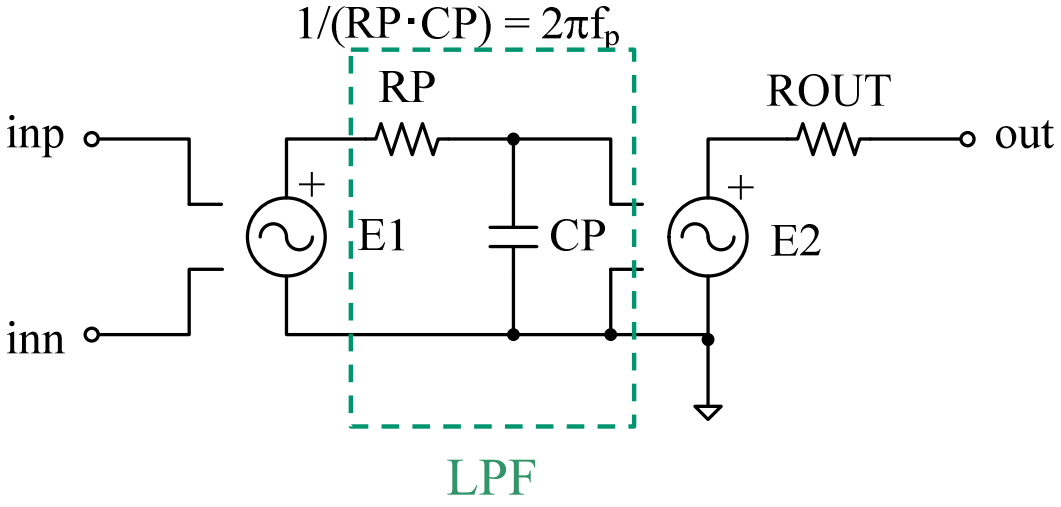
Example of SPICE behavior model

The frequency response of OPA is simulated with RC LPF.



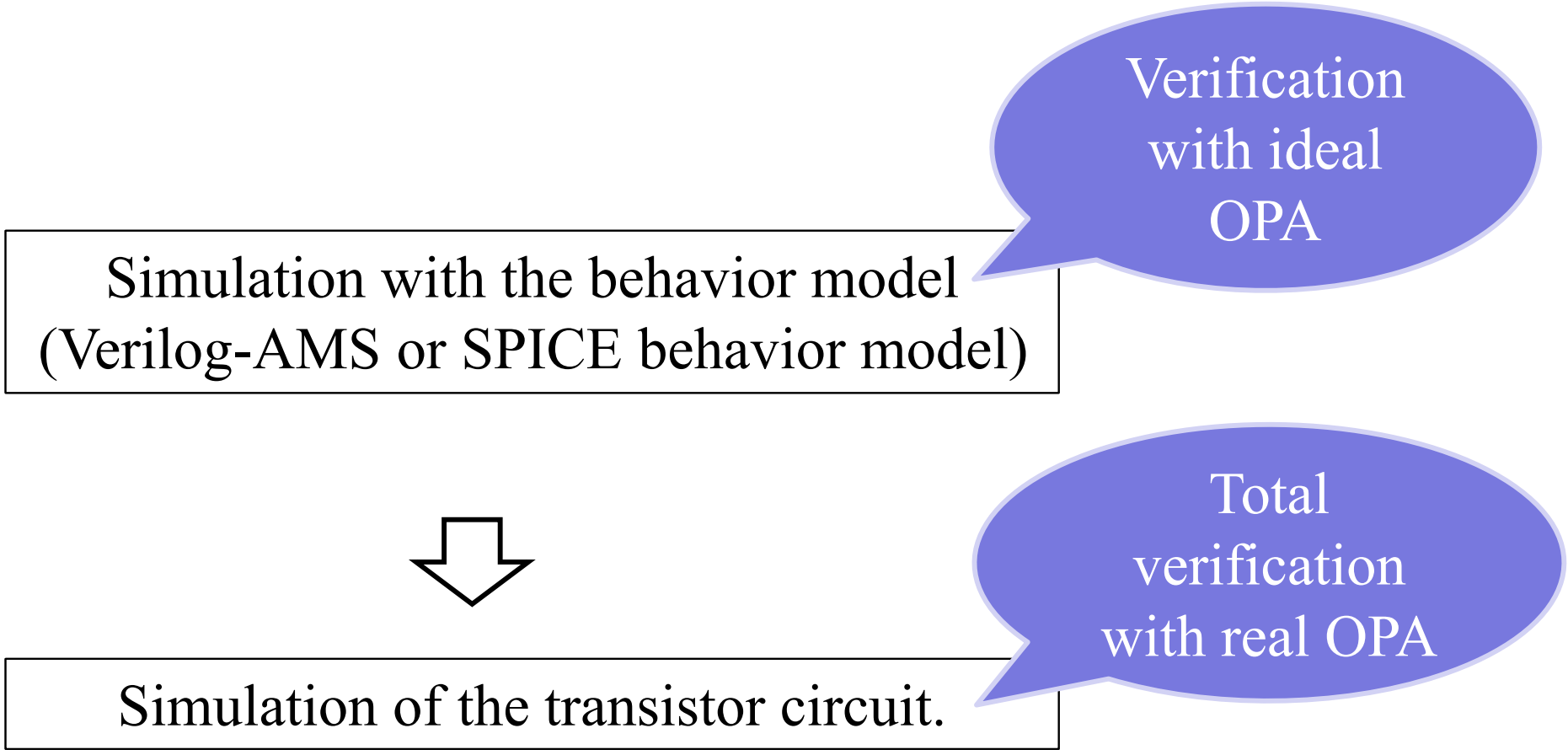
||

```
.SUBCKT opa_02 inp inn out
E1     1   0   inp   inn   10000
RC     1   2   318
CP     2   0   1n
E2     3   0   2   0   1
ROUT   3   out   100
.ENDS opa_02
```



Note: A behavior model should not include a transistor model.

2-step verification of analog circuits



NOTE: Verilog-AMS is an extended language including Verilog-A and Verilog-D.