15. Discrete time analog circuits

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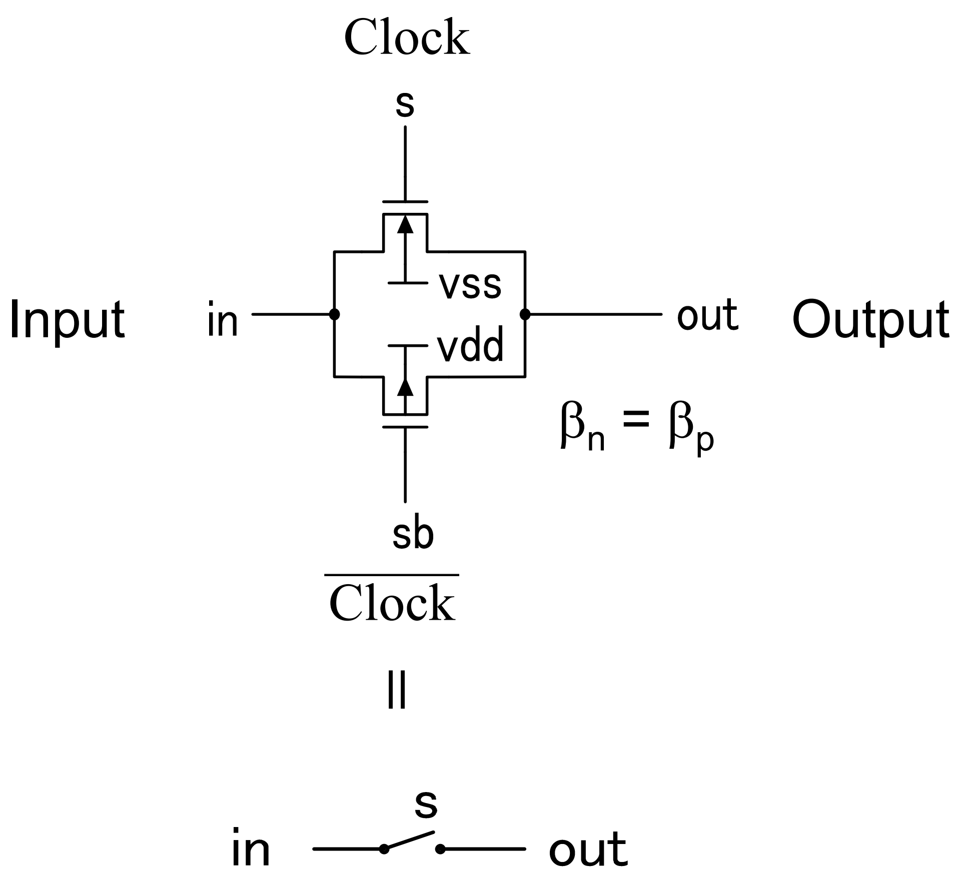
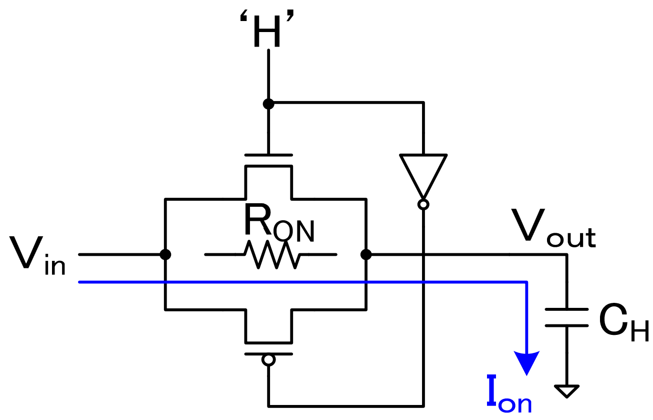
15.1 Analog switch

Analog switch (CMOS transmission gate)





$$\text{Time Constant} = R_{ON} \cdot C_H = \frac{C_H}{g_{dsn} + g_{dsp}}$$

g_{dsn}, g_{dsp}: Channel conductance of n-ch MOSFET and p-ch MOSFET

Conductance of analog switch

There is a minimum conductance at the middle of VDD and VSS.

n-ch MOSFET

$$\begin{cases} V_{in} - V_{out} = 0 \quad \text{(Linear region)} \\ V_{gsn} = VDD - V_{in} \\ V_{gsp} = VSS - V_{in} \end{cases}$$

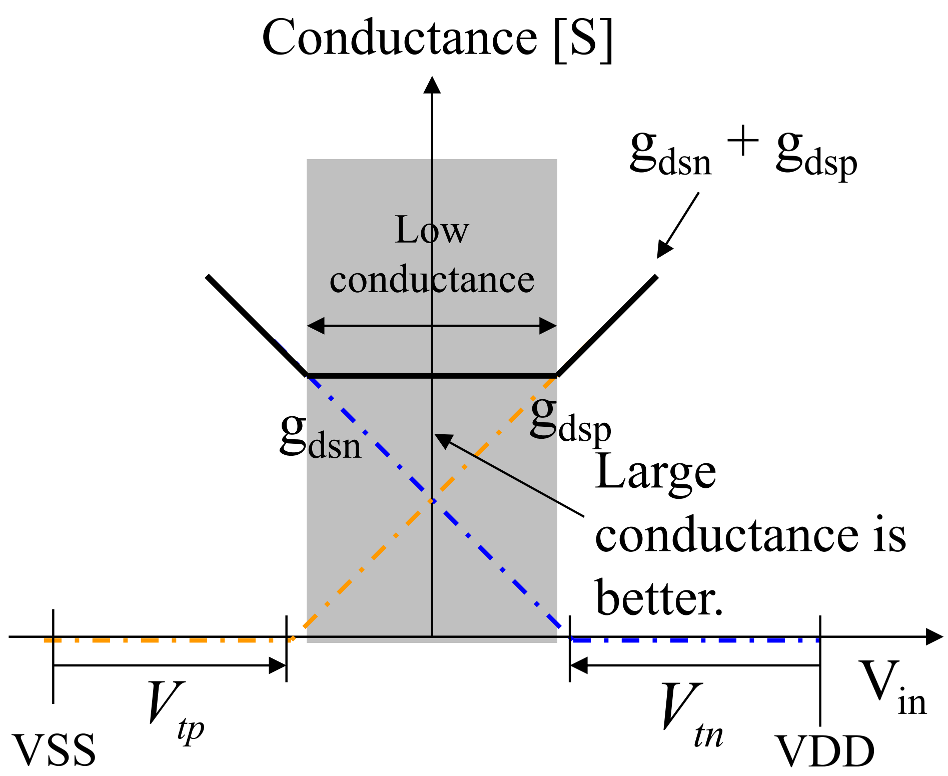
$$I_{dsn} = \beta_n \{(V_{gsn} - V_{Tn}) \cdot V_{dsn} - \frac{1}{2} V_{dsn}{}^2\}$$

$$= \beta_n \{(VDD - V_{in} - V_{Tn}) \cdot V_{in} - \frac{1}{2} V_{in}{}^2\}$$

$$g_{dsn} = \frac{1}{r_{dsn}} = \frac{\partial I_{dsn}}{\partial V_{in}} = \underline{\beta_n} \{(VDD - V_{Tn}) - 3V_{in}\}$$

p-ch MOSFET

$$g_{dsp} = \frac{1}{r_{dsp}} = \frac{\partial I_{dsp}}{\partial V_{in}} = \underline{\beta_p} \{(V_{Tp} - VSS) + 3V_{in}\}$$



Minimum conductance is degraded by the low power supply voltage and high V_{Tn} and V_{Tp}.

ON-resistance of analog switch

Quiz:

Find a ON-resistance of CMOS Switch, assuming that $|V_{Tp}| = V_{Tn} = 0.3(VDD - VSS)$、$\mu_p C_{OX} = 100$ (mA/V^2) , and VDD - VSS = 0.5 (V).

Answer:

Minimum conductance of CMOS switch is observed at $V_{in} = 0$ V, the conductance is minimum, assuming that $\beta_n = \beta_p$.

$$g_{dsn} + g_{dsp} = \beta_n\{(VDD - V_{Tn}) - 3V_{in}\} + \beta_p\{(V_{Tp} - VSS) + 3V_{in}\}$$

$$= \beta_p\{(VDD - VSS) - \beta_p \cdot 0.3(VDD - VSS)\}$$

$$= 0.7\beta_p(VDD - VSS)$$

$$= 0.35\beta_p = 35\frac{W_p}{L_p}\mu S$$

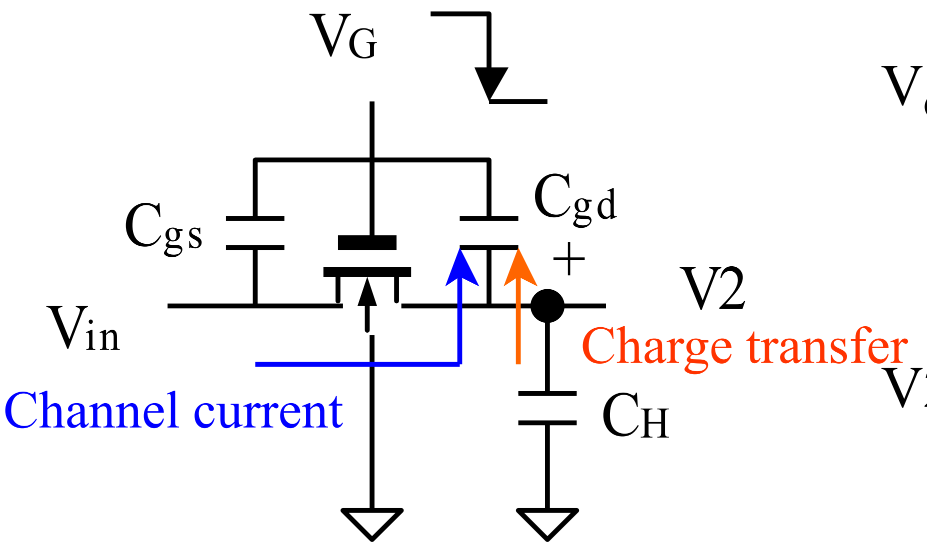
$$R_{ON} = \frac{1}{g_{dsn} + g_{dsp}} = 29\frac{L_p}{W_p}k\Omega$$

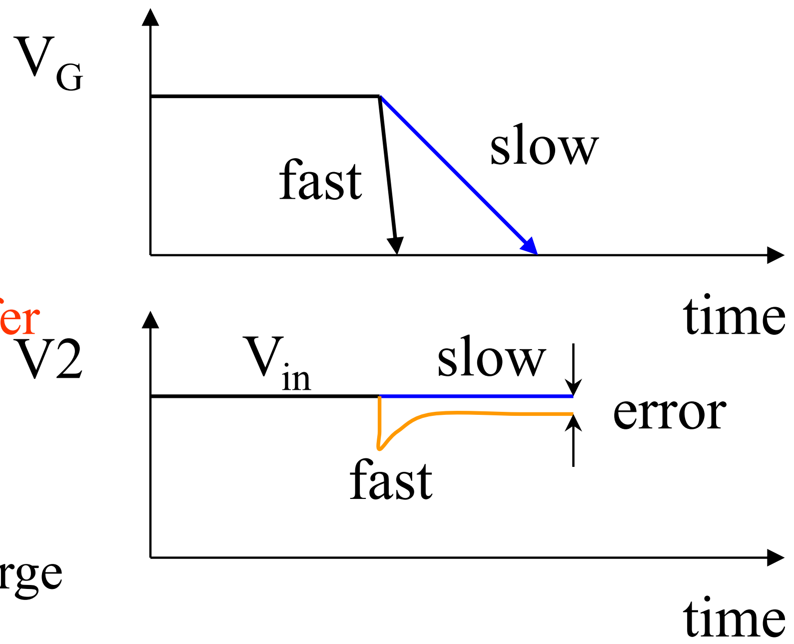
Set W_n and W_p to make V_{in} dependence of the conductance a symmetry for positive and negative voltage.

NOTE: Normally, R_{ON} = ~10kΩ*(L/W)

Clock feedthrough error

The error is raised by the charge transfer from the sampling capacitor to the parasitic capacitance of MOSFET $\propto$ L.

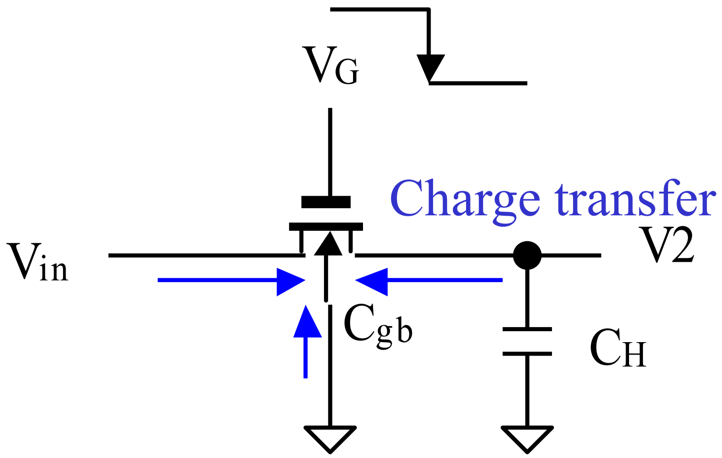


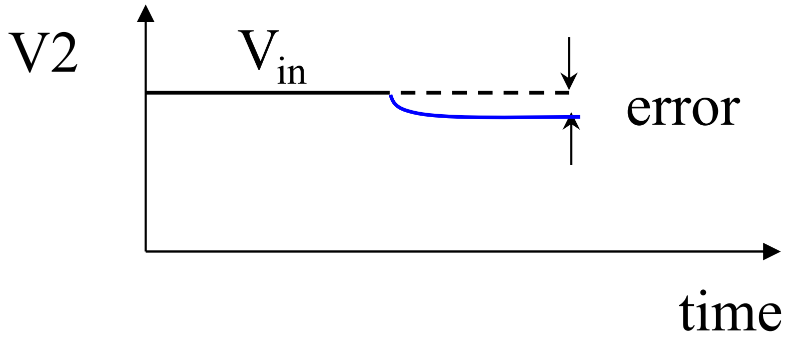


If V_G is fallen suddenly (ON→OFF), the charge of C_H is partially transferred to C_{gd} and V2 is decreased.

Charge injection error

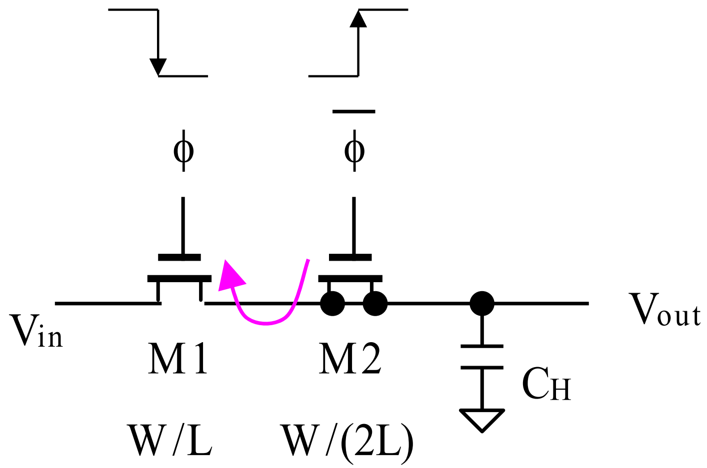
The error is raised by the charge transfer from the sampling capacitor to the channel of MOSFET $\propto$ LW.



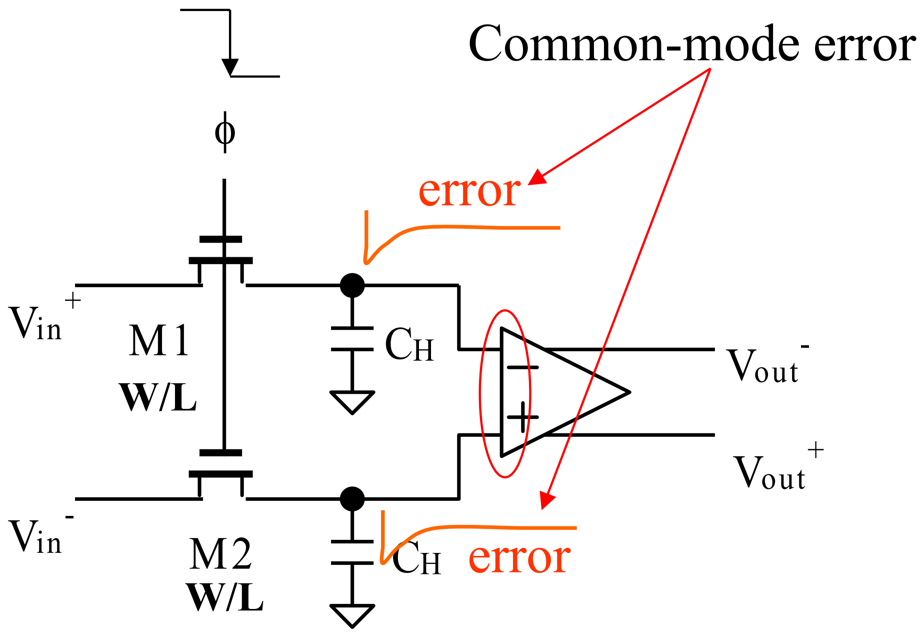


When the carrier in the channel of MOSFET recombine, the charge is injected from C_H and V2 is decreased.

Cancellation of errors



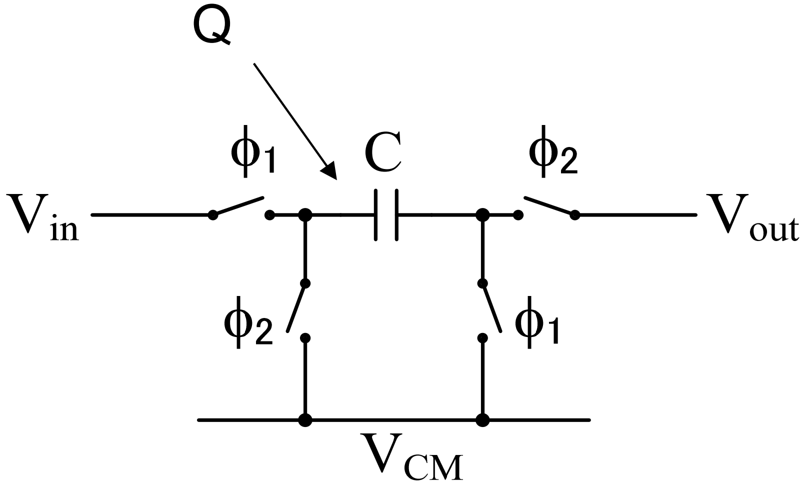
1. Withdraw from a dummy switch



2. Set-off of the common-mode error with the differential amplifier

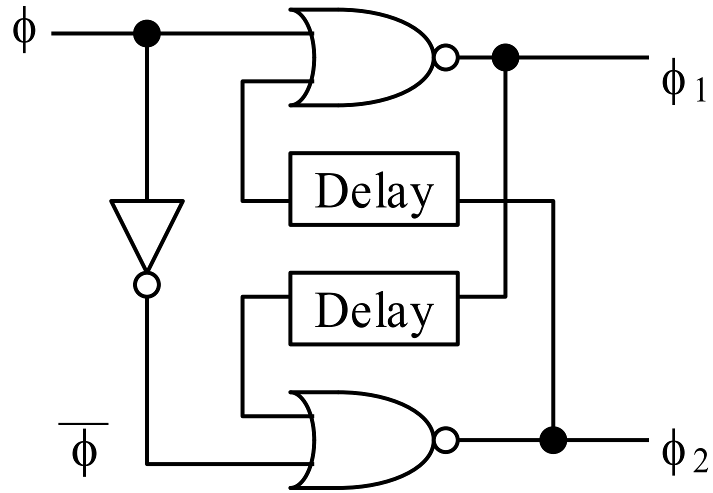
15.2 Clock circuit

Non-overlapping clock generation

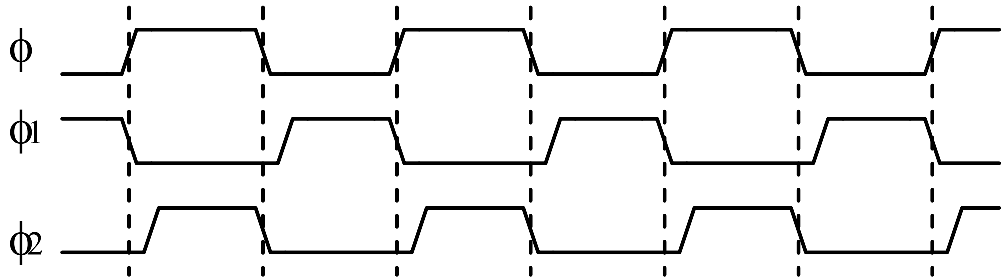


ϕ1: V_{in} = Q/C (Sampling of input voltage)
ϕ2: V_{out} = -Q/C (Inversion and output)

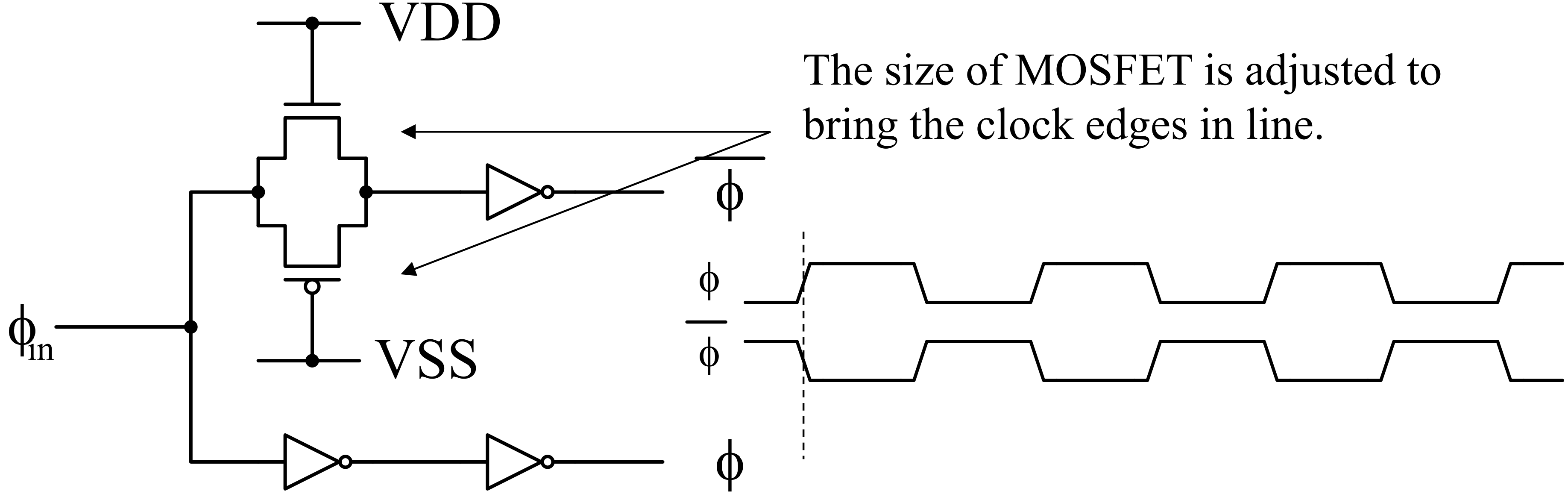
Non-overlapping Clock Generator



Even if only slightly 'H' level of ϕ1 and ϕ2 is overlapped, the sampled charge Q is leaked to VCM line. The non-overlapped clock signals is employed for the ϕ1 and ϕ2.



Complementary clock generation

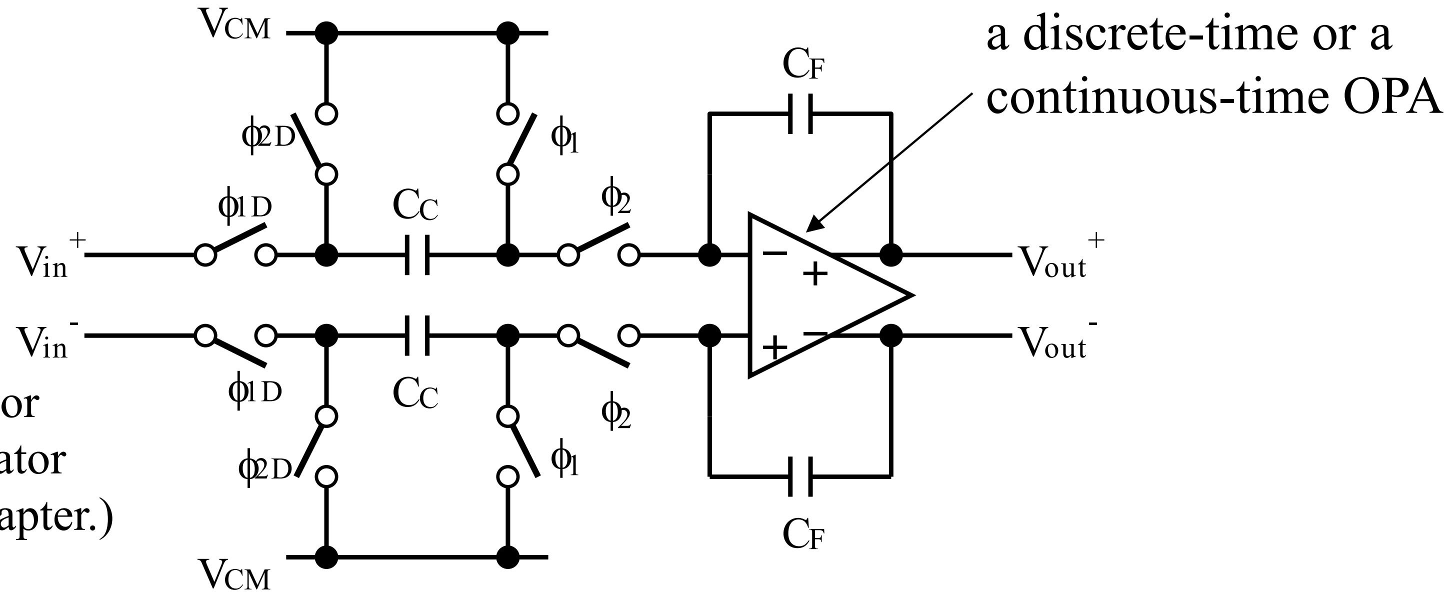


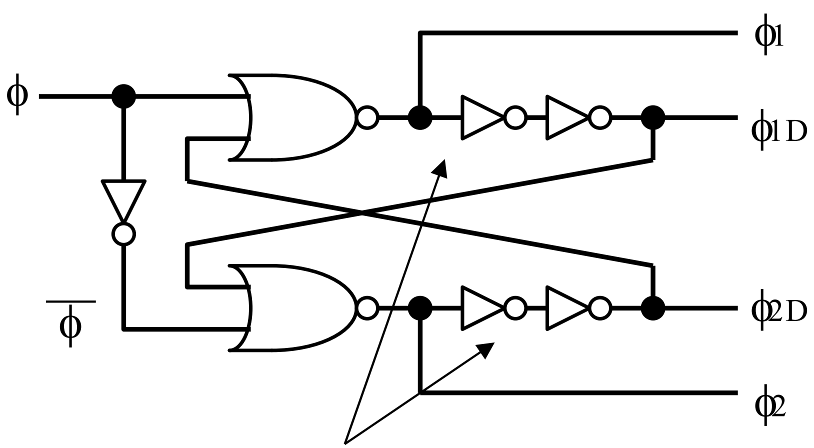
A complementary clock generation circuit is employed to generate the 2-phase clock without a timing error.

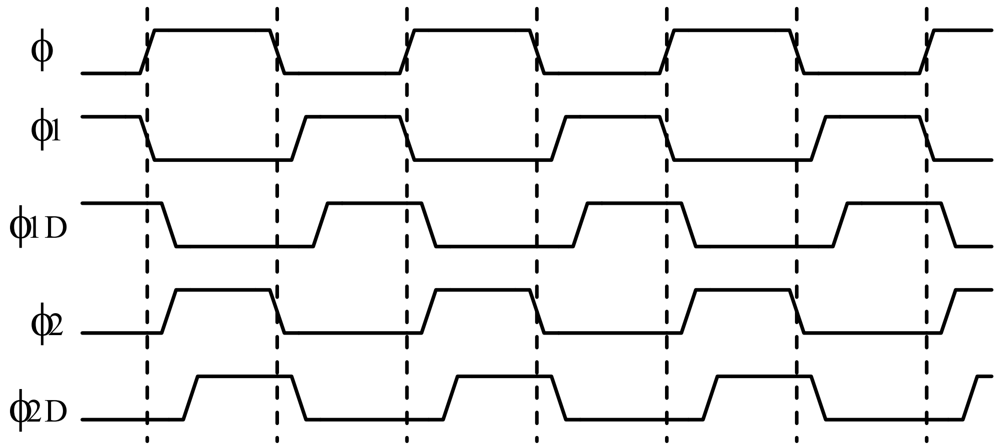
Application example of Non-overlapping Clock

SC DAI

(The switched capacitor discrete analog integrator will appear in next chapter.)







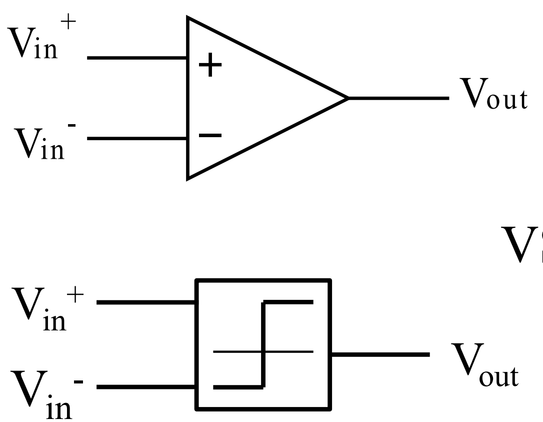
The delay time is adjusted by the number of stages.

15.3 Clocked comparator

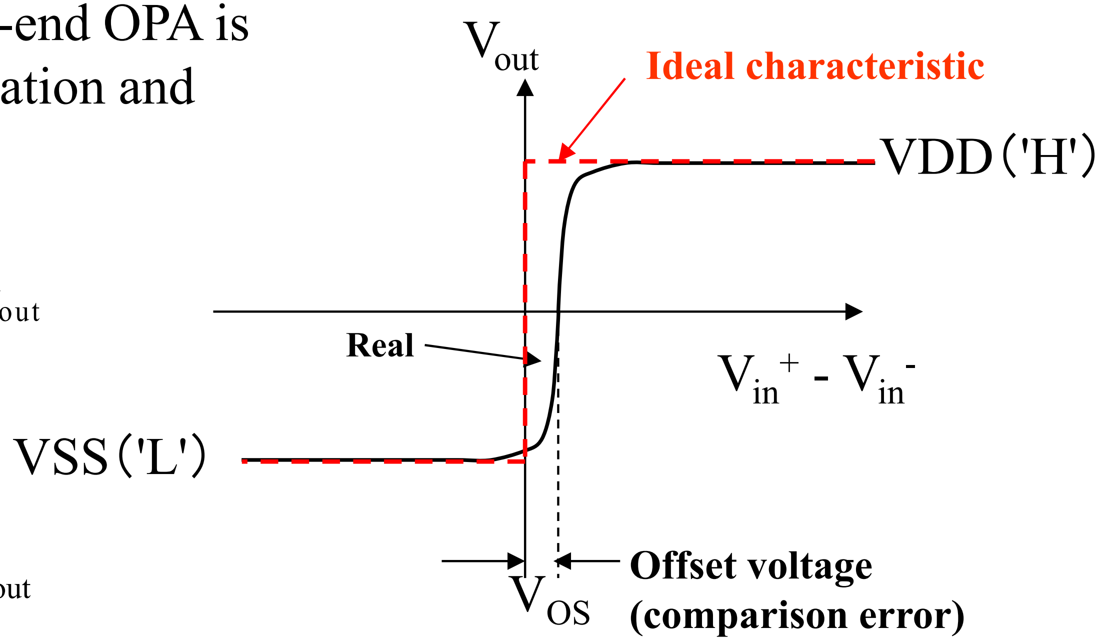
Function of analog comparator

- If ($V_{in}^{+} > V_{in}^{-}$), then V_{out} = VDD (Logic level = 'H')
- If ($V_{in}^{+} < V_{in}^{-}$)，then V_{out} = VSS (Logic level = 'L')

The same symbol as a single-end OPA is used, but the circuit configuration and function is different.



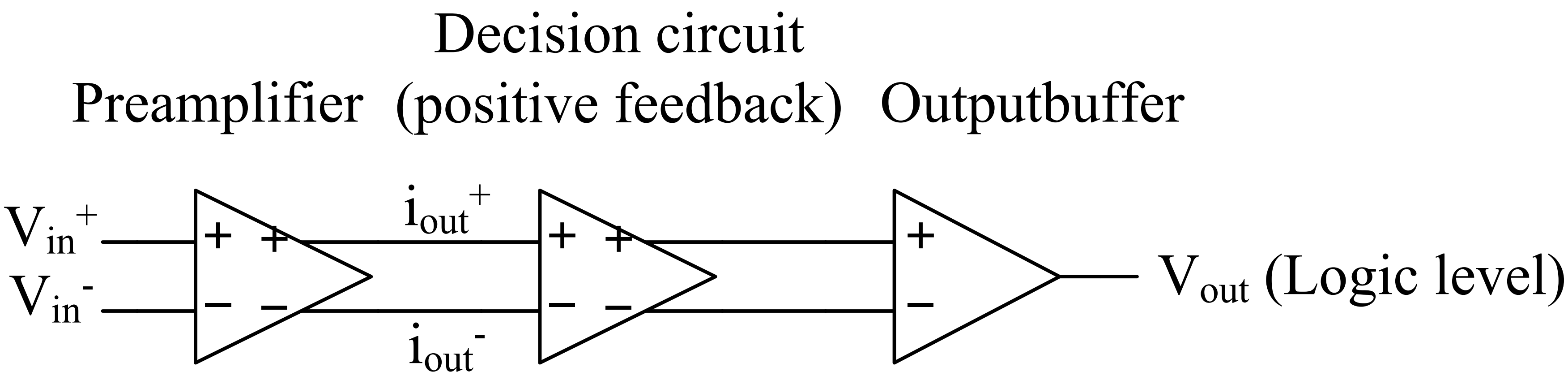
Symbol



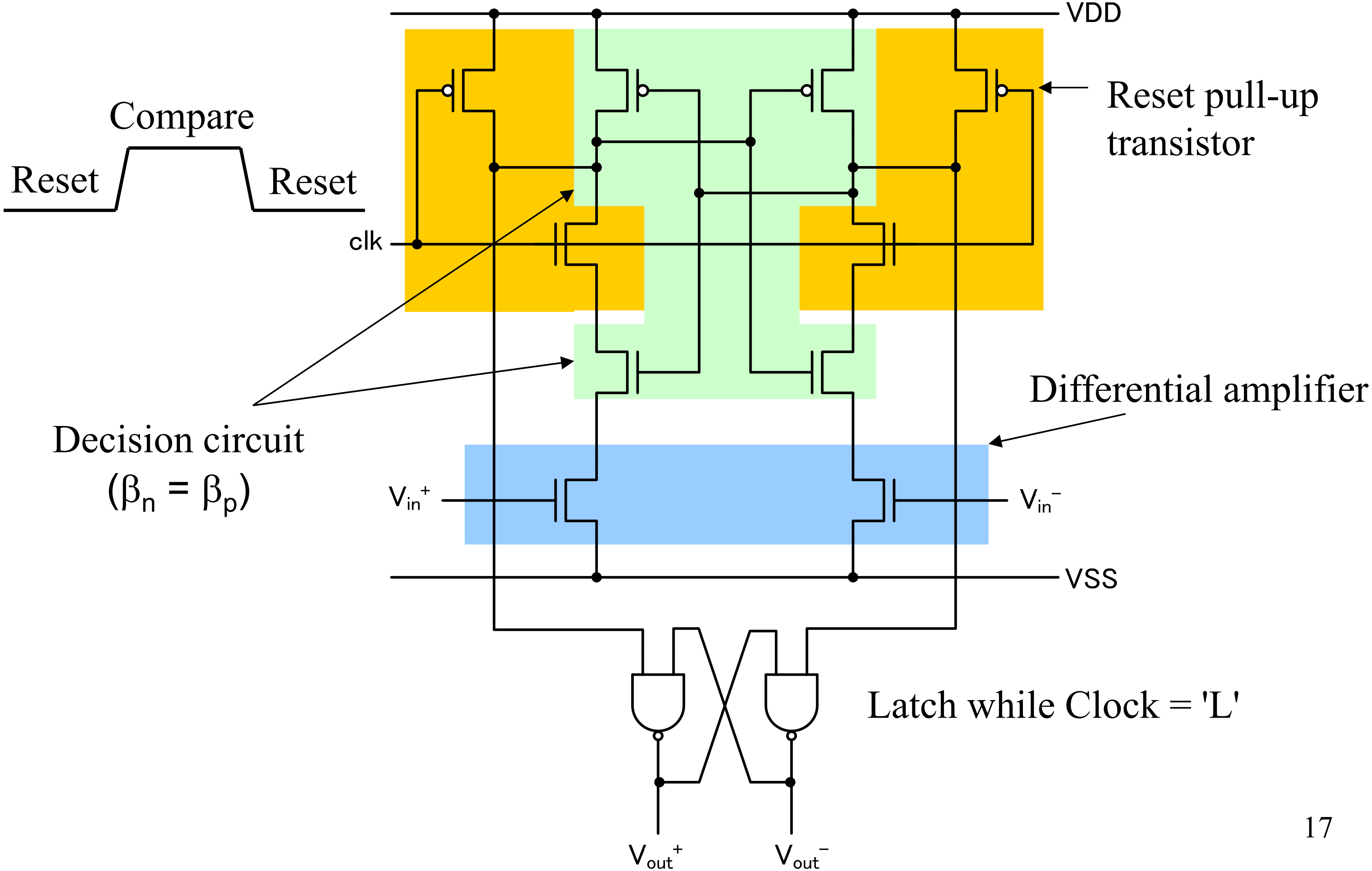
Specification of a comparator

Parameter	Design constraint	Description
VDD/VSS	max/typ/min	
I_{BIAS}	max	
I_{ACTIVE}	max	dependent on the clock frequency
f_S	typ	Clock frequency
Common-mode input range	min/max	
Input-referred offset V_{OS}	max	$V_{OS} << V_{LSB}/2$
Gain	min	Gain >> $(VDD - VSS)/V_{LSB}$
Settling time	max	>> f_S
Load capacitance	typ	

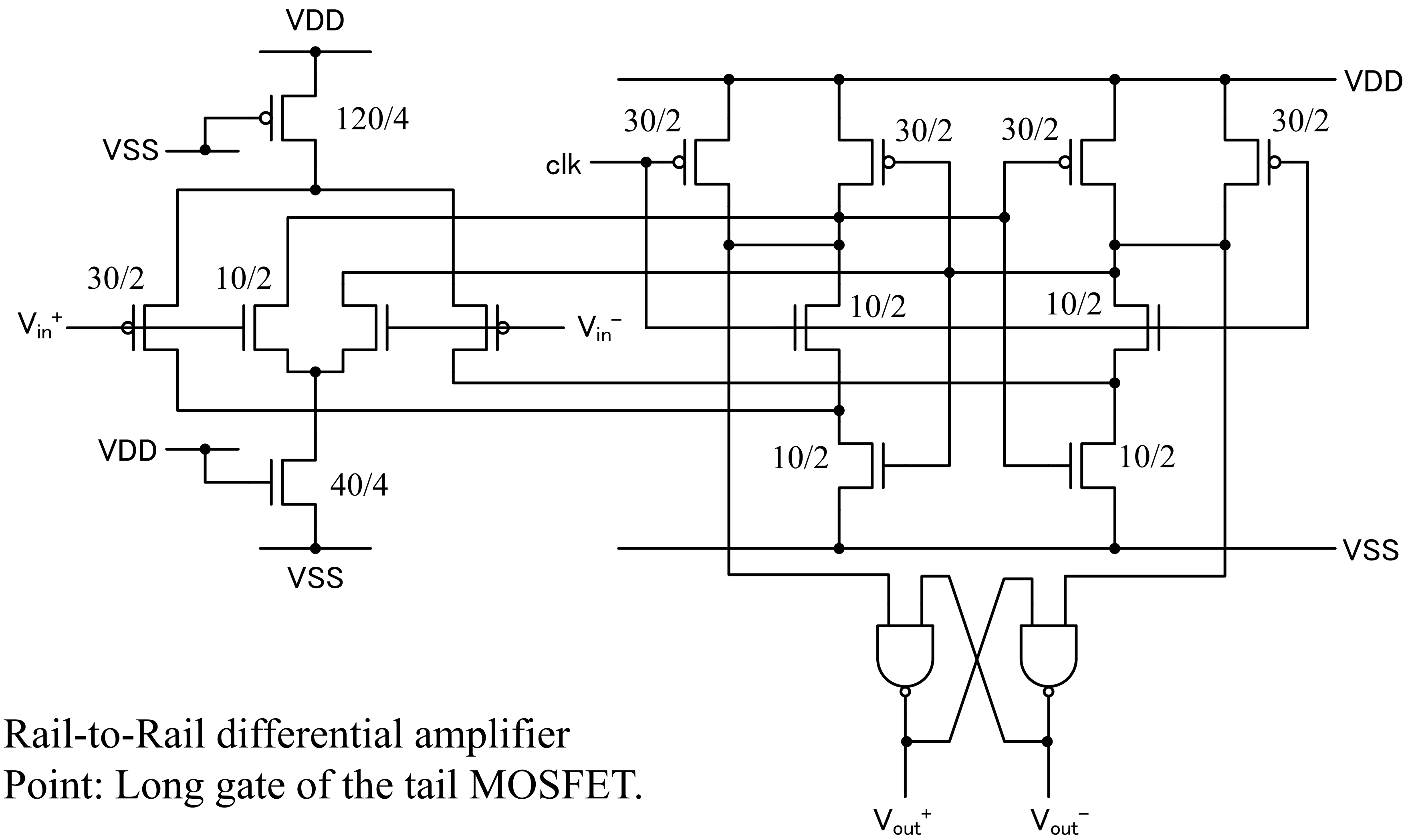
Block diagram of a comparator



Clocked Comparator (Sens. amp.)



Wide Swing Comparator



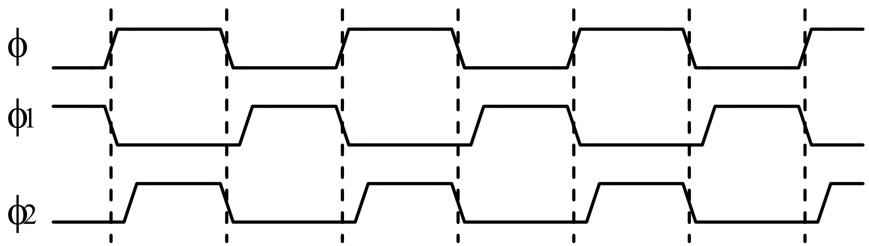
Rail-to-Rail differential amplifier
Point: Long gate of the tail MOSFET.

15.4 Dynamic comparator

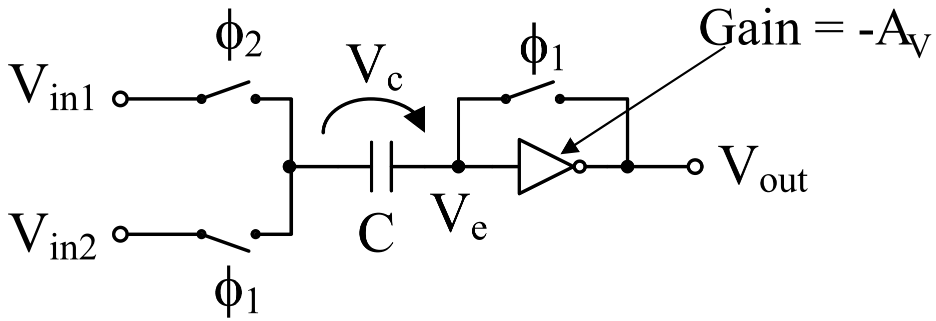
Dynamic comparator

- Small area
- High precision (self-reference)
- Wide input range
- Cancelling noise and drift in lower frequency than the clock frequency

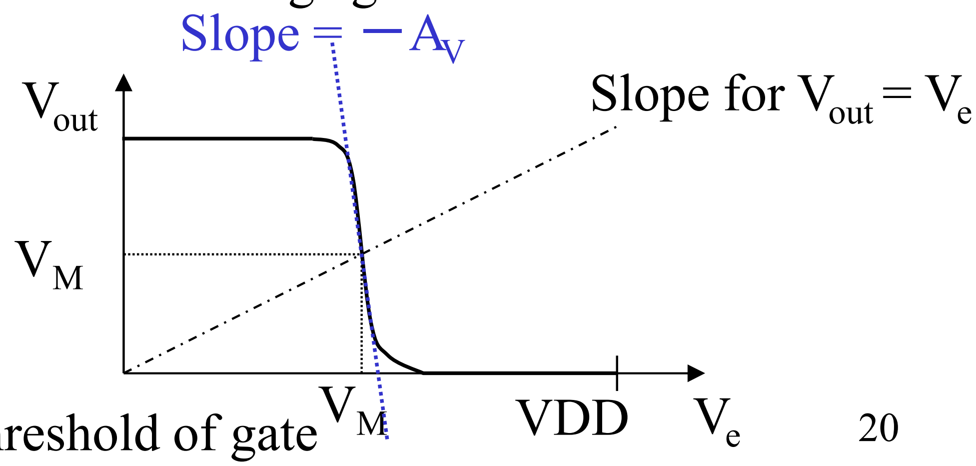
Non-Overlapping Clock



Clock phase	State
ϕ_1	Sample V_{in}^{-}
ϕ_2	Compare with V_{in}^{+}

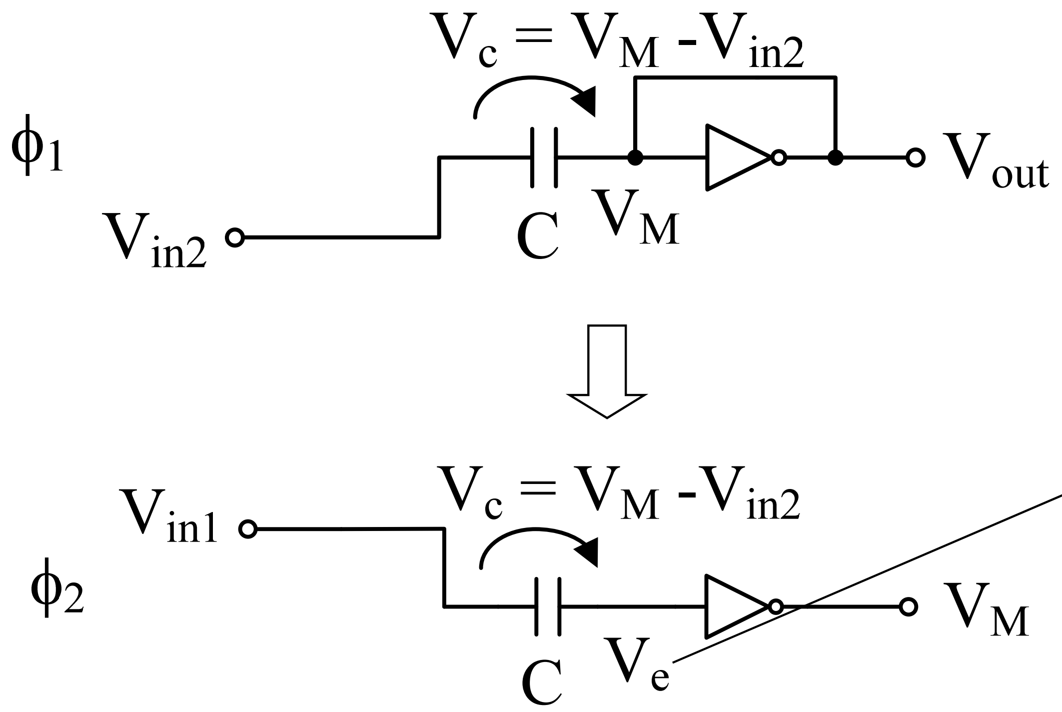


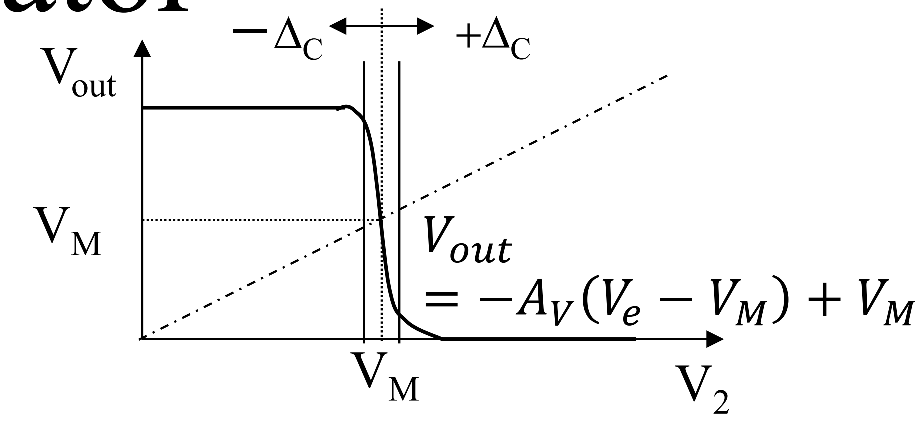
Voltage gain of a inverter



V_M: Threshold of gate

Operation of the dynamic comparator

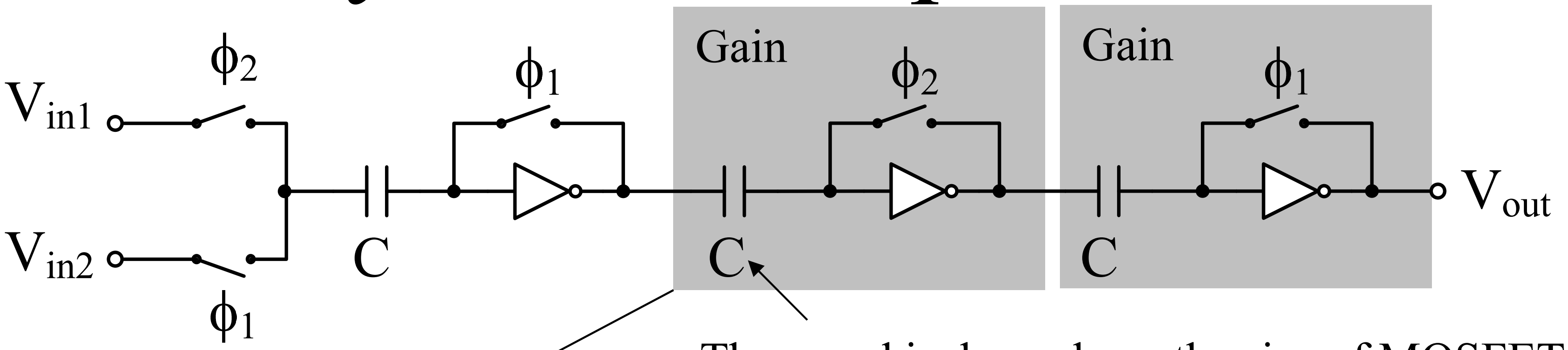




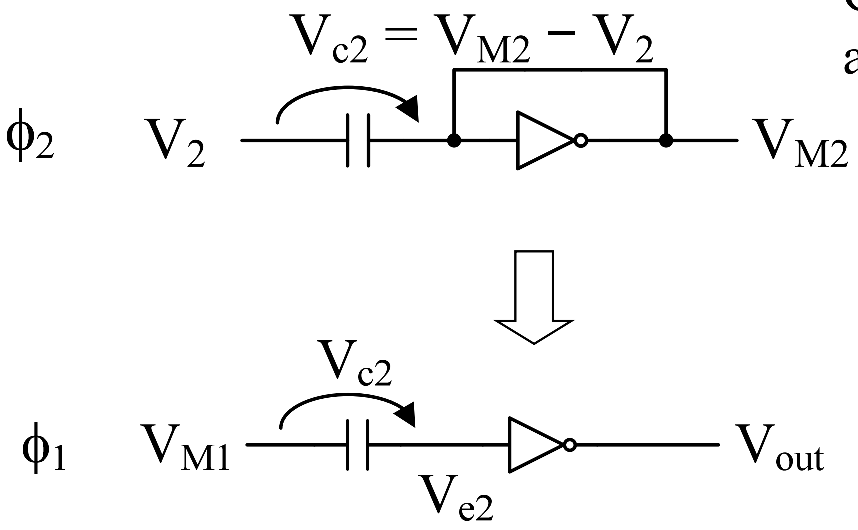
$$V_e = V_{in1} + V_C$$
$$= V_{in1} + V_M - V_{in2}$$
$$\equiv \Delta + V_M$$
$$V_{out} = -A_V(V_e - V_M) + V_M$$
$$= -A_V \cdot \Delta + V_M$$

If the threshold voltage V_M of the inverter is fluctuated, the fluctuation of the offset voltage is negligible. Because only a comparison result Δ is amplified. The voltage gain of inverter A_V is normally low (~20dB). The gain od the comparator can be increased by using additional inverter stage.

Practical implementation of the dynamic comparator

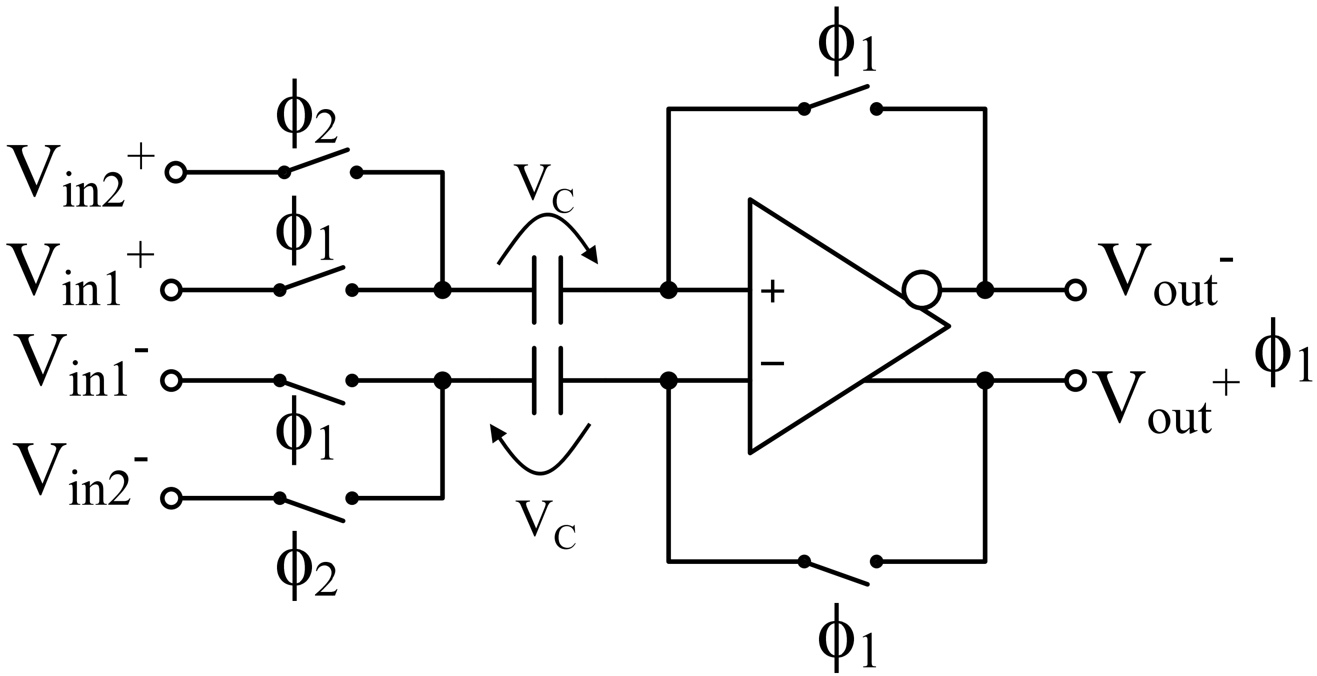


The speed is depends on the size of MOSFET and C, but the small capacitance suffers the kT/C noise and charge injection error of CMOS switch.



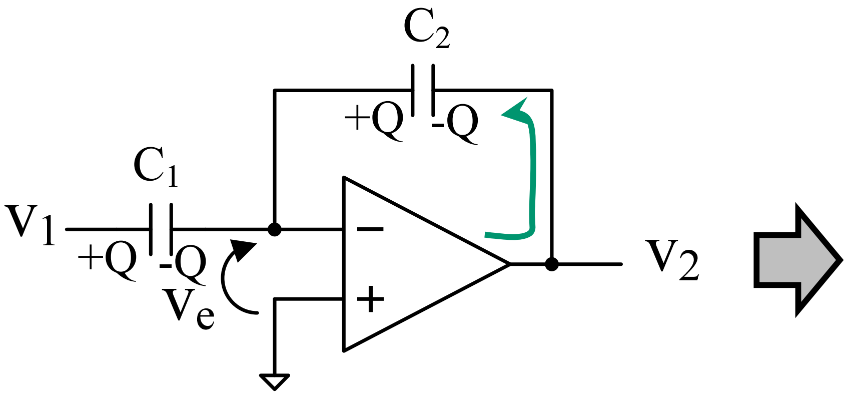
$$
\begin{aligned}
V_2 &= -A_V \cdot \Delta + V_{M1} \\
V_{c2} &= V_{M2} - V_2 = V_{M2} + A_V \cdot \Delta - V_{M1} \\
V_{e2} &= V_{M1} + V_{c2} = V_{M1} + V_{M2} + A_V \cdot \Delta - V_{M1} \\
&\equiv A_V \cdot \Delta + V_{M2} \\
V_{out} &= -A_V (V_{e2} - V_{M2}) \\
&= -A_V (A_V \cdot \Delta + V_{M2} - V_{M2}) + V_{M2} \\
&= -A_V^2 \cdot \Delta + V_{M2}
\end{aligned}
$$

Full-differential dynamic comparator

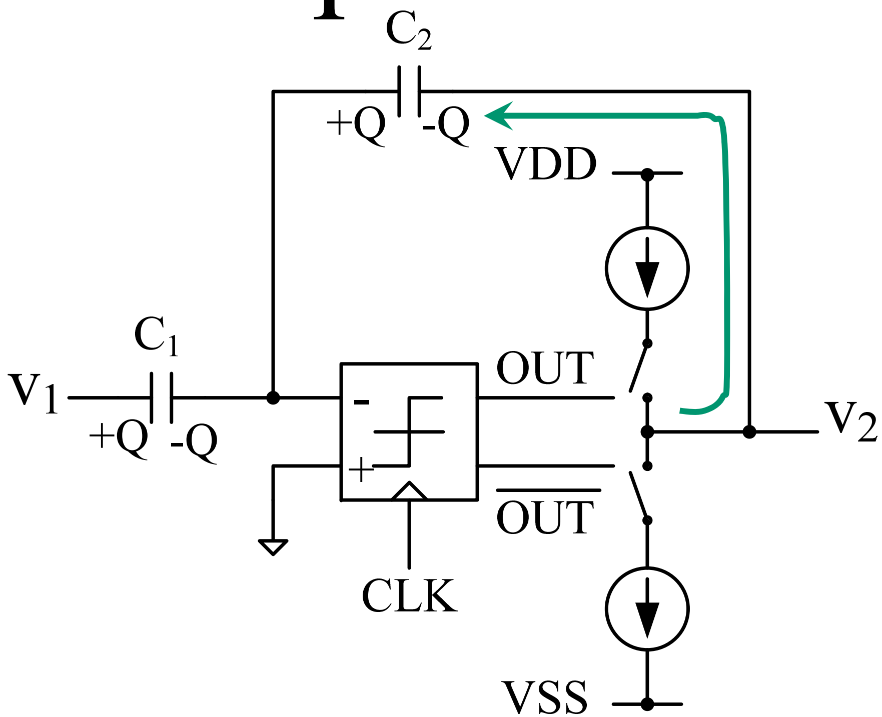


Clock phase	State
ϕ_1	Sample V_1
ϕ_2	Compare with V_2

Discrete-time operational amplifier with comparator



The output voltage V_2 is regulated to keep the virtual ground, i.e. $V_e = 0$.



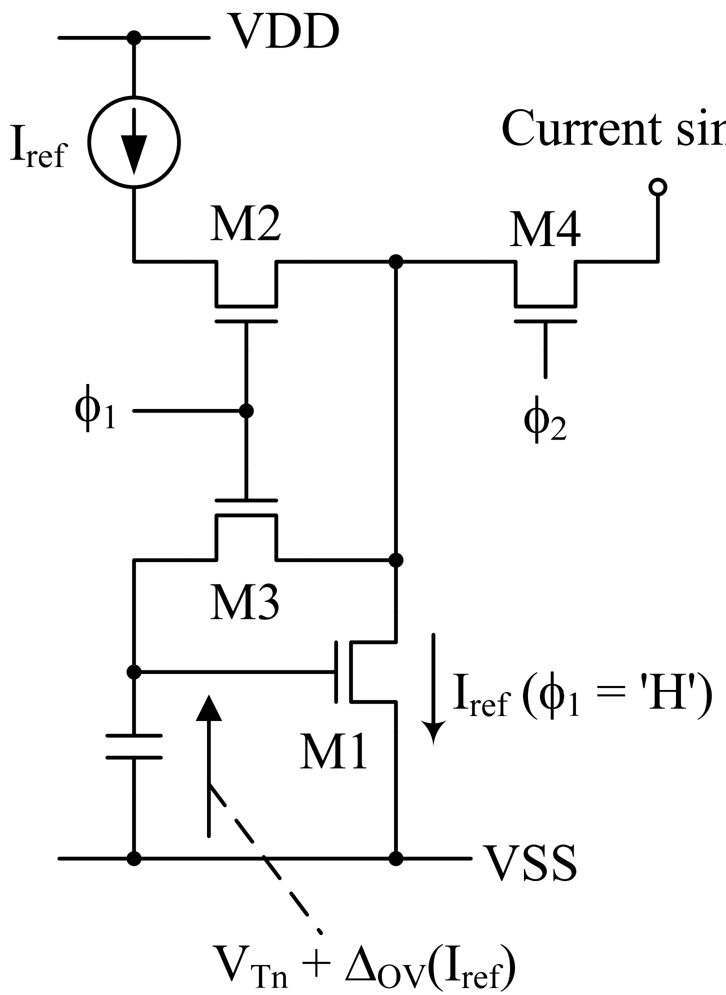
Equivalent circuit with comparator

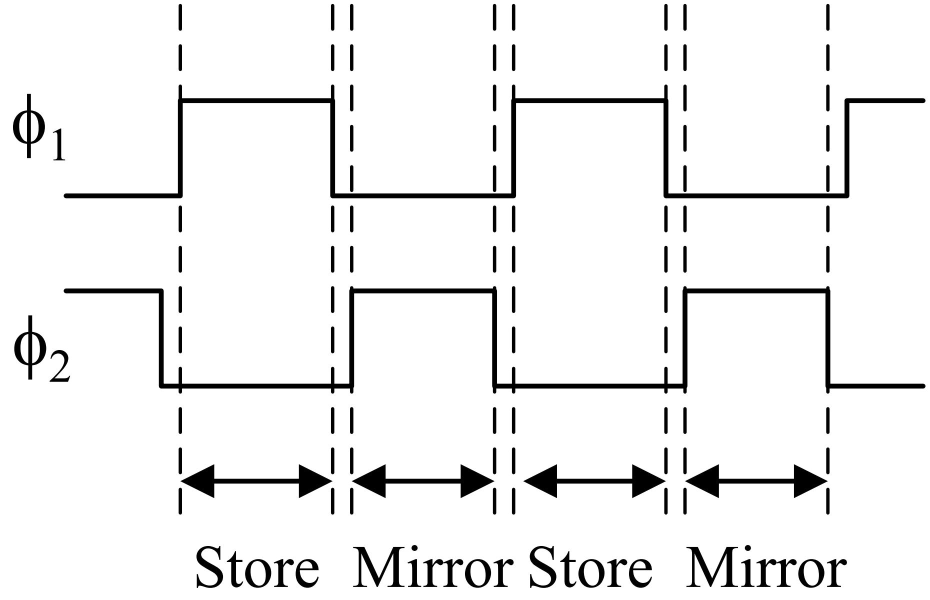
The discrete time OPA can be replaced with high-precision comparator to implement the differential amplifier, because it is difficult to design the high gain OPA with the fine processes.

15.5 Dynamic amplifier

Dynamic analog circuits can avoid a mismatch error of MOSFET.

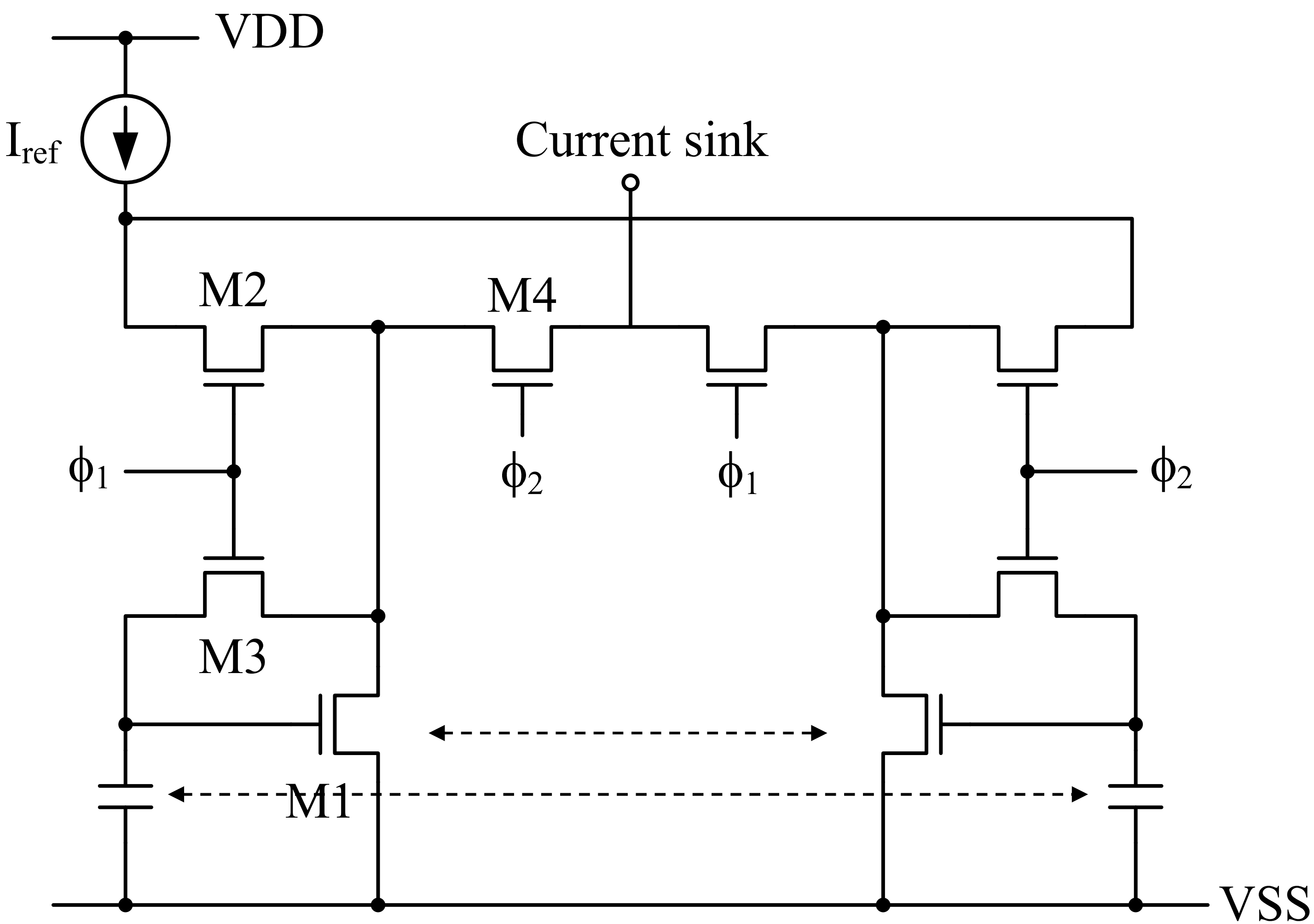
Discrete time dynamic current mirror





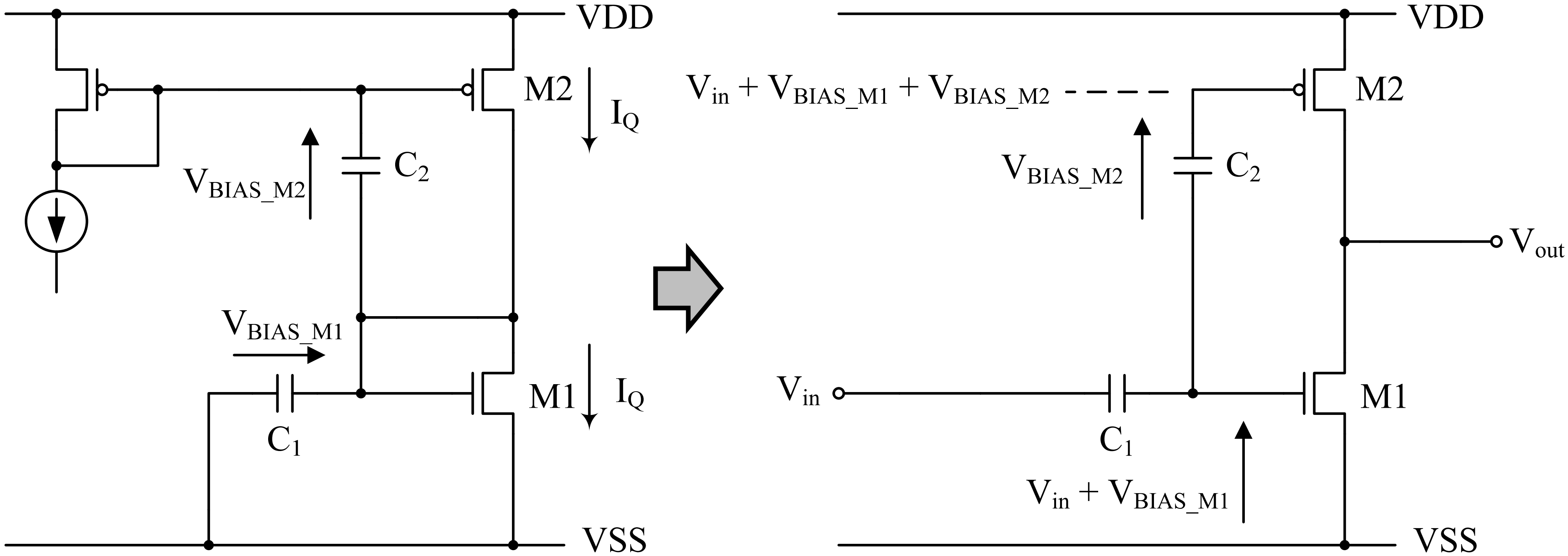
There is no mismatch error because the M1 is used for a constant voltage source and a current sink.

Continuous time dynamic current mirror



Matching of M1 and C are not required.

Dynamic class-AB amplifier

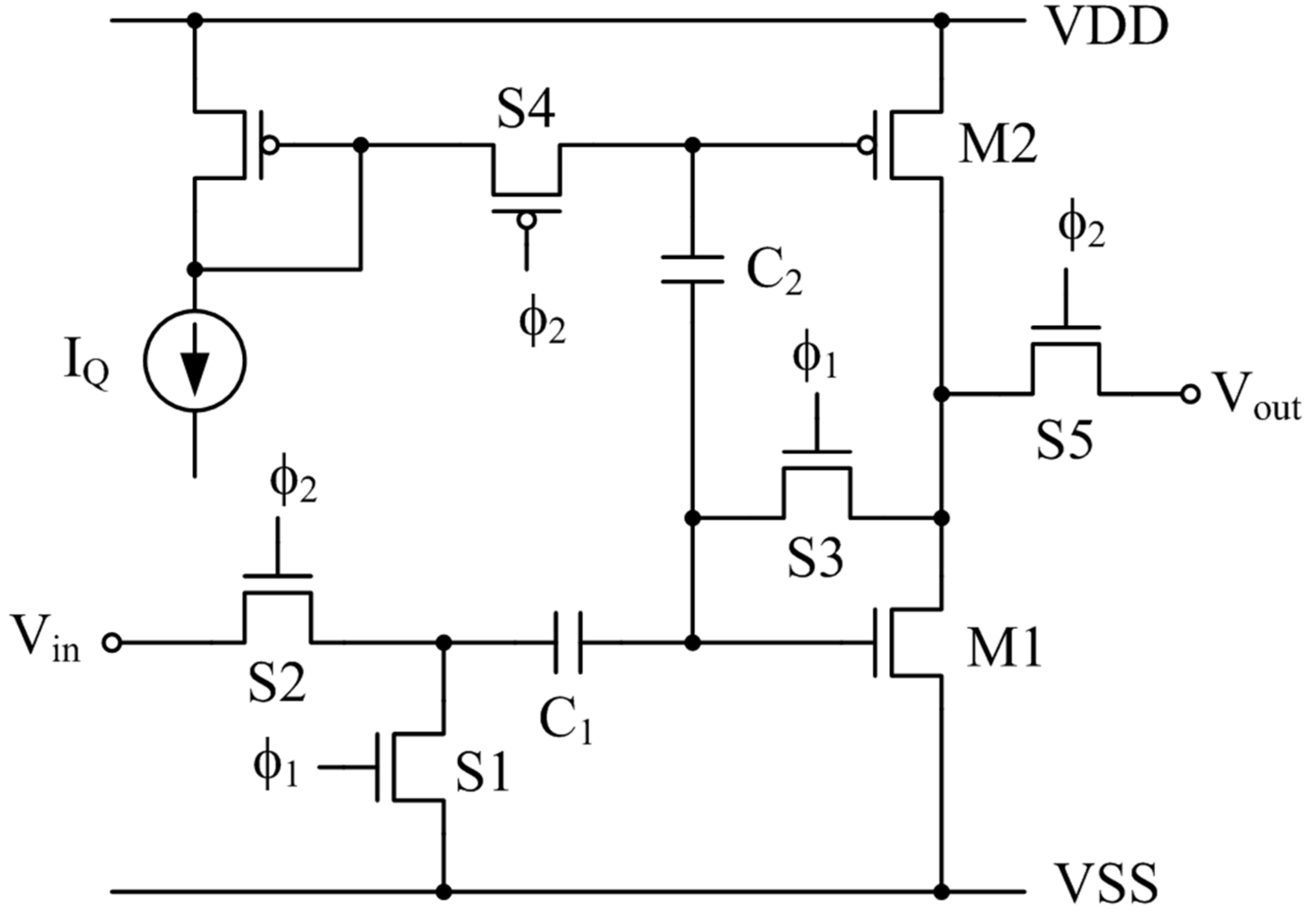


ϕ1: Storing phase of the bias condition for the quiescent current.

ϕ2: Amplification phase.

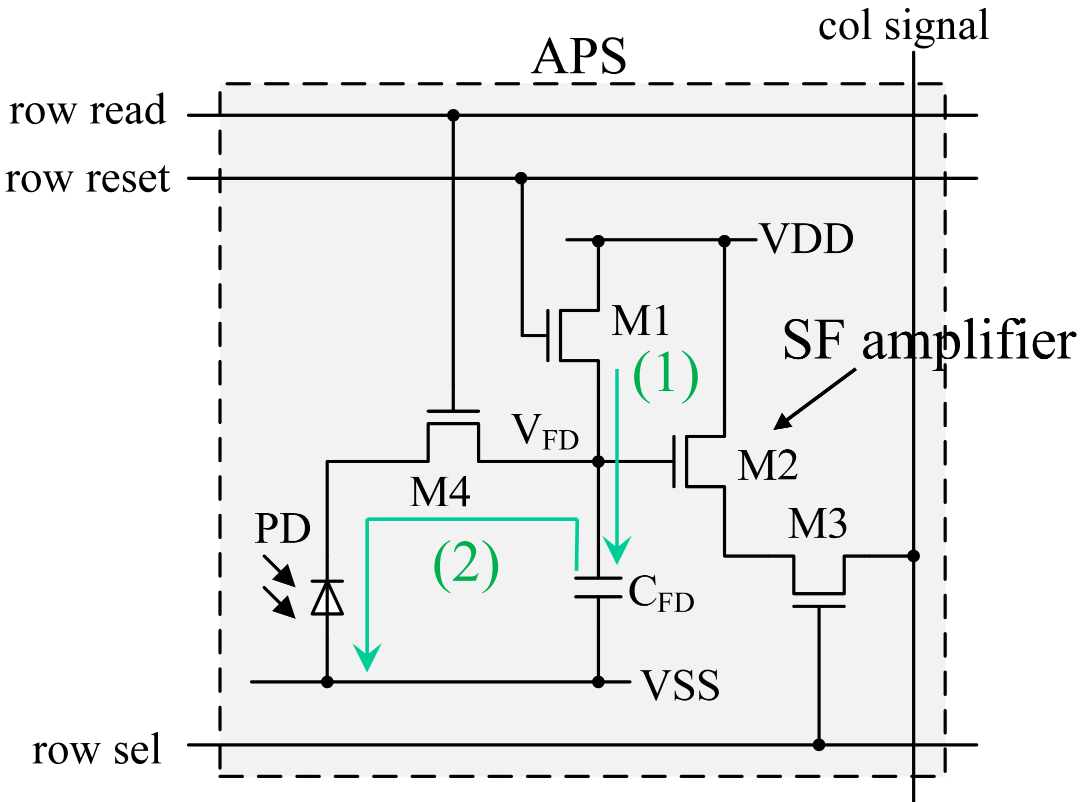
The biasing scheme makes the amplifier less sensitive to V_T and VDD variations.

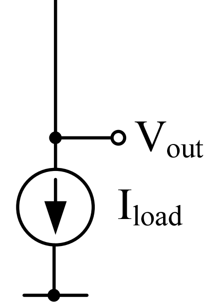
Example of dynamic class-AB amplifier

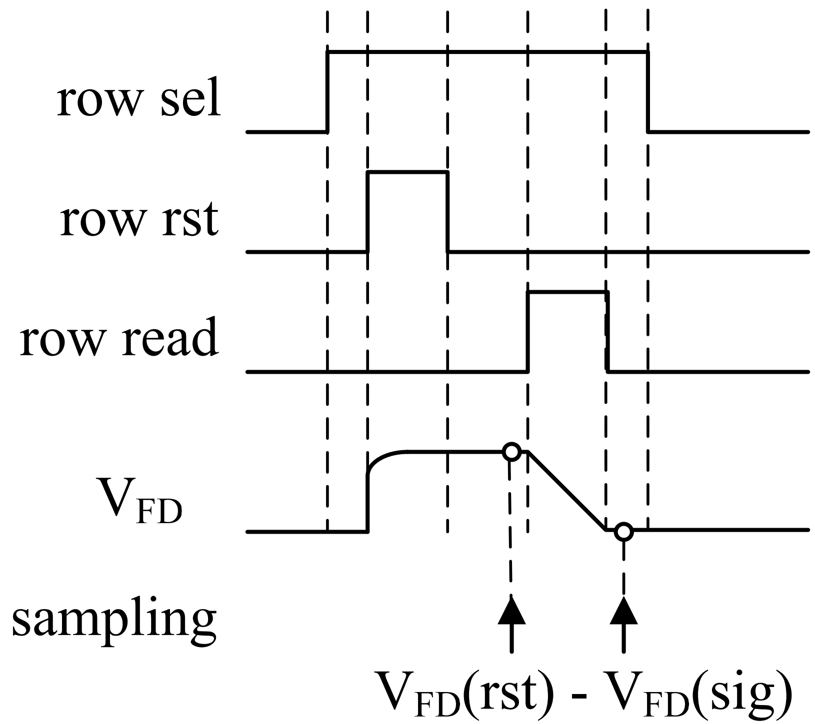


15.6 Active pixel sensor (APS)

4T active pixel sensor





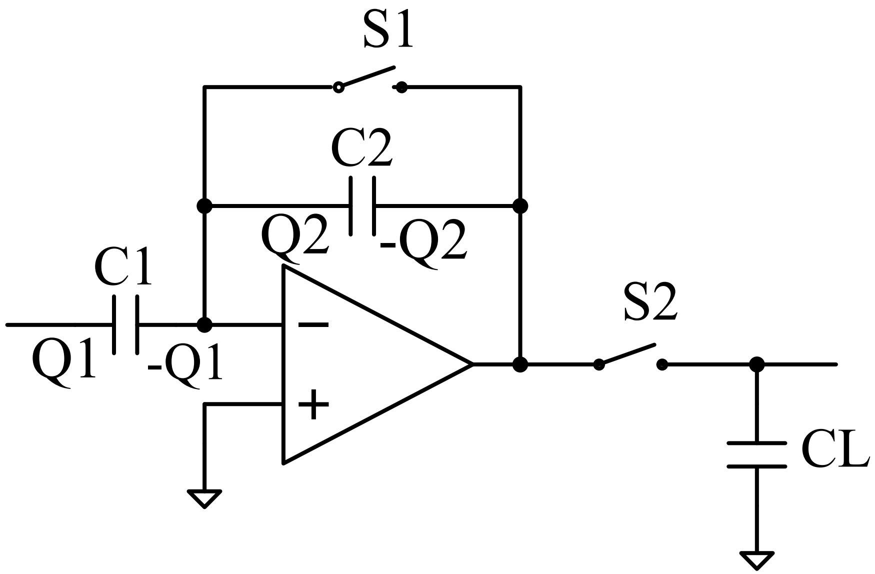


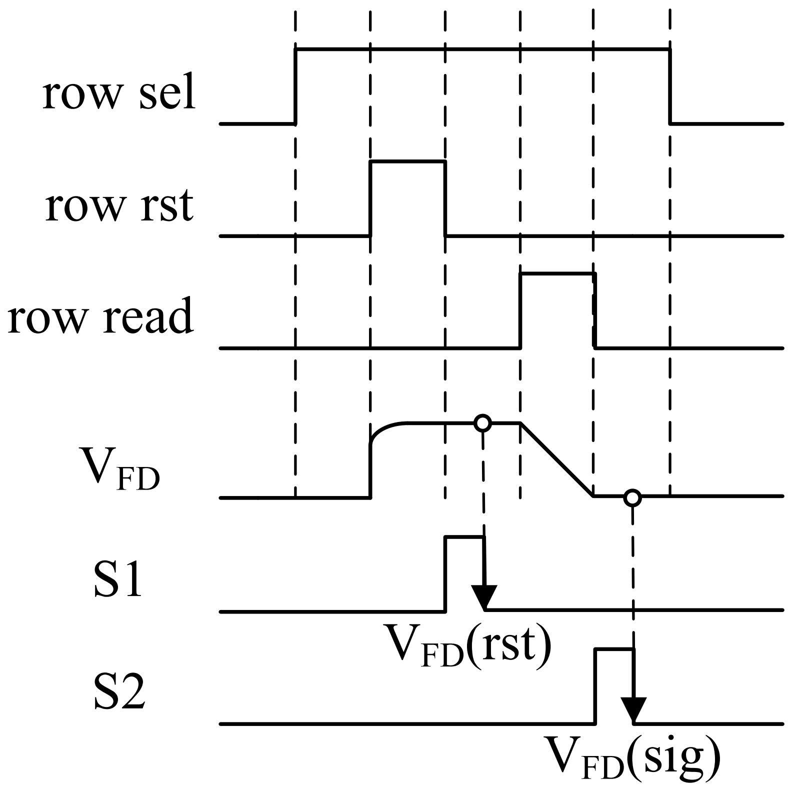
(1) Pre-charge of VDD - V_{Tn}

(2) Charge transfer proportional to the photo-current

Correlated double sampling

The fixed pattern noise (process variation) and switching noise are canceled by each correlated double sampling.





$$\begin{cases} S1 = \text{ON: } Q1 = C1V_{rst},\ Q2 = 0 \\ S1 = \text{OFF: } Q1' = C1V_{sig},\ Q2' = Q1 - Q1' \end{cases}$$

$$V_{out} = \frac{C1}{C2}(V_{sig} - V_{rst})$$