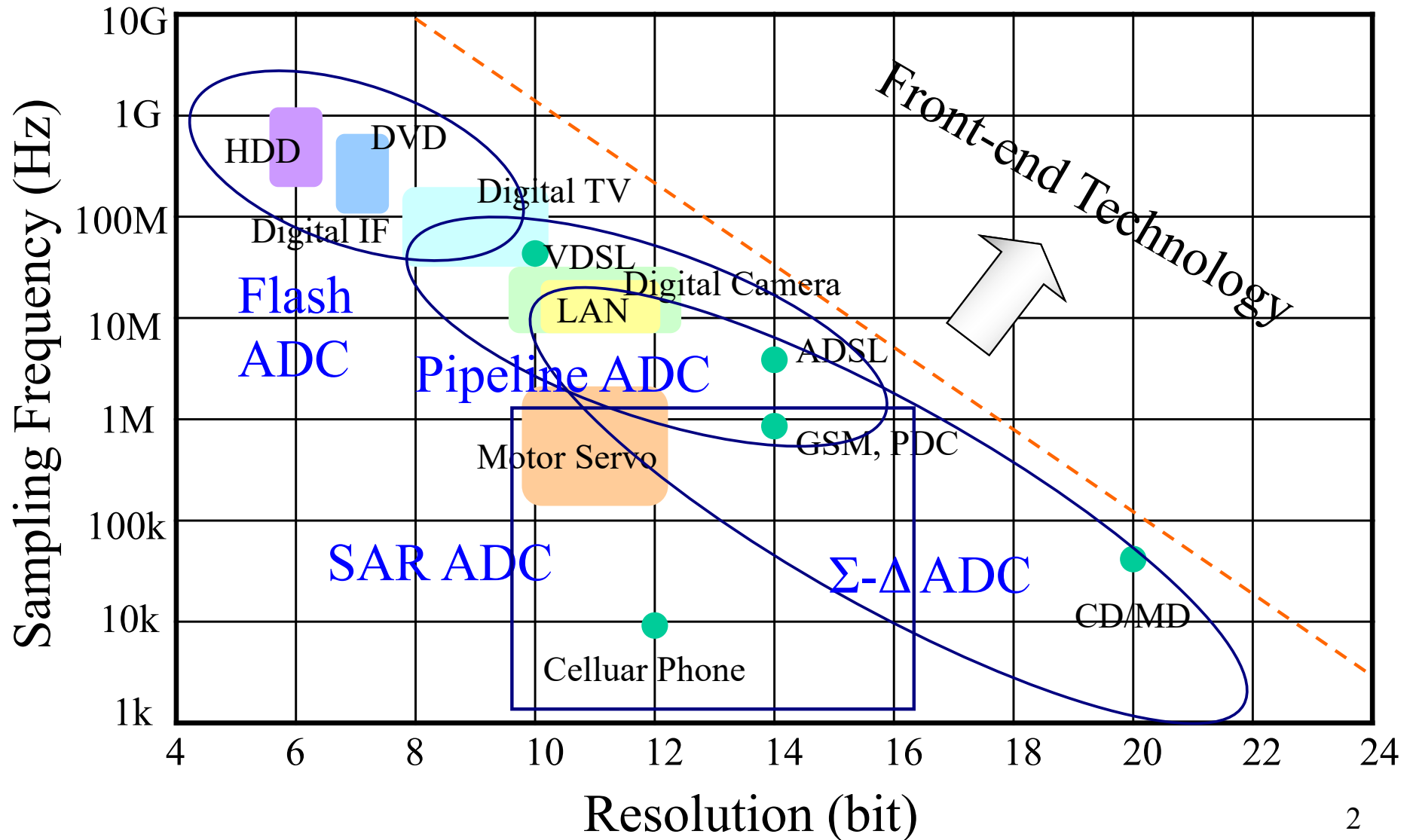


4. Data converters 1

(Oversampling converters)

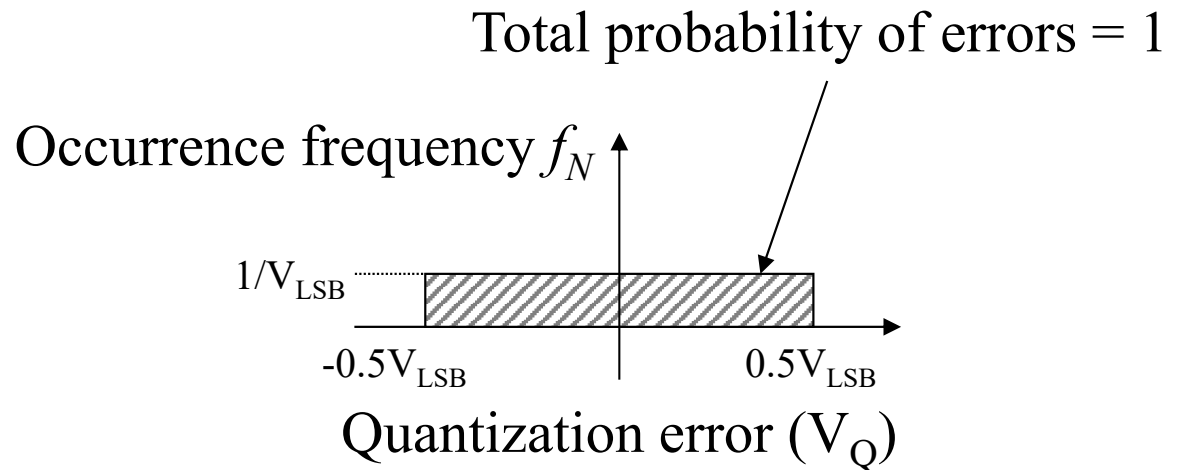
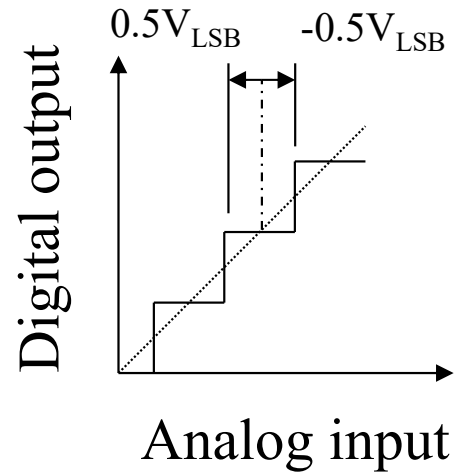
Kanazawa University
Microelectronics Research Lab.
Akio Kitagawa

Performance of ADC architecture



4.1 Quantization noise and noise shaping

Quantization noise



N-bit quantization $\Rightarrow V_{max} = (2^N - 1)V_{LSB}$

Noise level $V_{Q_RMS} = \sqrt{\int_{-\infty}^{\infty} V_Q^2 f_N(V_Q) dV_Q} = \sqrt{\frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{0.5V_{LSB}} V_Q^2 dV_Q} = \frac{V_{LSB}}{2\sqrt{3}}$

Maximum Signal level $V_{max_RMS} = \sqrt{\int_{-\infty}^{\infty} V_S^2 dV_S} = \frac{V_{max}}{2\sqrt{2}} = \frac{(2^N - 1)V_{LSB}}{2\sqrt{2}}$

SNR of quantized signal

$$SNR(\text{dB}) = 10\log \frac{V_{\text{max_RMS}}^2}{V_{\text{Q_RMS}}^2} = 10\log \frac{\left(\frac{2^N - 1}{2\sqrt{2}} V_{\text{LSB}}\right)^2}{\left(\frac{1}{2\sqrt{3}} V_{\text{LSB}}\right)^2} = 20\log \sqrt{\frac{3}{2}} (2^N - 1)$$
$$\approx 20\log 2^N + 20\log \sqrt{\frac{3}{2}} \approx 6.02N + 1.76 \text{ (dB)}$$

Quantization noise by oversampling

Assuming that the quantization error generates the white noise,

Noise power spectrum density $PDS_Q = \frac{V_{Q_RMS}^2}{f_s} = \frac{\left(\frac{V_{LSB}}{2\sqrt{3}}\right)^2}{f_s} = \frac{V_{LSB}^2}{12f_s}$

Noise power level in band $P_{Q_RMS} = \int_{-f_0}^{f_0} PSD_Q df = \frac{V_{LSB}^2}{12f_s} 2f_0 = \frac{V_{LSB}^2}{12} \frac{1}{OSR}$

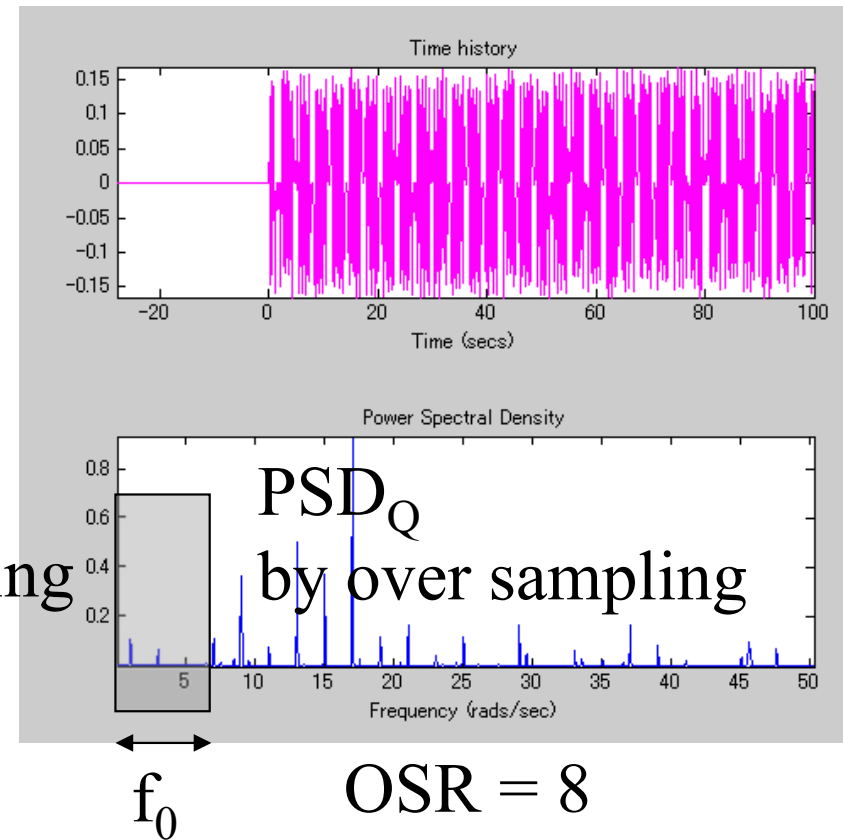
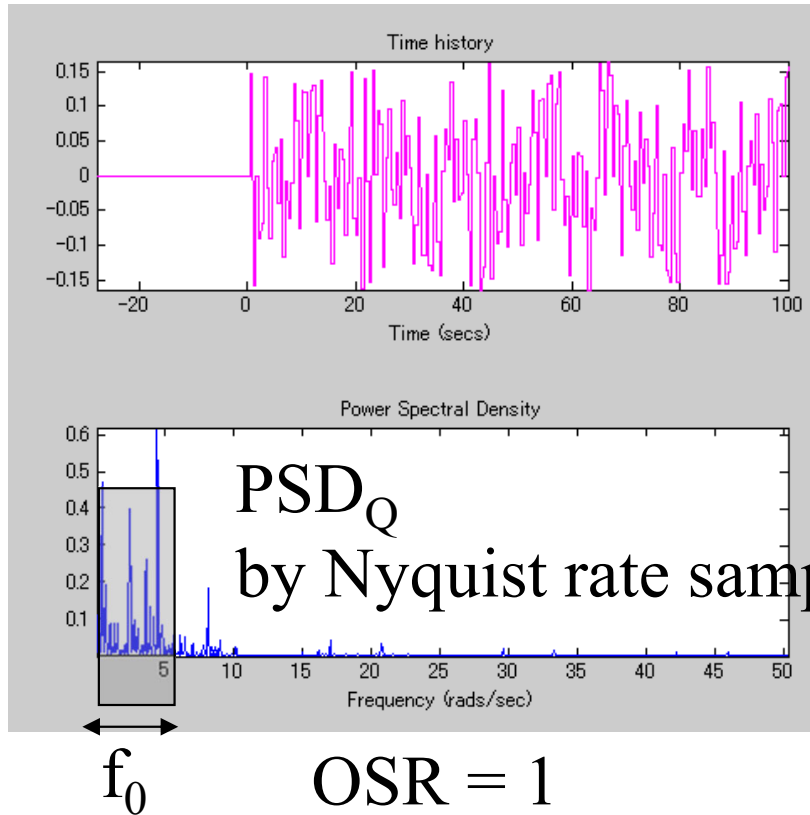
SNR in band width $SNR(\text{dB}) = 10\log \frac{V_{\max_RMS}^2}{P_{Q_RMS}} = 10\log \frac{\left(\frac{2^N-1}{2\sqrt{2}}V_{LSB}\right)^2}{\frac{V_{LSB}^2}{12}} OSR$
 $= 10\log \frac{3}{2} (2^N - 1)^2 + 10\log OSR$
 $\cong 6.02N + 1.76 + 10\log OSR \quad (\text{dB})$

Noise reduction by over sampling

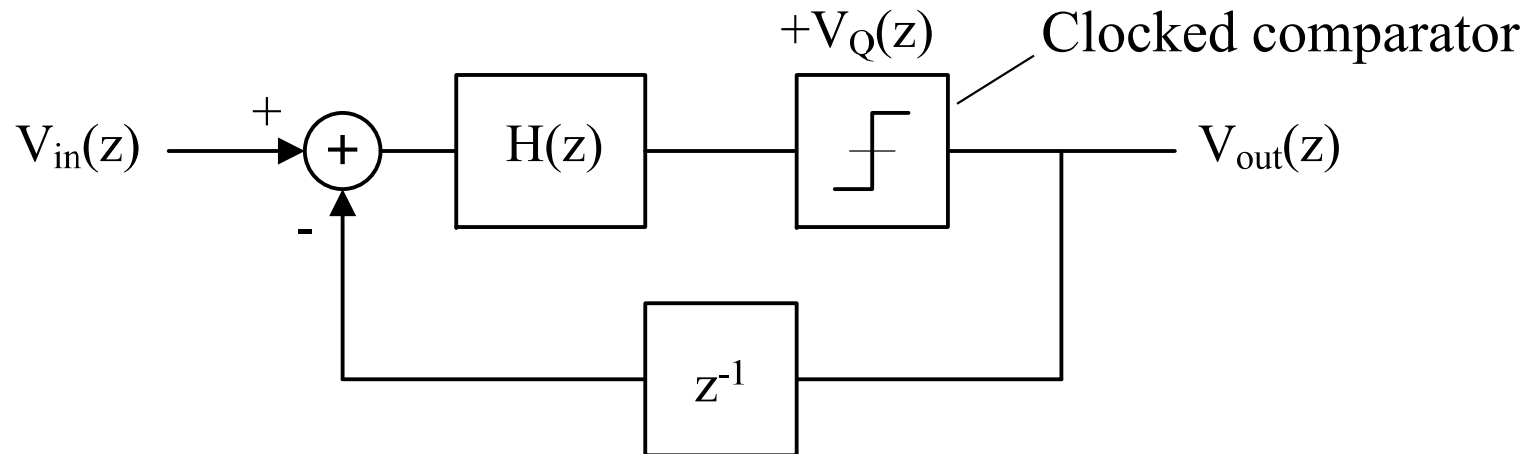
N = 1bit

N = 1bit

Quantization error



Delta-sigma modulator



$$V_{out}(z) = H(z)\{V_{in}(z) - z^{-1}V_{out}(z)\} + V_Q(z)$$

$$V_{out}(z) = \frac{H(z)}{1 + z^{-1}H(z)} V_{in}(z) + \frac{1}{1 + z^{-1}H(z)} V_Q(z)$$

For example, $H(z) = \frac{1}{1 - z^{-1}}$ (BET Integral) Transfer function of noise

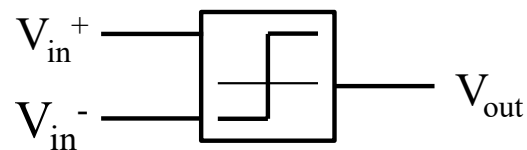
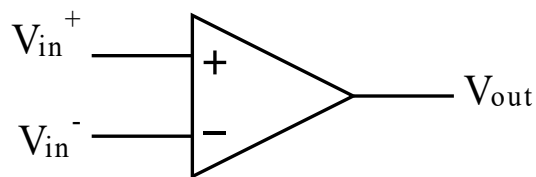
$$V_{out}(z) = V_{in}(z) + (1 - z^{-1})^M V_Q(z) \quad (\text{Order } M = 1)$$

Zero @ $f = 0$

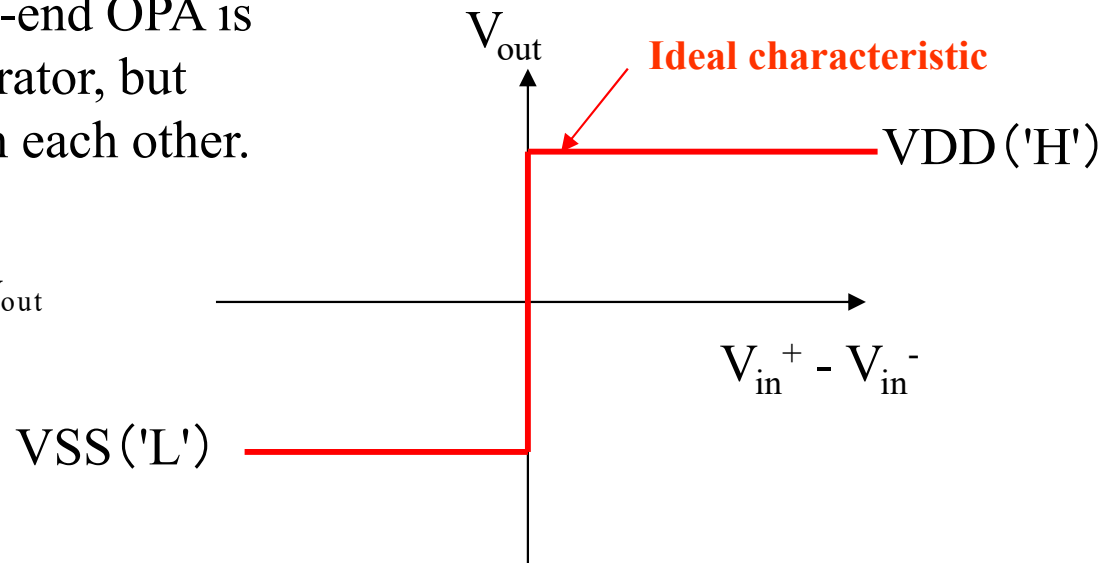
Function of analog comparator

- If ($V_{in}^+ > V_{in}^-$), then $V_{out} = VDD$ (Logic level = 'H')
- If ($V_{in}^+ < V_{in}^-$), then $V_{out} = VSS$ (Logic level = 'L')

The same symbol as a single-end OPA is sometimes used for a comparator, but the circuitry is different from each other.



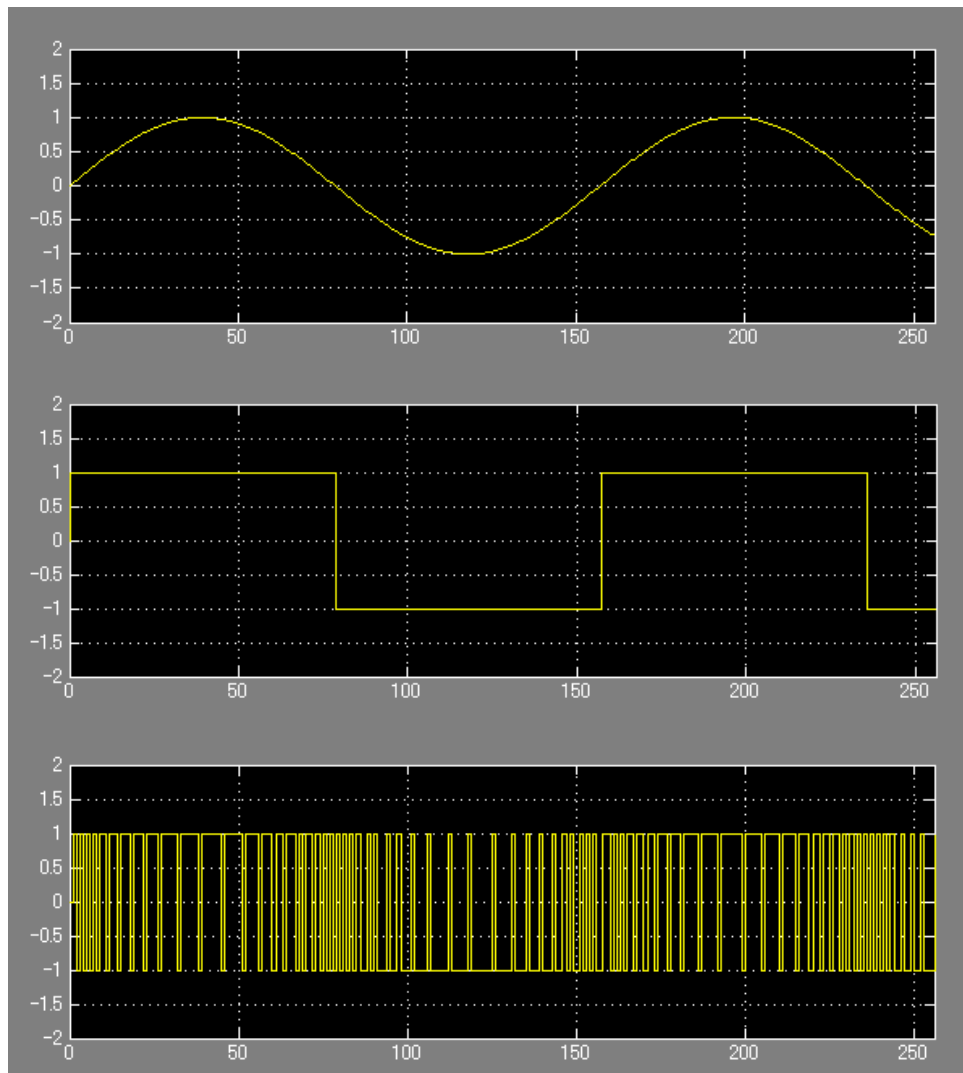
Symbol



Two types of voltage comparator

- Detection of timing when the voltage difference becomes 0V (No clock signal is required.)
- Voltage comparison at a certain time (Clock signal is required.)
 - Here we will use the latter.

Time domain characteristic of delta-sigma modulator



32 bit binary



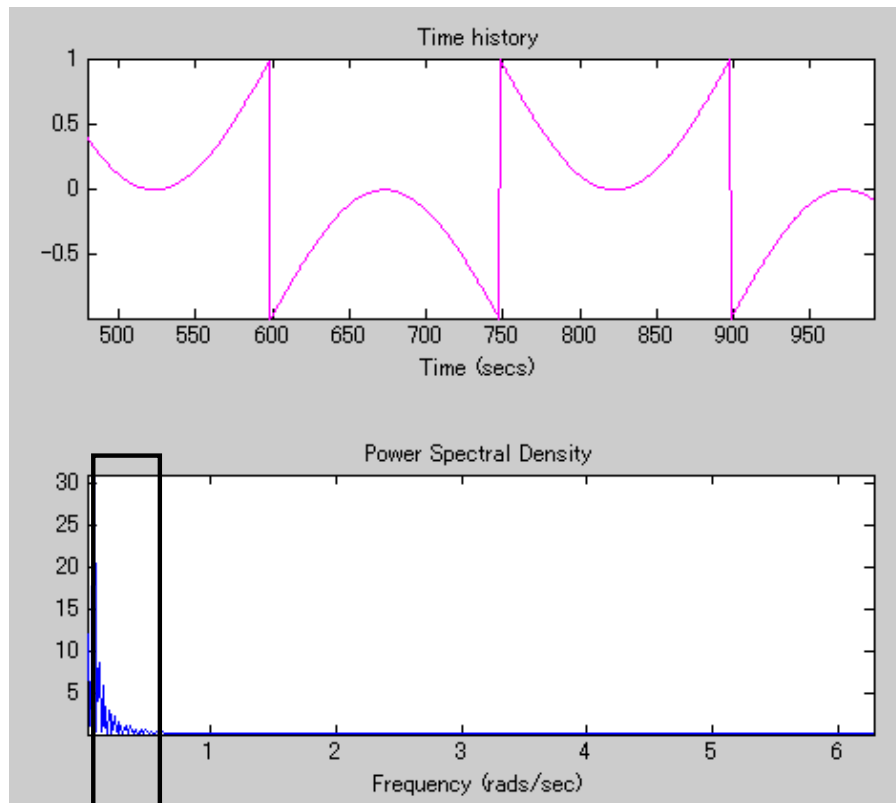
Comparator
(OSR = 24)



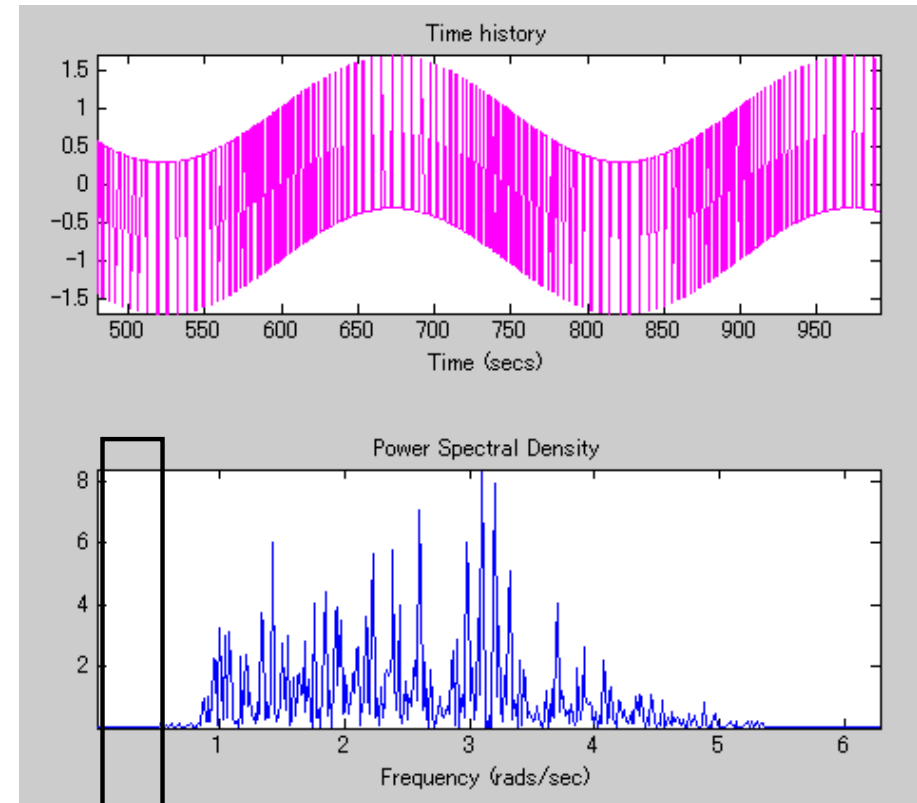
1-bit delta-sigma modulation
= Pulse-density modulation
(OSR = 24)

Noise shaping by delta-sigma modulation

Error of comparator



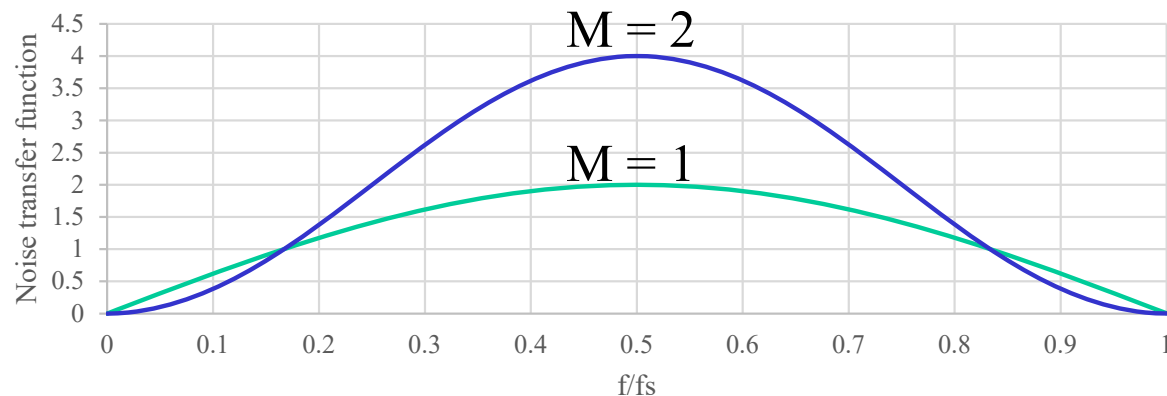
Error of 1-bit delta-sigma modulation



f_0

f_0

Noise reduction by noise shaping



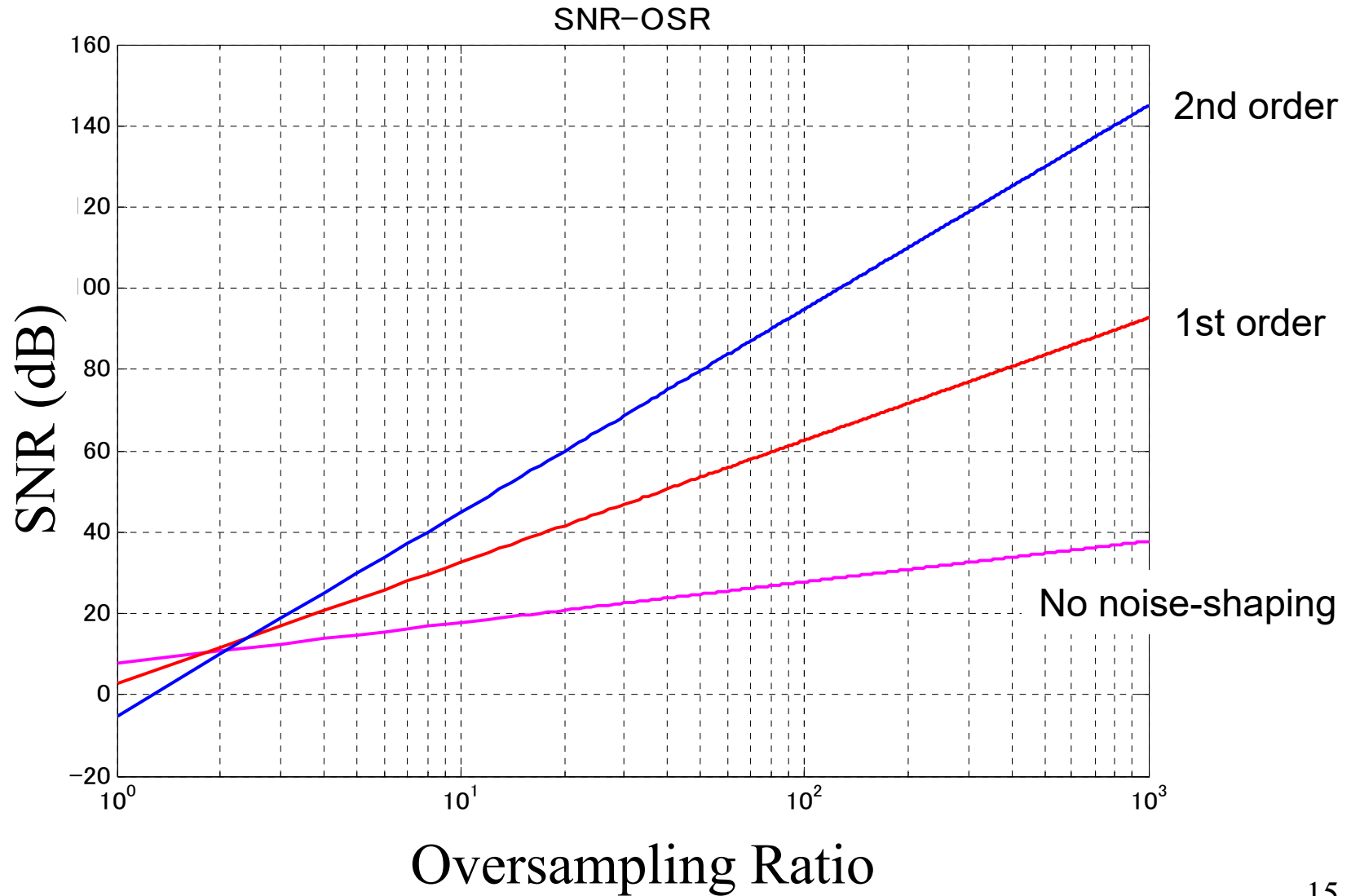
$$M=1 \quad |(1 - z^{-1})| = |1 - e^{-j\omega T_s}| = \left| 2\sin\left(\pi \frac{f}{f_s}\right) \right|$$

$$M=2 \quad |(1 - z^{-1})^2| = |1 - e^{-j\omega T_s}|^2 = \left| 2\sin\left(\pi \frac{f}{f_s}\right) \right|^2$$

$$SNR(dB) = \int_{f_0}^{f_0} \frac{V_{\max_RMS}^2}{P_{Q_RMS} \cdot \left| 2\sin\left(\pi \frac{f}{f_s}\right) \right|^{2M}} df$$

$$\cong 6.02N + 1.76 - 20 \log \left(\frac{\pi^M}{\sqrt{2M+1}} \right) + (20M + 10) \log OSR$$

SNR vs. OSR



Effective number of bits (ENOB)

For 1-bit quantization (=Comparator),

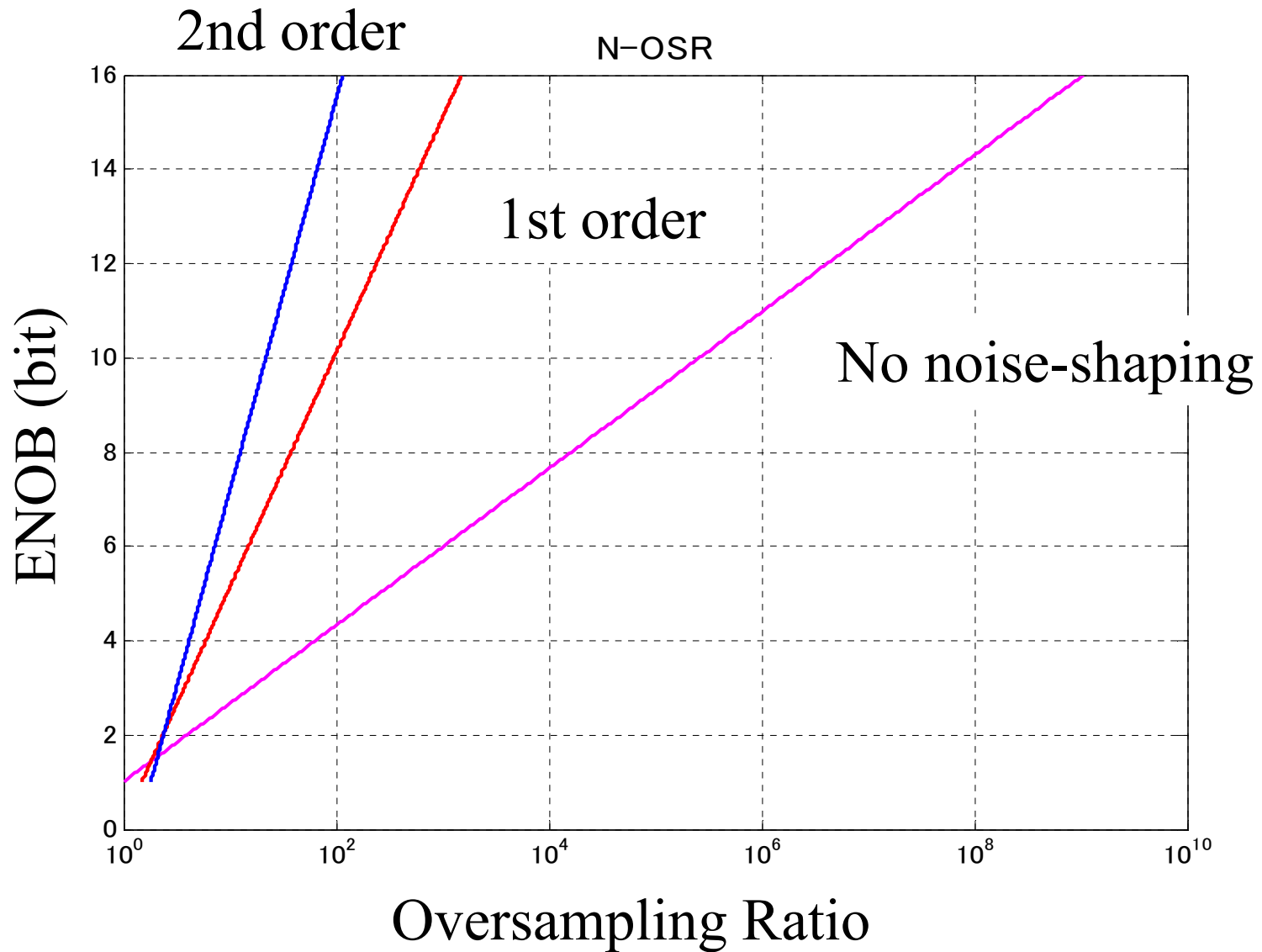
Simple quantization

Noise shaping (N = 1bit)

$$6.02ENOB + 1.76 = 6.02 + 1.76 - 20 \log \left(\frac{\pi^M}{\sqrt{2M + 1}} \right) + (20M + 10) \log OSR$$

$$ENOB = 1 + \frac{1}{6.02} \left\{ (20M + 10) \log OSR - 20 \log \left(\frac{\pi^M}{\sqrt{2M + 1}} \right) \right\}$$

ENOB vs. OSR



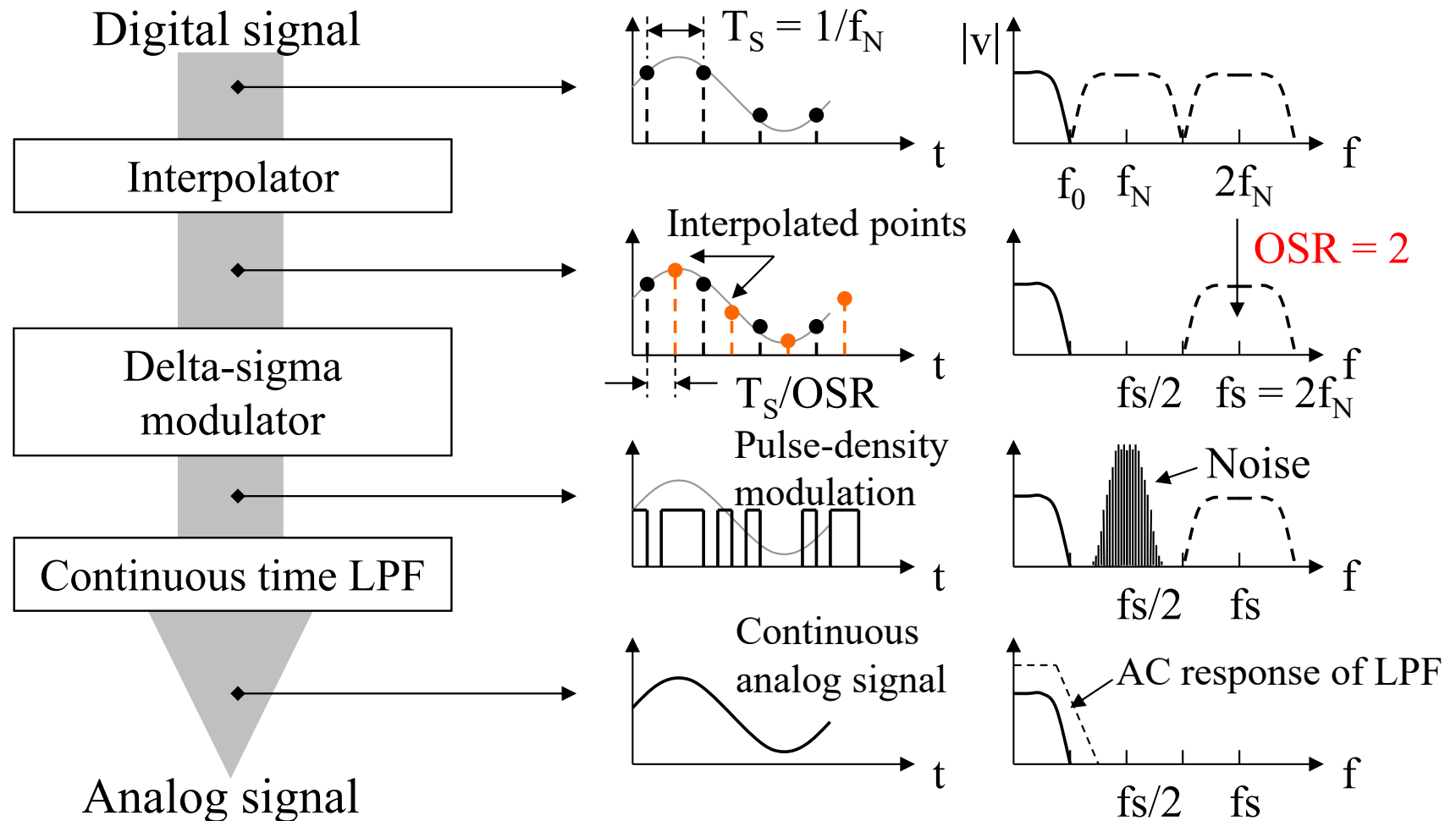
4.2 Oversampling DAC

Principle of oversampling DAC

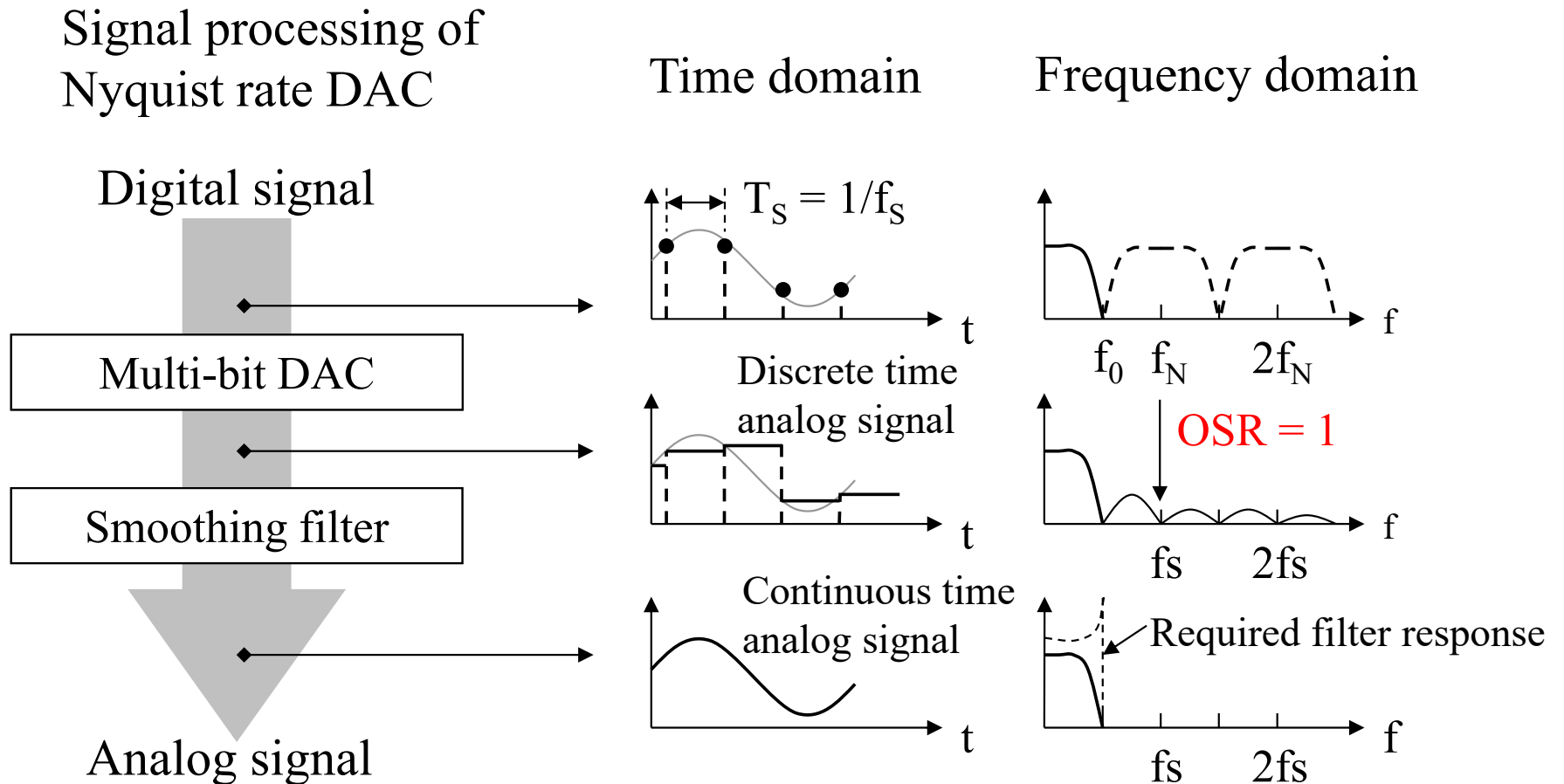
Signal processing

Time domain

Frequency domain



Advantage of oversampling DAC




Nyquist rate DAC requires the ideal LPF for smoothing.

Appendix: Frequency response of sample and hold circuit

Sample and hold of the signal $x(t)$

$$x_{du}(t) = \sum_n x(nT_S) \cdot \underbrace{\{u(t - nT_S) - u(t - (n+1)T_S)\}}_{\text{Step sampler}}$$

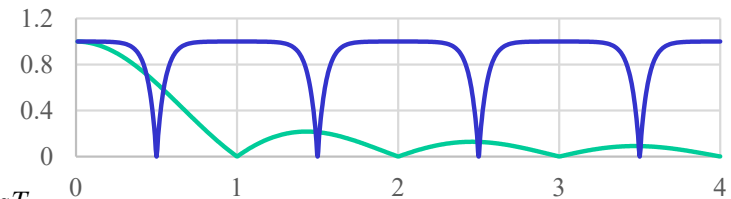
\mathcal{L} 

$$X_{du}(s) = \int_0^\infty \sum_n x(nT_S) \cdot \{u(t - nT_S) - u(t - (n+1)T_S)\} \cdot e^{-st} dt$$

$$= \sum_n x(nT_S) \cdot \int_0^\infty \{u(t - nT_S) - u(t - (n+1)T_S)\} \cdot e^{-st} dt$$

$$= \sum_n x(nT_S) \cdot \frac{e^{-snT_S} (1 - e^{-sT_S})}{s}$$

$$= \frac{1 - e^{-sT_S}}{s} \sum_n x(nT_S) \cdot e^{-snT_S} \xrightarrow{z} \underbrace{\frac{1 - e^{-sT_S}}{s}}_{\text{Transfer function of step sampler}} \underbrace{\sum_n x(nT_S) \cdot z^{-n}}_{\text{Impulse train}}$$

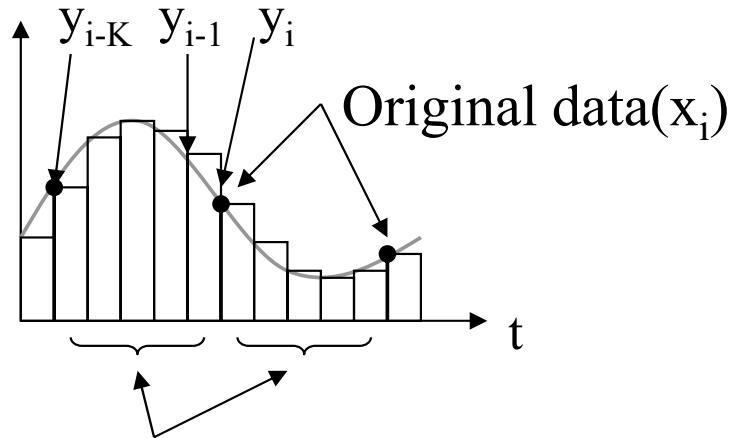


Transfer function of step sampler

Impulse train

Interpolator

Example: Linear interpolation



K-1 interpolated data

Sampling rate conversion
(up conversion)

$$\frac{f_s}{K}$$

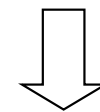
$$e^{-sKT_s} = z^{-K}$$

$$(1 - z^{-1})^{L+1} \xrightarrow{f_s/K} (1 - z^{-K})^{L+1}$$

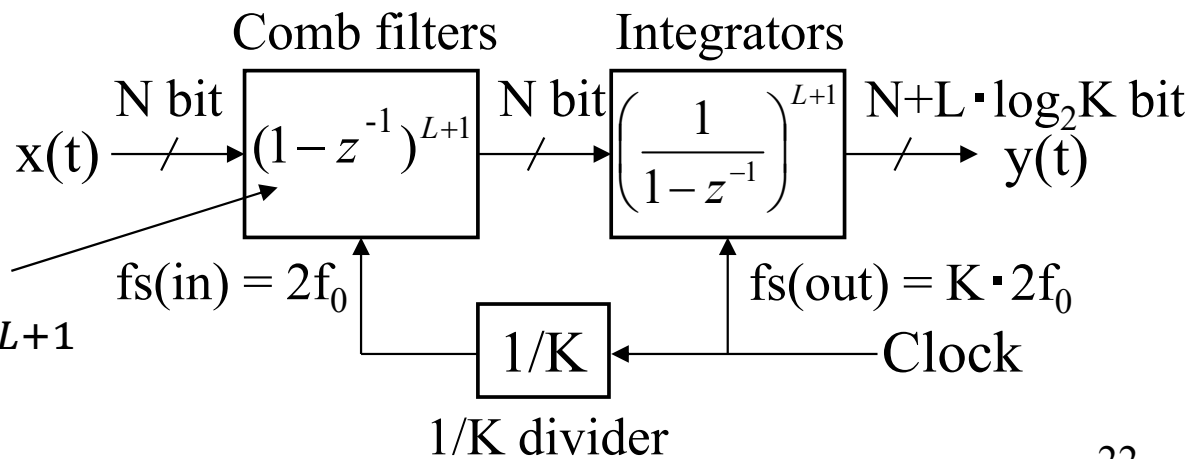
$$\frac{y_i - y_{i-1}}{T_s} = \frac{x_i - x_{i-K}}{K \cdot T_s} \quad \curvearrowright Z$$

$$Y(z)(1 - z^{-1}) = X(z) \frac{1 - z^{-K}}{K}$$

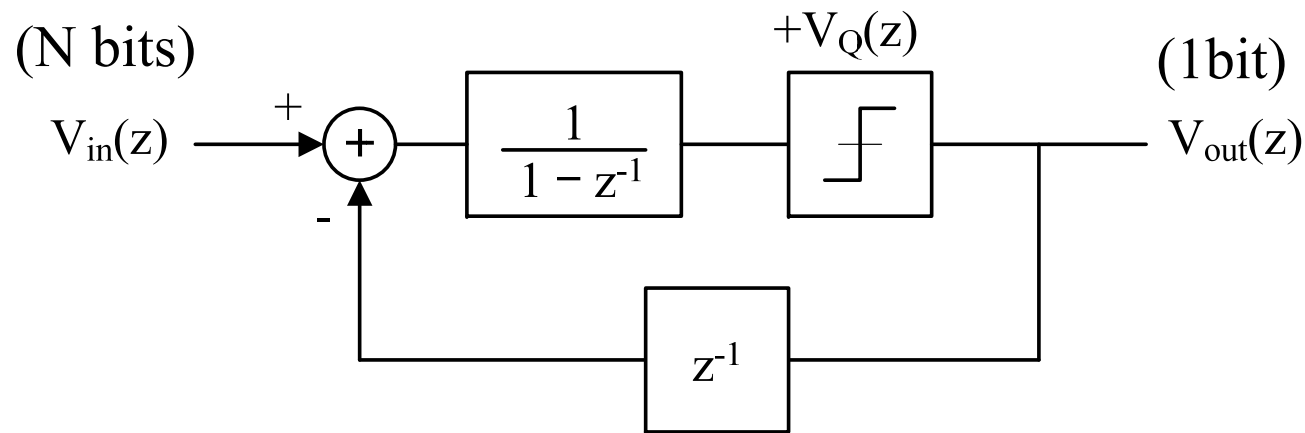
$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{K} \frac{1 - z^{-K}}{1 - z^{-1}}$$



Circuits implementation



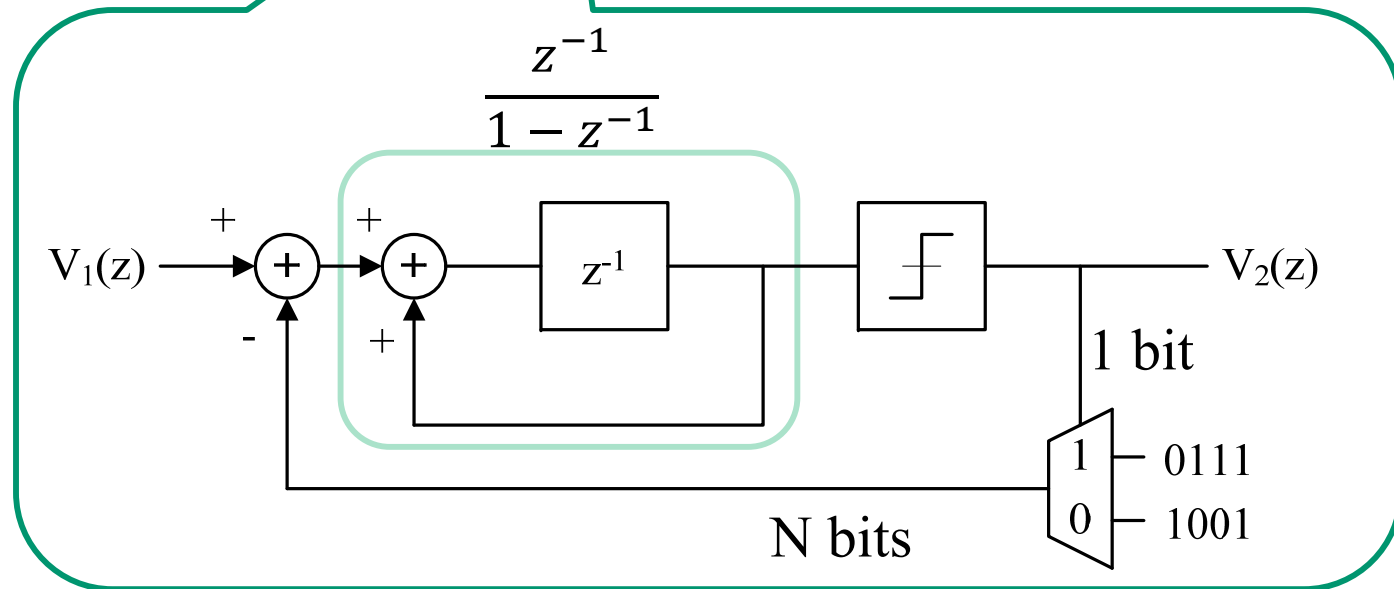
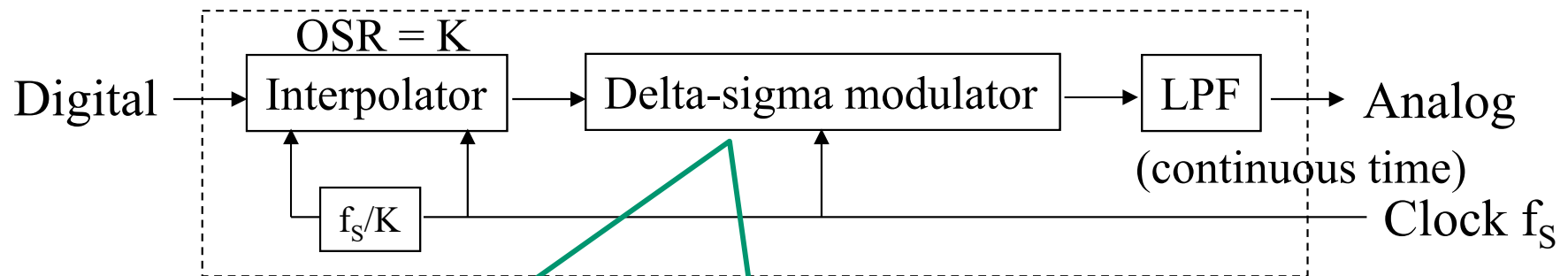
Pulse-density modulation by delta-sigma modulator (DSM)



$$V_{out}(z) = V_{in}(z) + (1 - z^{-1})^M V_Q(z)$$

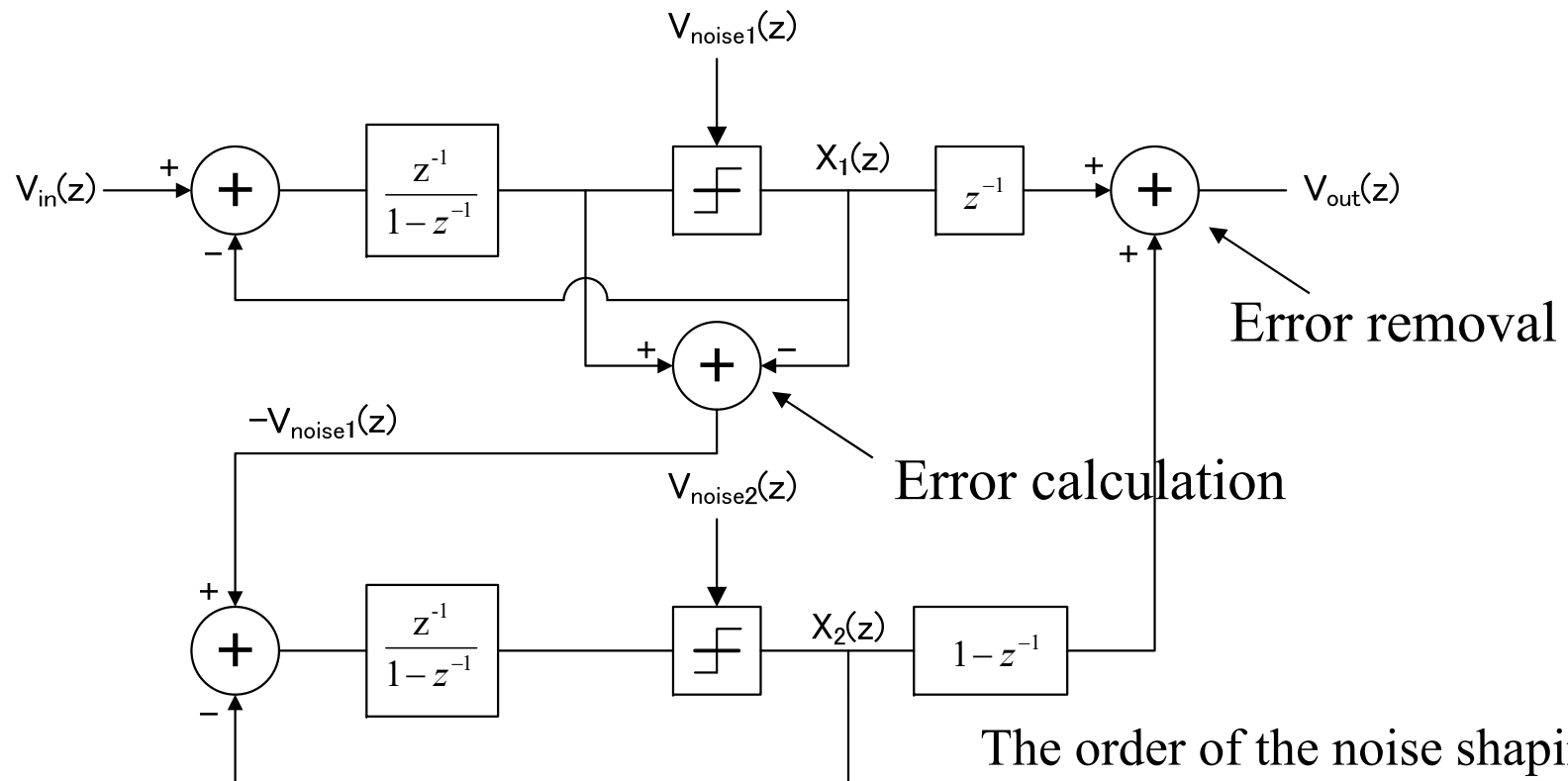
\nearrow 1 bit signal \uparrow N bits signal \uparrow Quantization noise

Architecture of oversampling DAC



Higher order DSM

Multi-stage noise shaping (MASH)



$$X_1(z) = z^{-1}V_{in}(z) + (1-z^{-1})V_{noise1}(z)$$

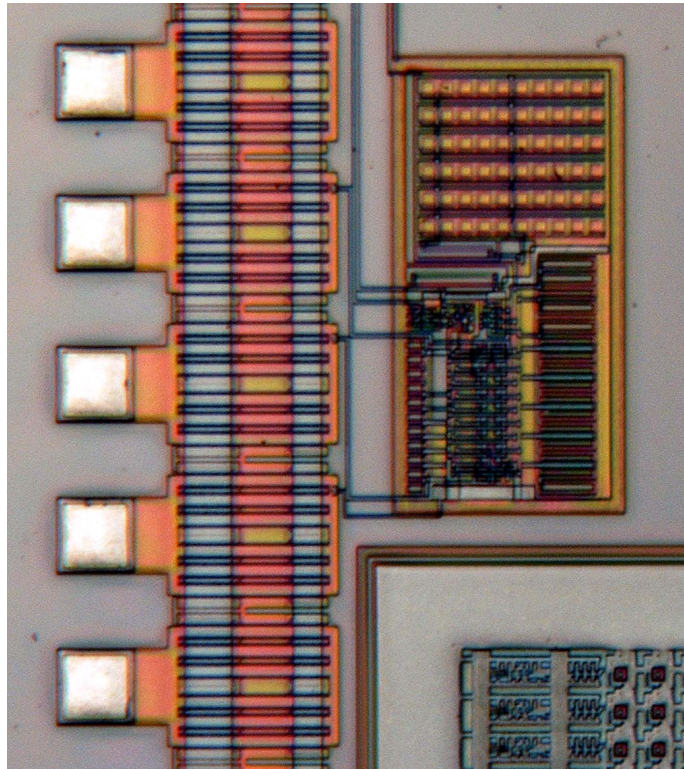
$$X_2(z) = -z^{-1}V_{noise1}(z) + (1-z^{-1})V_{noise2}(z)$$

$$V_{out}(z) = z^{-1}X_1(z) + (1-z^{-1})X_2(z) = z^{-2}V_{in}(z) + (1-z^{-1})^2V_{noise2}(z)$$

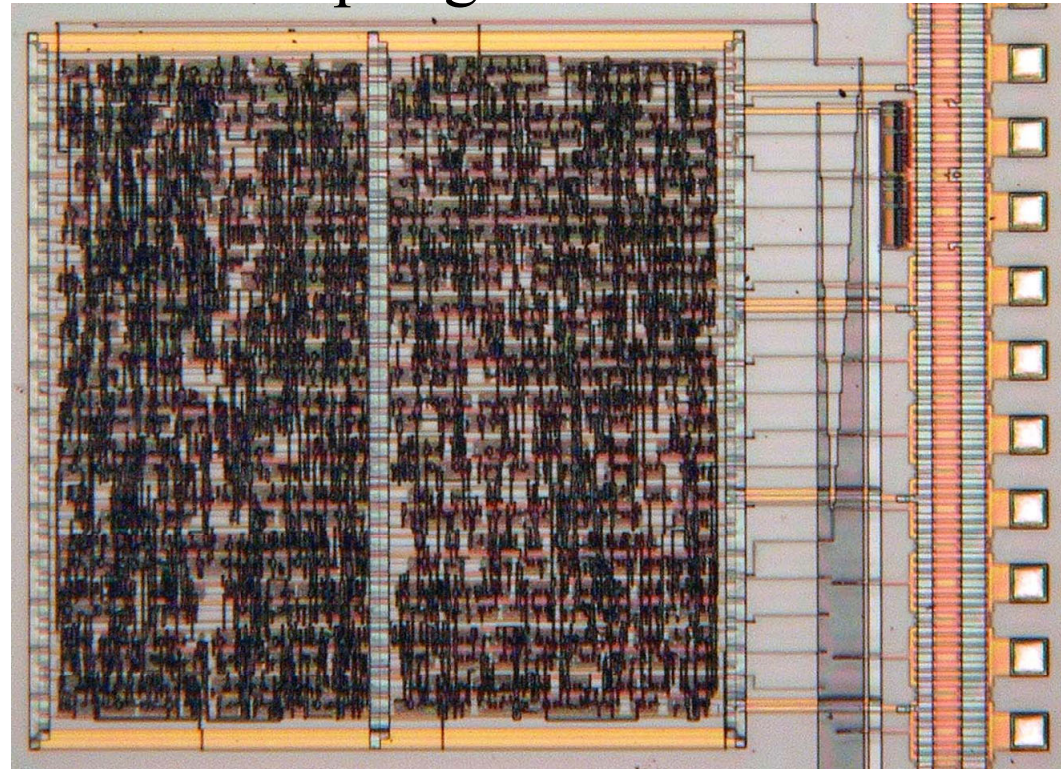
The order of the noise shaping is increased by repeating the error calculation.

Example of oversampling DAC

Continuous time LPF



Oversampling DAC



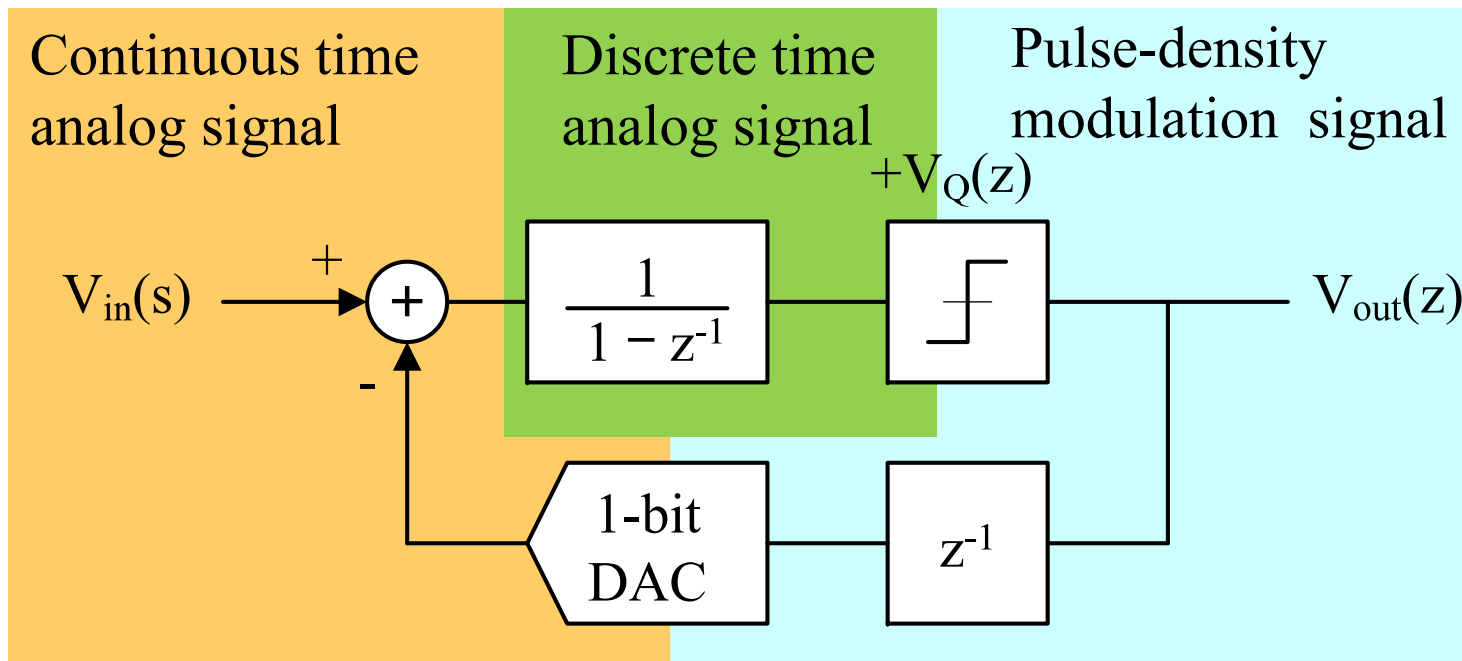
IO buffers

(c) Kanazawa University

SOI-CMOS 0.6um, 16bit, 2nd order DSM, OSR=128

4.3 Delta-Sigma ADC

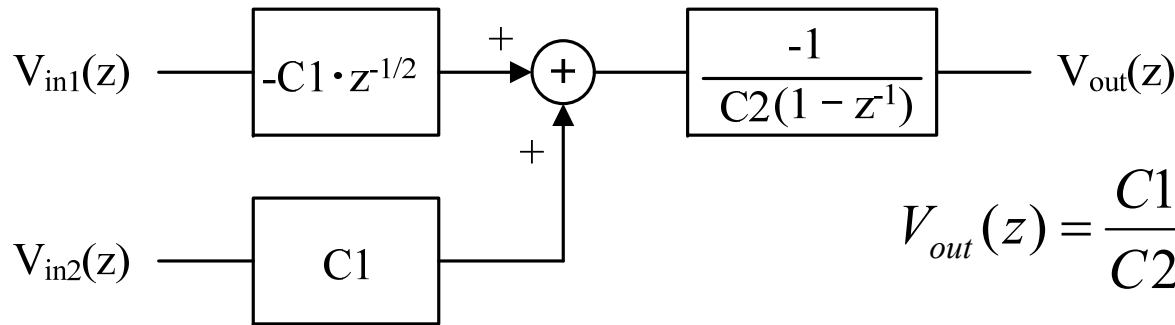
Principle of analog DSM



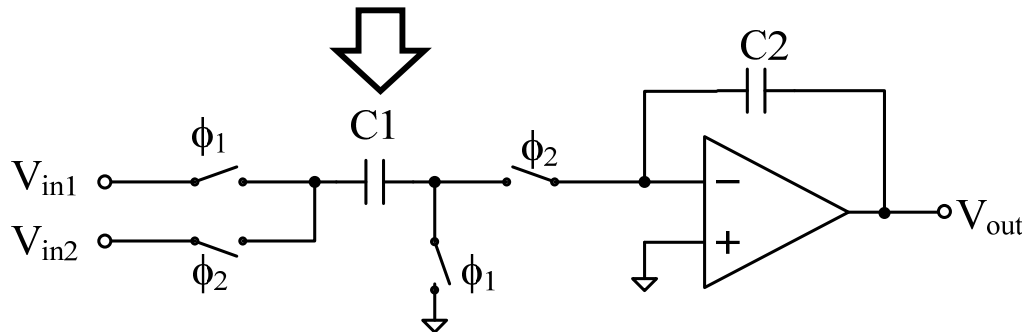
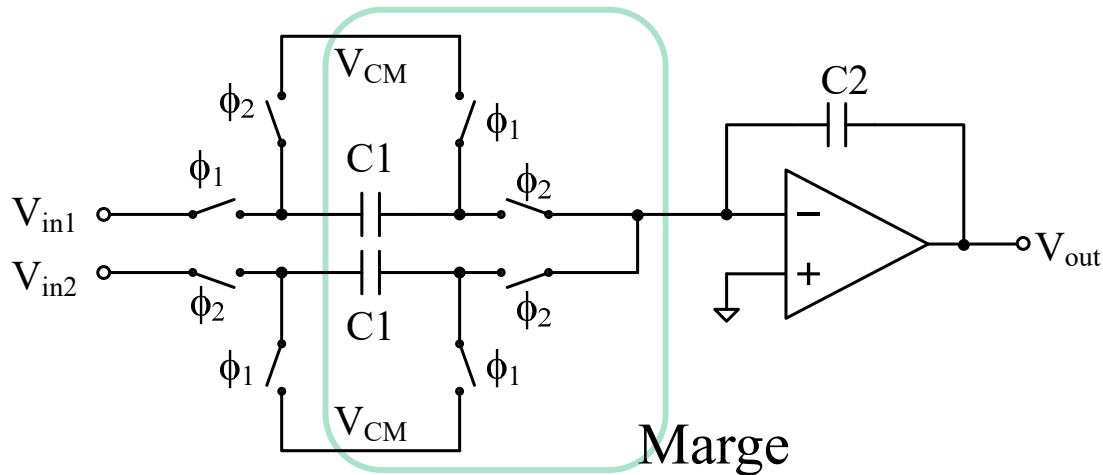
$$V_{out}(z) = V_{in}(z) + (1 - z^{-1})^M V_Q(z)$$

Pulse-density modulated signal Continuous time analog signal Quantization noise

DAI with reference input

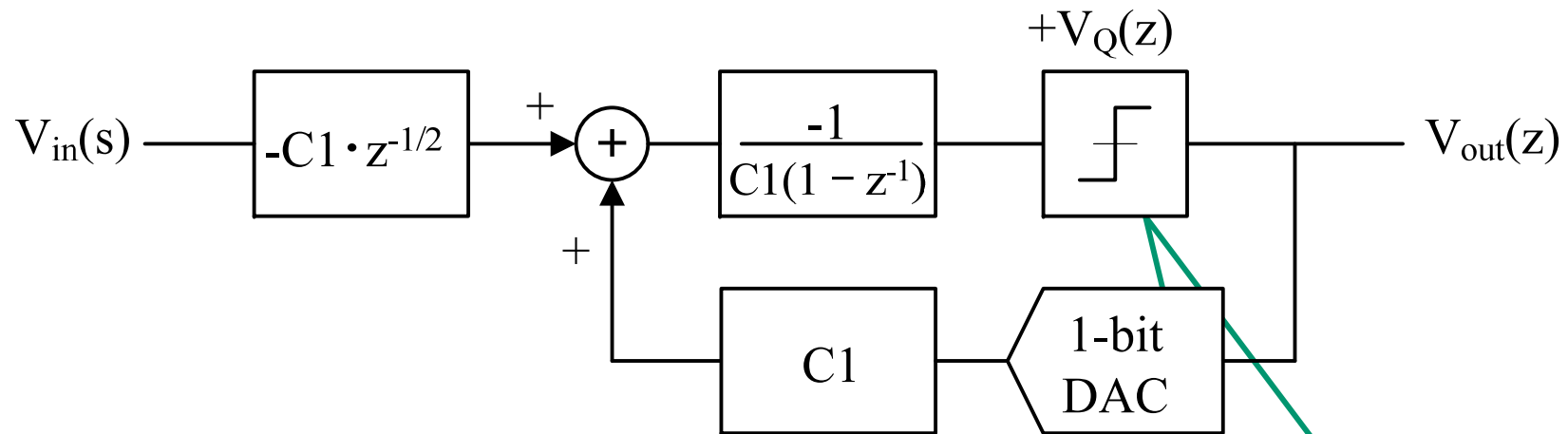


$$V_{out}(z) = \frac{C1}{C2} \frac{1}{1 - z^{-1}} \{z^{-\frac{1}{2}} V_{in1}(z) - V_{in2}(z)\}$$



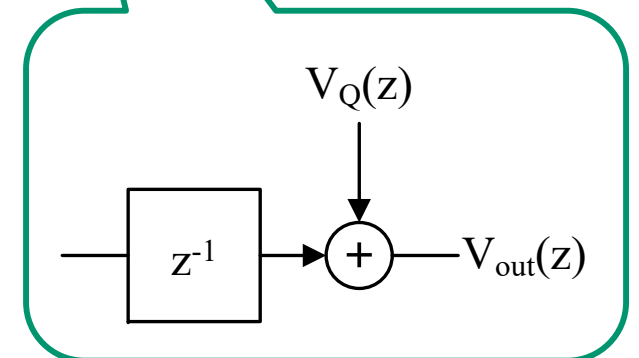
2-input DAI

Architecture of delta-sigma ADC



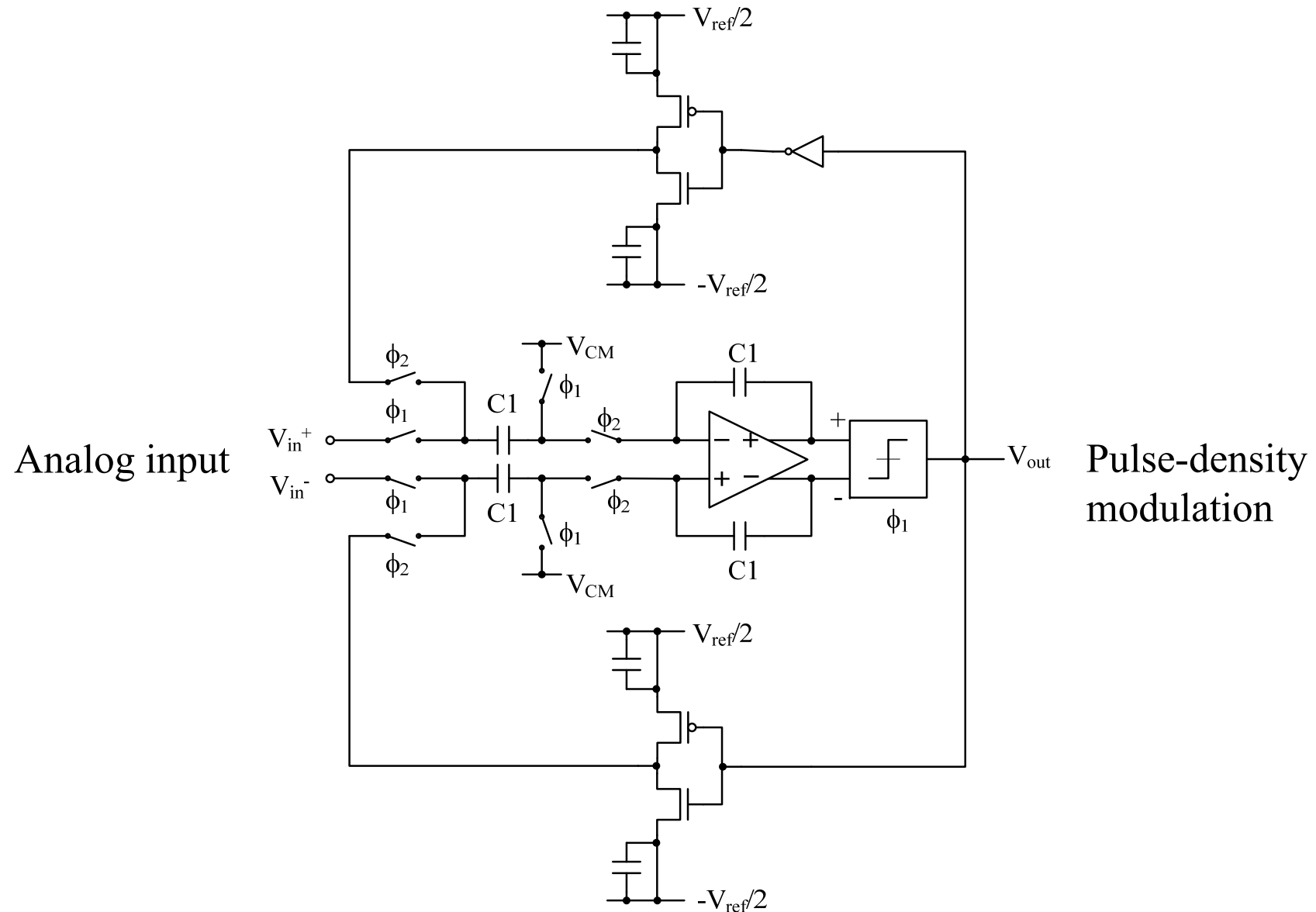
$$V_{out}(z) = \frac{z^{-1}}{1 - z^{-1}} \left(z^{-\frac{1}{2}} V_{in}(z) - V_{out}(z) \right) + V_Q(z)$$

$$V_{out}(z) = z^{-\frac{3}{2}} \cdot V_{in}(z) + (1 - z^{-1}) \cdot V_Q(z)$$

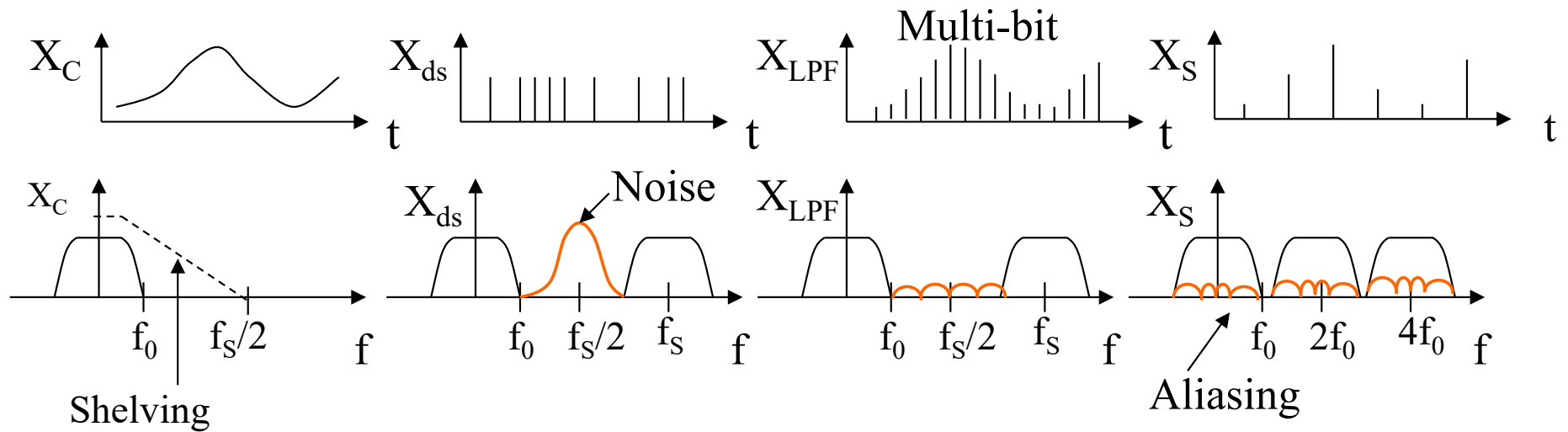
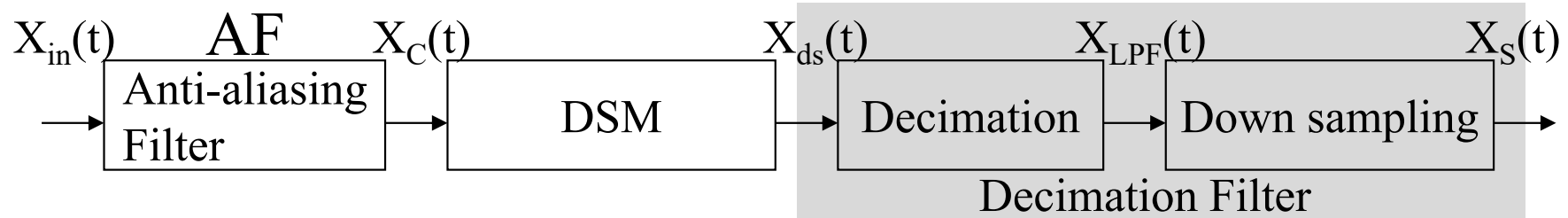


Transfer function of comparator

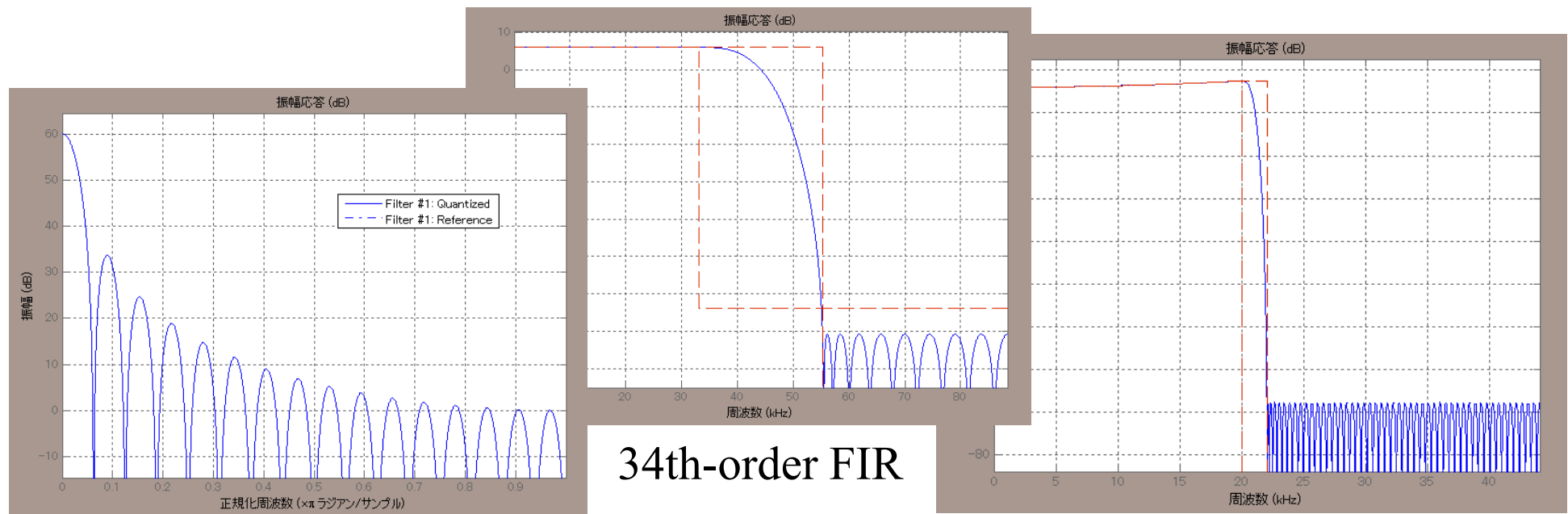
Full differential implementation



Conversion to binary signal



Structure of decimation filter



SinC IIR

34th-order FIR

186th-order FIR

Design of SinC^{L+1} filter

Averaging of M data $T_A = \frac{1}{M} \sum_{i=0}^{M-1} z^{-i} \equiv \frac{X_{out}(z)}{X_{in}(z)}$

$$\begin{aligned} MX_{out}(z) &= \left\{ \sum_{i=0}^{M-1} z^{-i} \right\} X_{in}(z) = (z^{-1} + z^{-2} + \dots + z^{-M}) X_{in}(z) + (1 - z^{-M}) X_{in}(z) \\ &= Mz^{-1} X_{out}(z) + (1 - z^{-M}) X_{in}(z) \end{aligned}$$

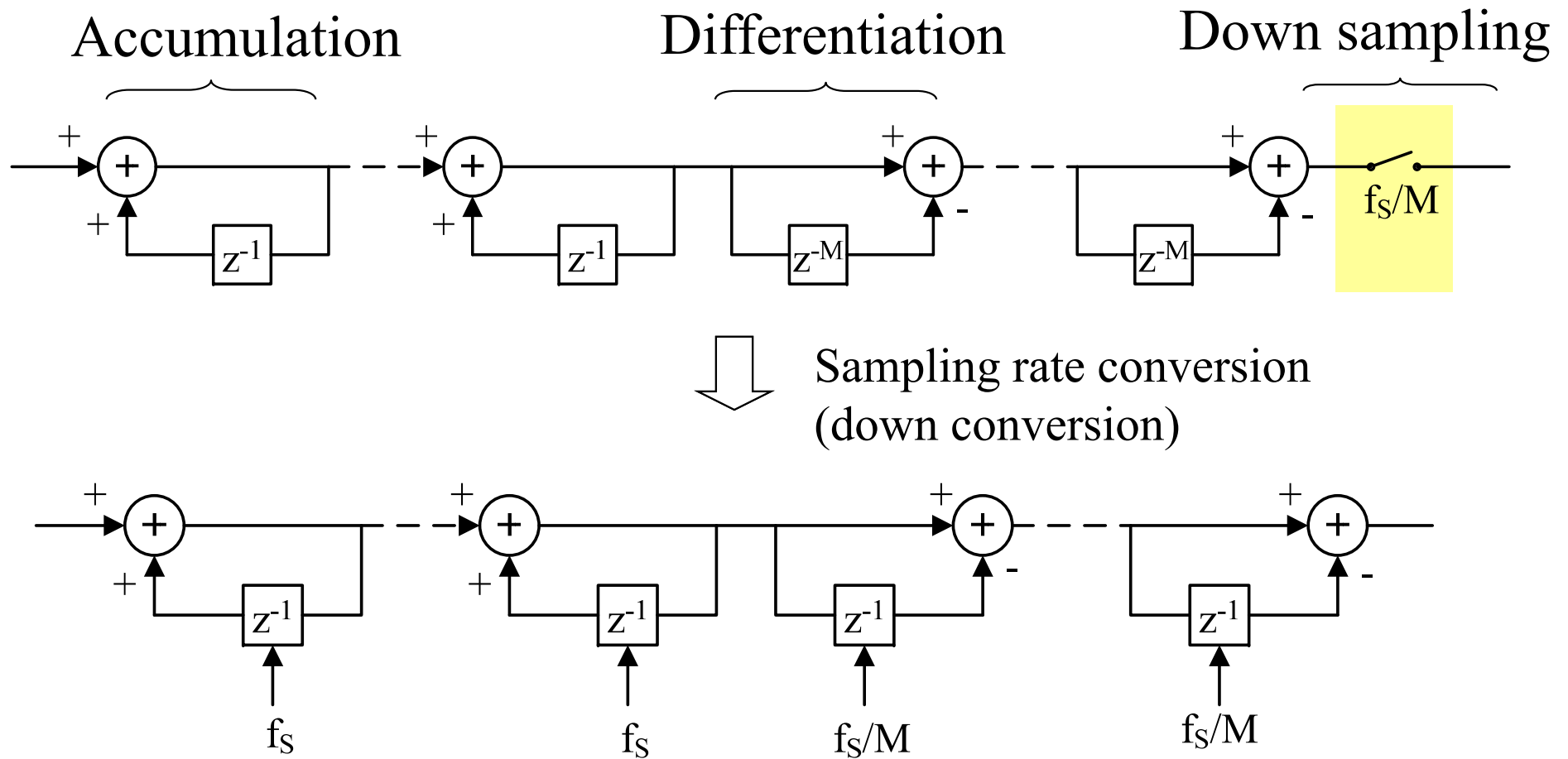
$$T_A = \frac{1}{M} \frac{1 - z^{-M}}{1 - z^{-1}}$$

SinC^{L+1} Filter $H_{SinC} = \frac{1}{M^{L+1}} \left[\frac{1 - z^{-M}}{1 - z^{-1}} \right]^{L+1}$

$$= \frac{1}{(1 - z^{-1})^{L+1}} (1 - z^{-M})^{L+1} \frac{1}{M^{L+1}}$$

Accumulation Differentiation Constant

Implementation of SinC^{L+1} Filter



SinC filter = CIC (Cascaded Integration-Comb) filter

Order of SinC^{L+1} Filter

Without noise shaping

$$SNR = 6.02 \cdot ENOB + 1.76$$

With 1st-order noise shaping

$$SNR = 6.02 + 1.76 - 5.17 + 30\log OSR$$

With 2nd-order noise shaping

$$SNR = 6.02 + 1.76 - 12.9 + 50\log OSR$$



With 1st-order noise shaping

$$ENOB = 1 + (-5.17 + 30\log OSR)/6.02$$

With 2nd-order noise shaping

$$ENOB = 1 + (-12.9 + 50\log OSR)/6.02$$

Number of bits of decimation filter

$$N_{out} = N_{stage} \log_2(OSR)$$

N_{out} must be larger than ENOB.

With 1st-order noise shaping

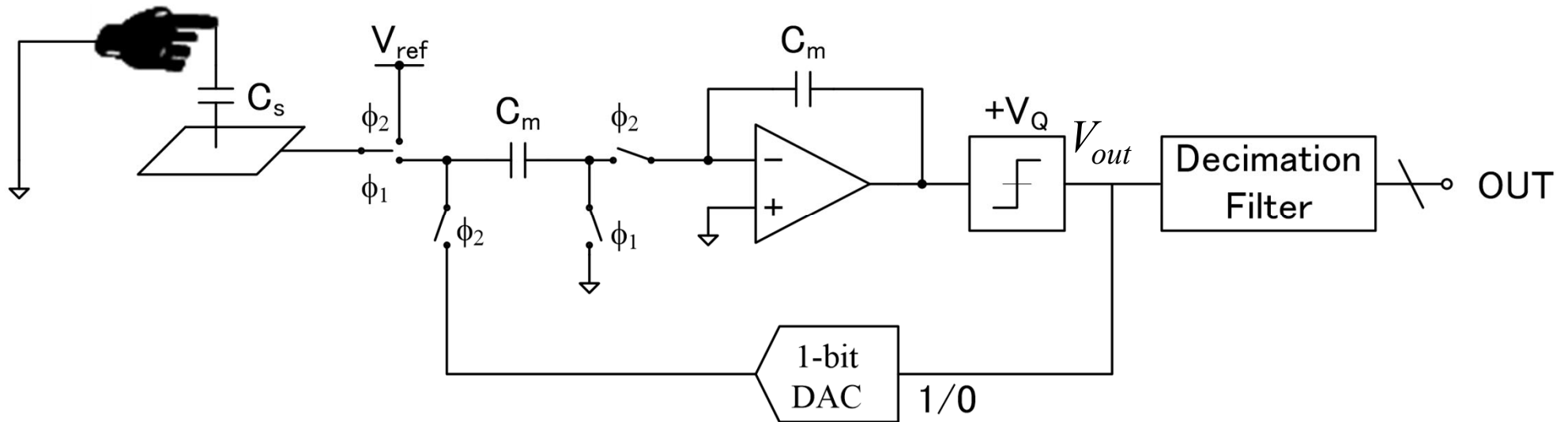
$$N_{stage} > \frac{ENOB}{\log_2(OSR)} \approx 1.5 > L$$

With 2nd-order noise shaping

$$N_{stage} > \frac{ENOB}{\log_2(OSR)} \approx 2.5 > L$$

where L is a order of the noise shaping.

Application example of cap sense (touch panel)



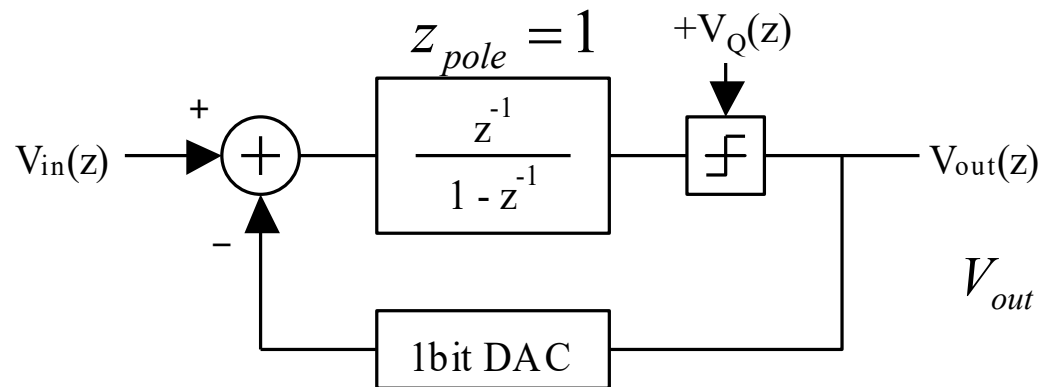
$$V_{out}(z) = z^{-\frac{3}{2}} \frac{C_s}{C_s + C_m} V_{ref} + (1 - z^{-1}) V_Q(z)$$

$$\text{When } f = 0\text{Hz and } z = 1 \text{ (DC), } C_s = \frac{V_{out}(z)}{V_{ref} + V_{out}(z)} C_m$$

4.4 Band-pass Delta-Sigma ADC

Transfer function of band-pass DSM

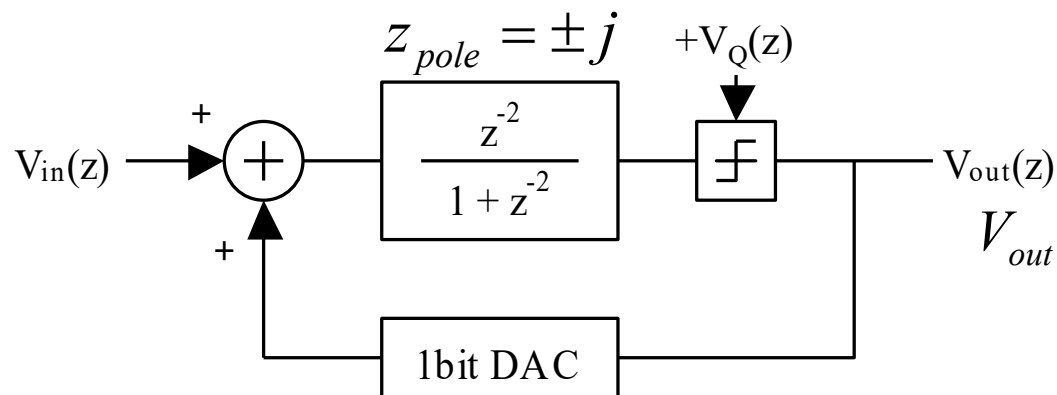
Low-pass DSM



$$V_{out}(z) = z^{-1}V_{in}(z) + \underbrace{(1 - z^{-1})}_{z_{zero} = 1}V_{noise}(z)$$

$$z_{zero} = 1$$

Band-pass DSM



$$V_{out}(z) = z^{-2}V_{in}(z) + \underbrace{(1 + z^{-2})}_{z_{zero} = \pm j}V_{noise}(z)$$

$$z_{zero} = \pm j$$

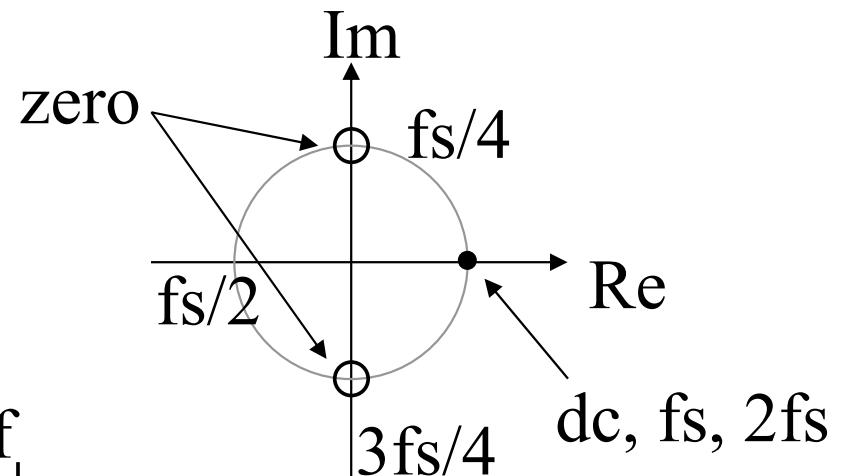
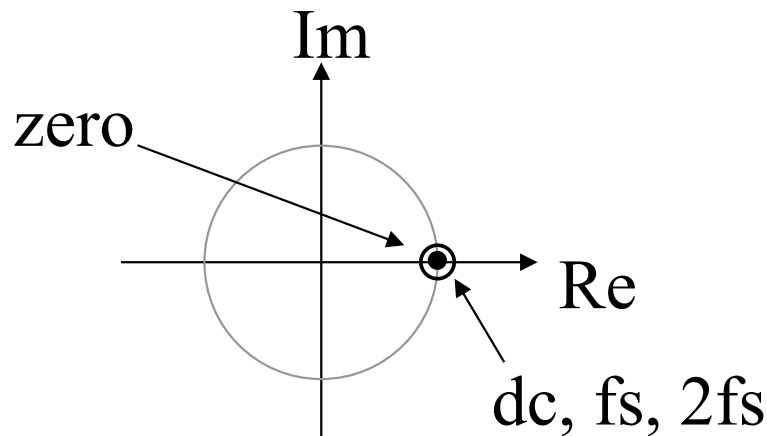
Noise shaping of band-pass DSM

Low-pass

$$V_{out}(z) = z^{-1}V_{in}(z) + (1 - z^{-1})V_{noise}(z)$$

Band-pass

$$V_{out}(z) = z^{-2}V_{in}(z) + (1 + z^{-2})V_{noise}(z)$$

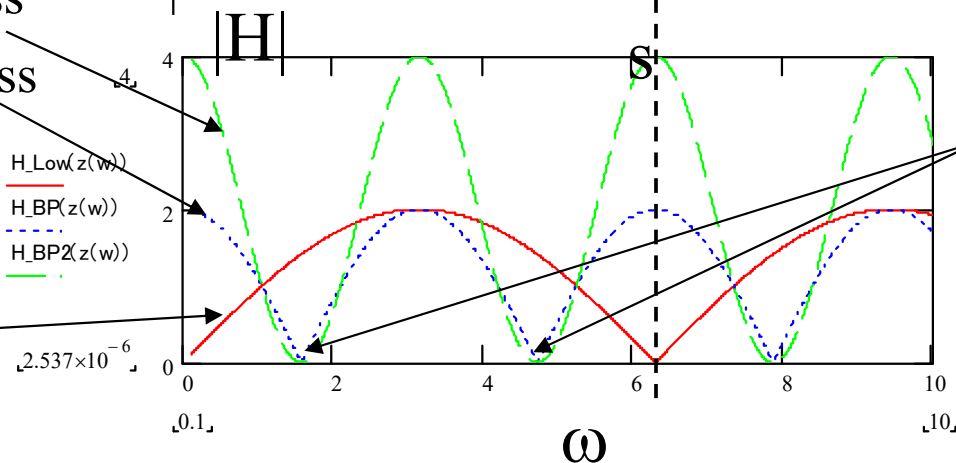


4th order bandpass

2nd order bandpass

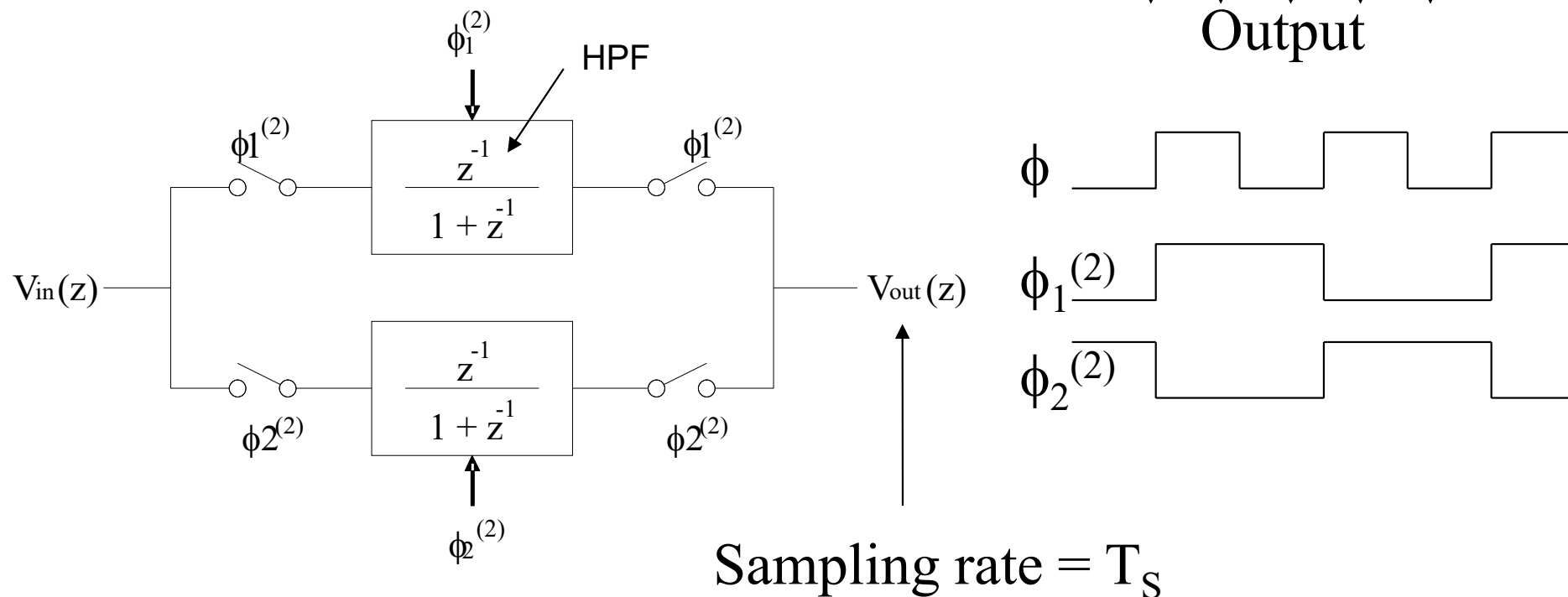
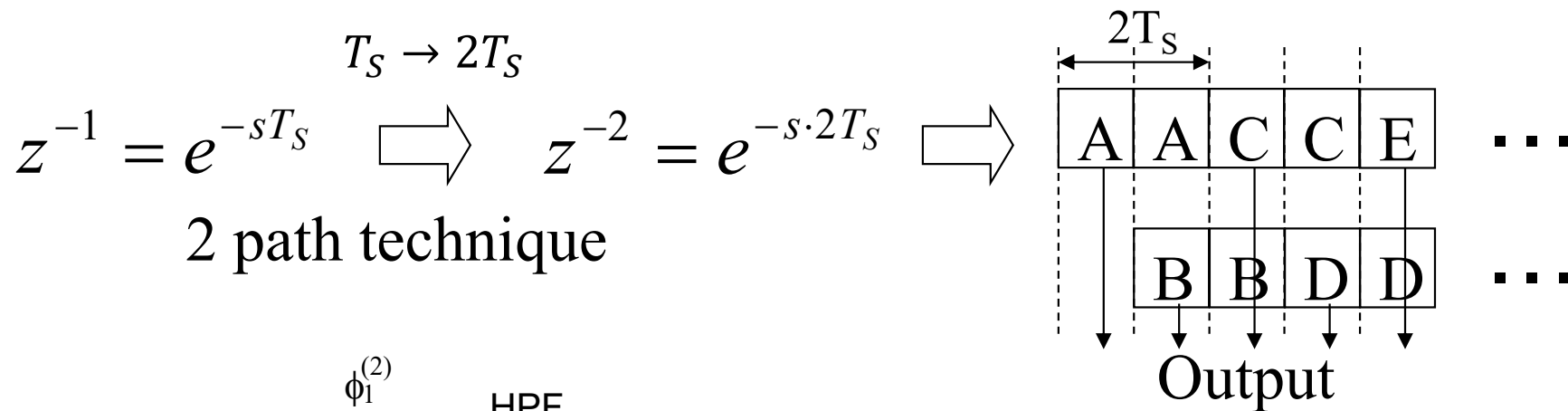
$H_{Low}(z(w))$
 $H_{BP}(z(w))$
 $H_{BP2}(z(w))$
 $H_{BP4}(z(w))$

1st order lowpass



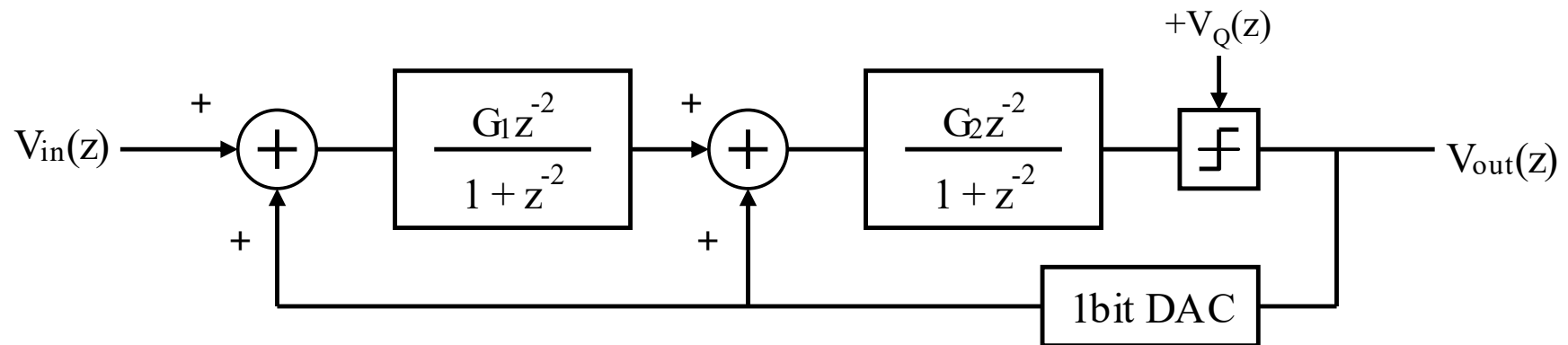
Noise reduction

z^{-2} operation with N-Path technique



4th order band-pass DSM

High-order band-pass ADC is often used for the wireless communication systems.



$$\begin{cases} G_1 = -0.5 \\ G_2 = 2 \end{cases} \Rightarrow V_{out}(z) = -z^{-4}V_{in}(z) + \underbrace{(1+z^{-2})^2}_{z = \pm j} V_{noise}(z)$$

Exercise

Question:

Derive the transfer function of the block diagram shown in the previous slide.

Example solution:

$$V_{out}(z) = \frac{G_2 z^{-2}}{1 + z^{-2}} \left\{ \frac{G_1 z^{-2}}{1 + z^{-2}} (V_{in}(z) + V_{out}(z)) + V_{out}(z) \right\} + V_{noise}(z)$$

$$\left(1 - \frac{G_1 G_2 z^{-4}}{(1 + z^{-2})^2} - \frac{G_2 z^{-2}}{1 + z^{-2}} \right) \cdot V_{out}(z) = \frac{G_1 G_2 z^{-4}}{(1 + z^{-2})^2} V_{in}(z) + V_{noise}(z)$$

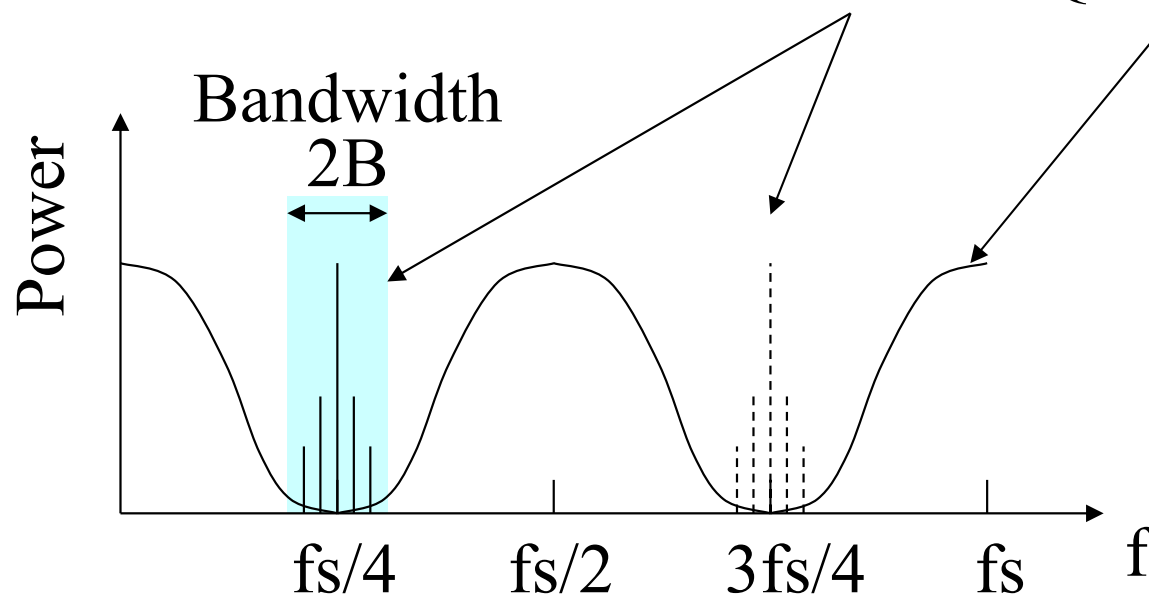
$$\frac{(1 + z^{-2})^2 - G_1 G_2 z^{-4} - G_2 z^{-2} (1 + z^{-2})}{(1 + z^{-2})^2} V_{out}(z) = \frac{G_1 G_2 z^{-4}}{(1 + z^{-2})^2} V_{in}(z) + V_{noise}(z)$$

$$V_{out}(z) = \frac{G_1 G_2 z^{-4} \cdot V_{in}(z) + (1 + z^{-2})^2 \cdot V_{noise}(z)}{1 + 2z^{-2} + z^{-4} - G_1 G_2 z^{-4} - G_2 z^{-2} - G_2 z^{-4}}$$

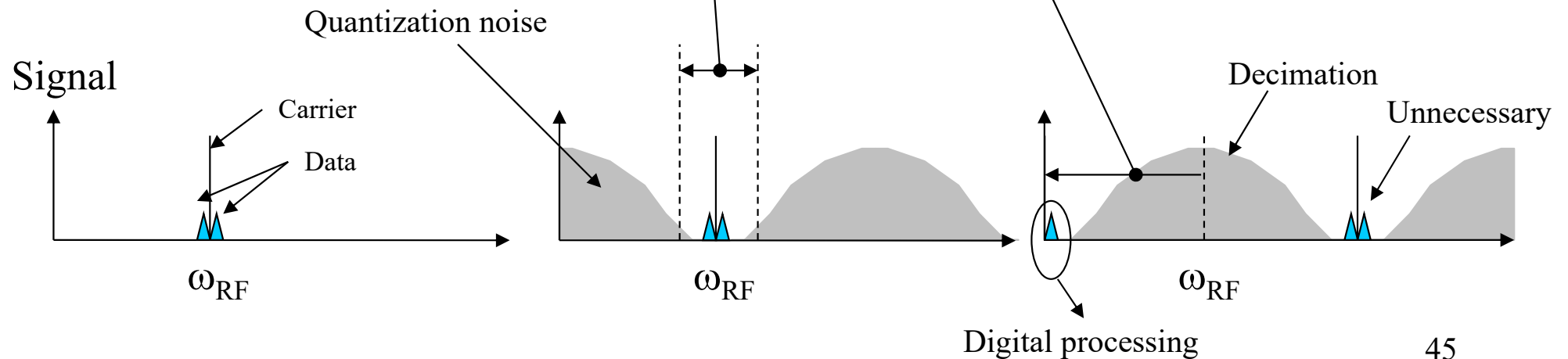
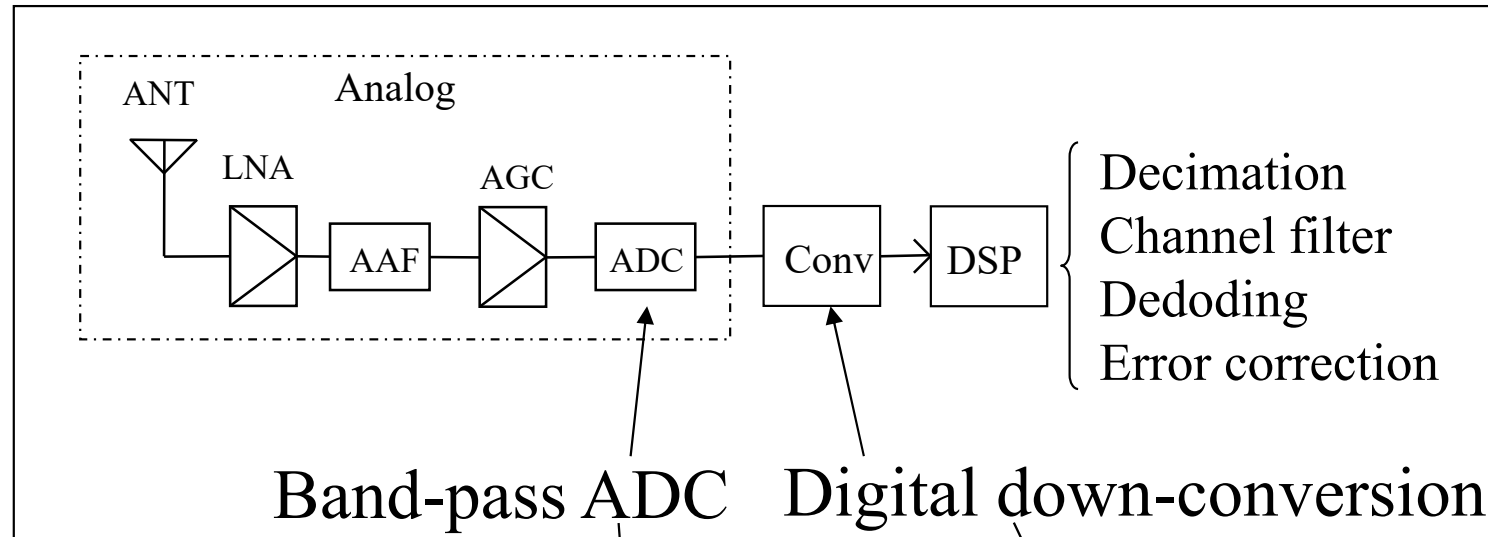
Oversampling ratio of band-pass ADC

The OSR of the band-pass DSM cannot be determined by the carrier frequency, but should be calculated by the bandwidth of the converted signal.

$$OSR = \frac{f_s}{2 \cdot (2B)} \quad V_{out}(z) = \underbrace{z^{-4}V_{in}(z)}_{\text{Signal}} + \underbrace{(1+z^{-2})^2 V_Q(z)}_{\text{Quantization noise}}$$

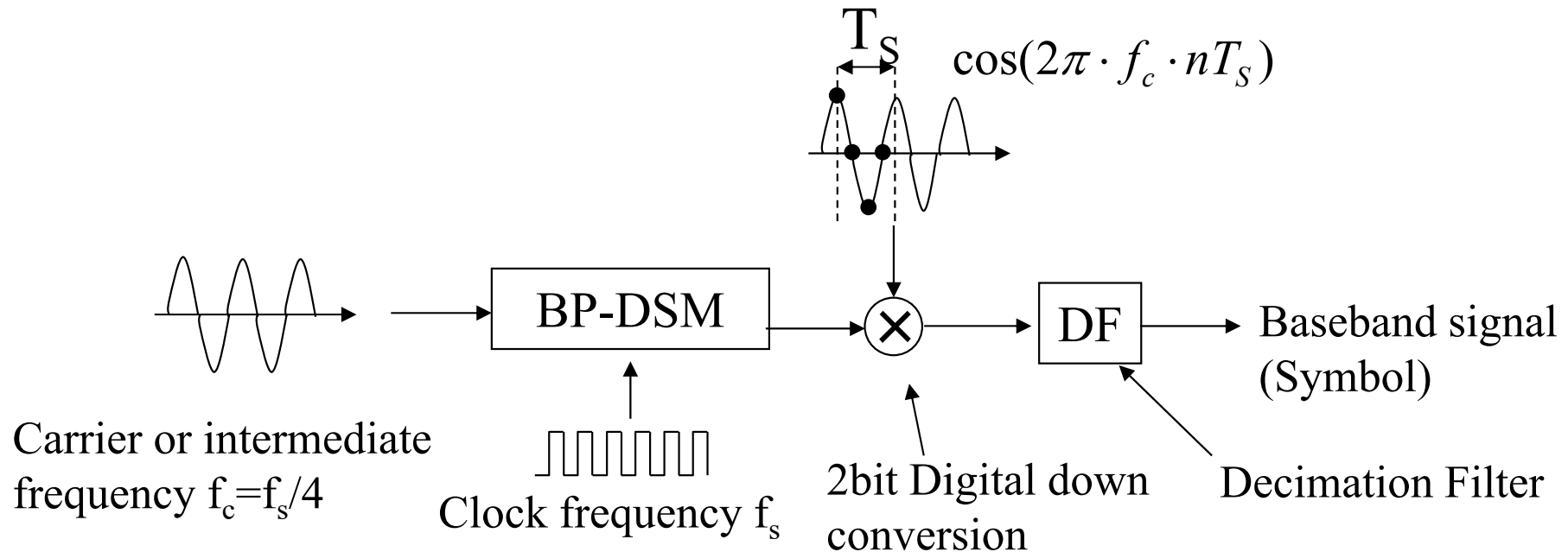


Receiver architecture



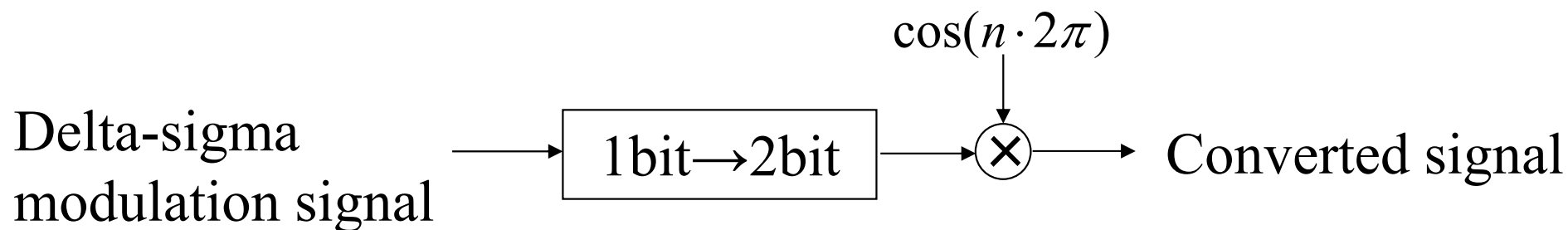
Digital down-conversion

When $f_s = 4f_c$, the digital down conversion can be implemented by 2-bit logic.



$$\cos(2\pi \cdot f_c \cdot nT_s) = \cos\left(2\pi \frac{f_s}{4} n \frac{1}{f_s}\right) = \cos\left(n \frac{\pi}{2}\right) = \{1, 0, -1, 0\} \quad \text{2-bit-at-a-time}$$

Example of 2-bit multiplier



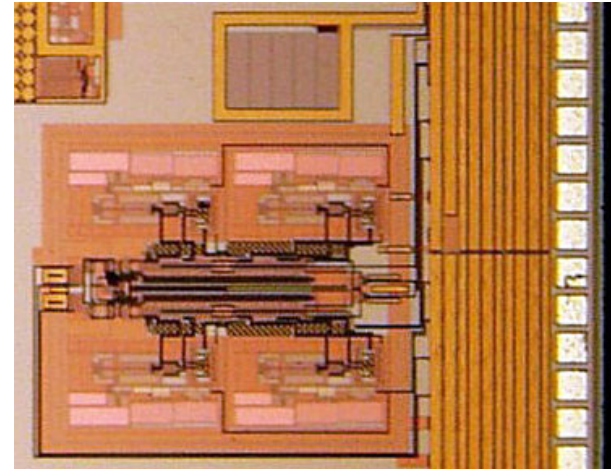
a	A
0	11(-1)
1	01(1)

2bit multiplier

A	B	OUT
11 (-1)	00 (0)	00 (0)
01 (1)	00 (0)	00 (0)
11 (-1)	01 (1)	11 (-1)
01 (1)	01 (1)	01 (1)
11 (-1)	11 (-1)	01 (1)
01 (1)	11 (-1)	11 (-1)
·	·	DC
·	·	DC
·	·	DC

Example of band-pass DSM

CMOS 0.25um,
OSR = 256,
4th-order noise shaping,
ENOB = 14bit



Down conversion, Decimation, and Decoding

