5. Data converters 2

(Nyquist-rate converters)

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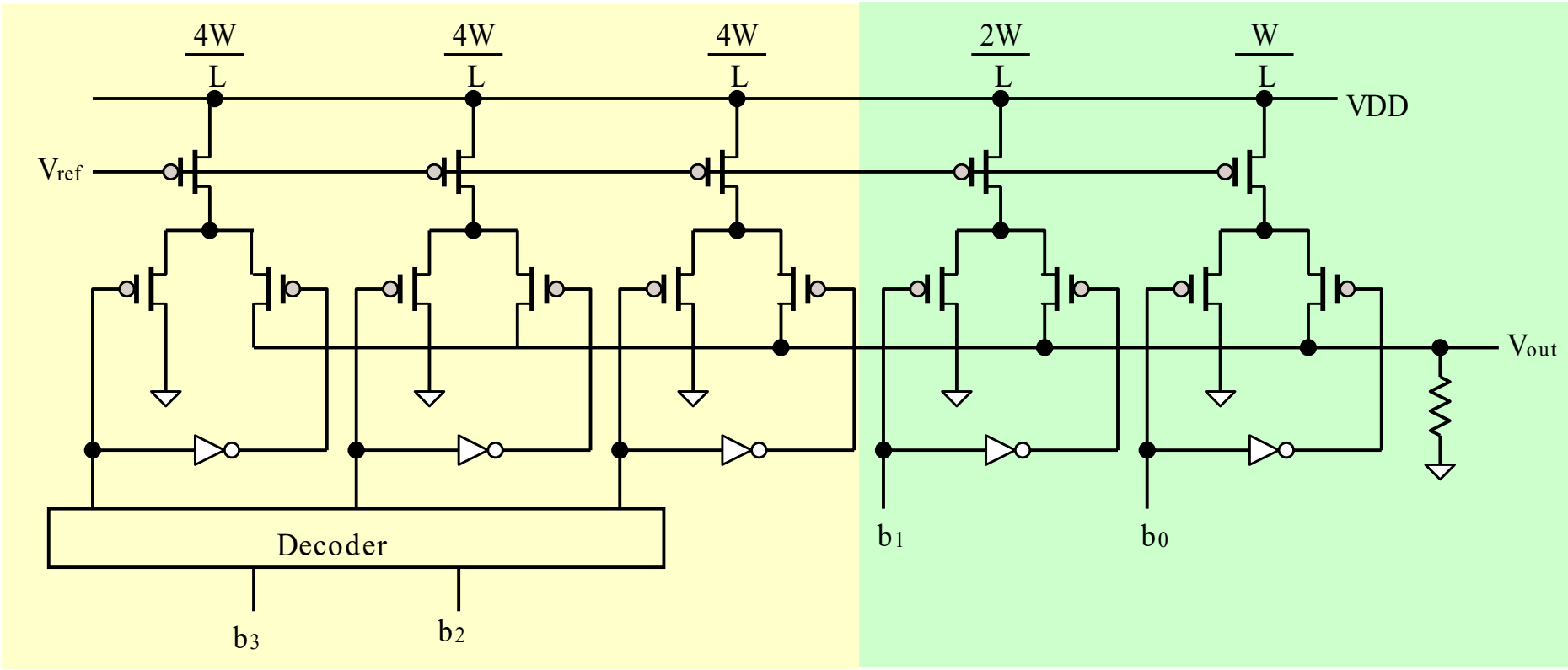
Akio Kitagawa

5.1 Current steering DAC (High speed and no glitch)

Basic circuit

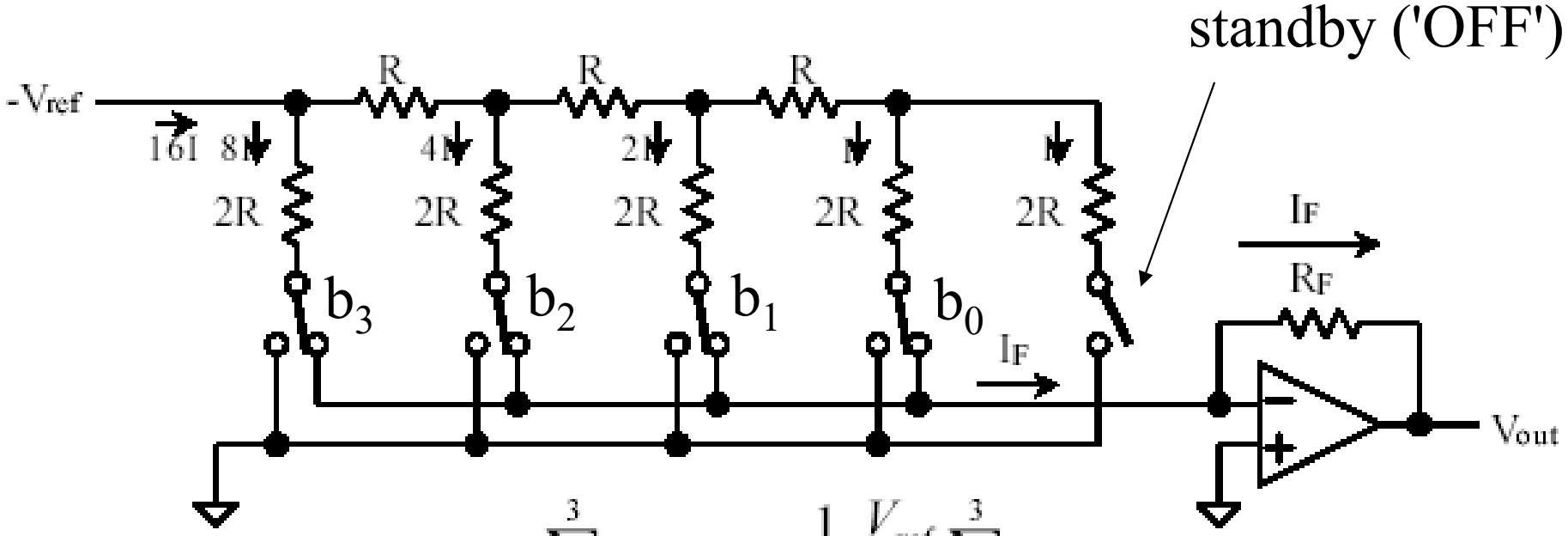


Thermometer code for high-order bits

Binary code for low-order bits

5.2 Current mode R-2R DAC (Small size)

Basic circuit

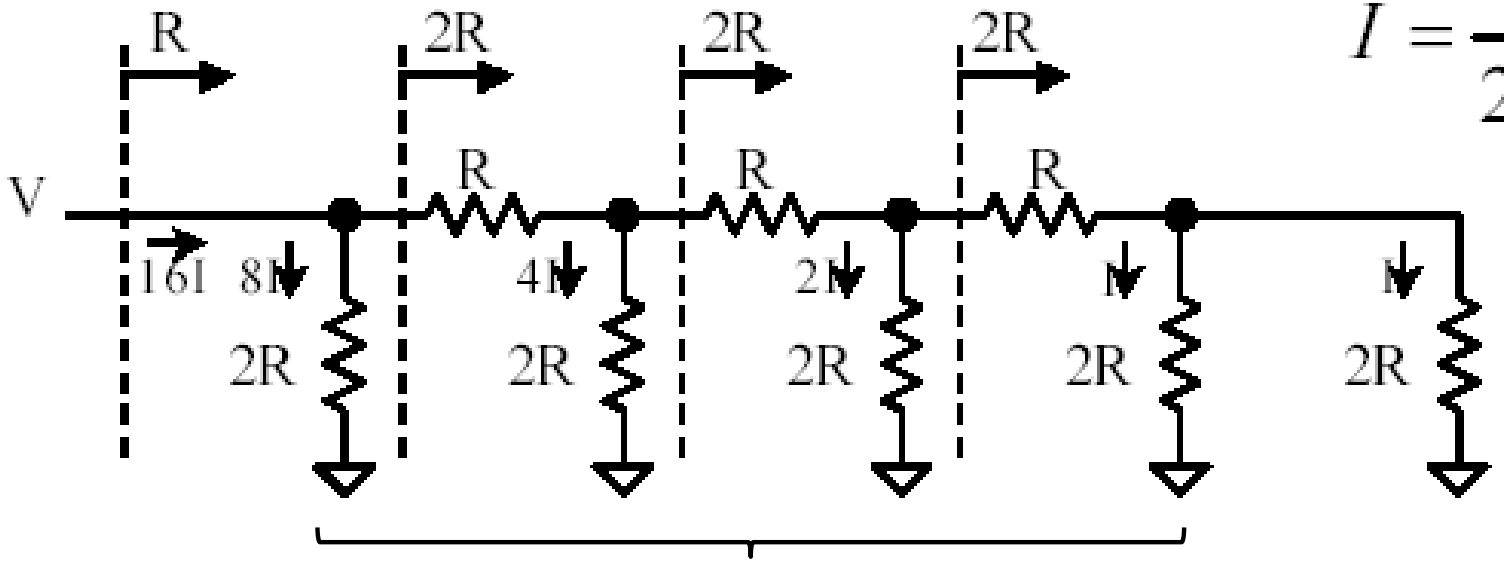


$$I_F = I\sum_{n=0}^{3} 2^n b_n = -\frac{1}{2^4}\frac{V_{ref}}{R}\sum_{n=0}^{3} 2^n b_n$$

$$V_{out} = -R_F I_F$$

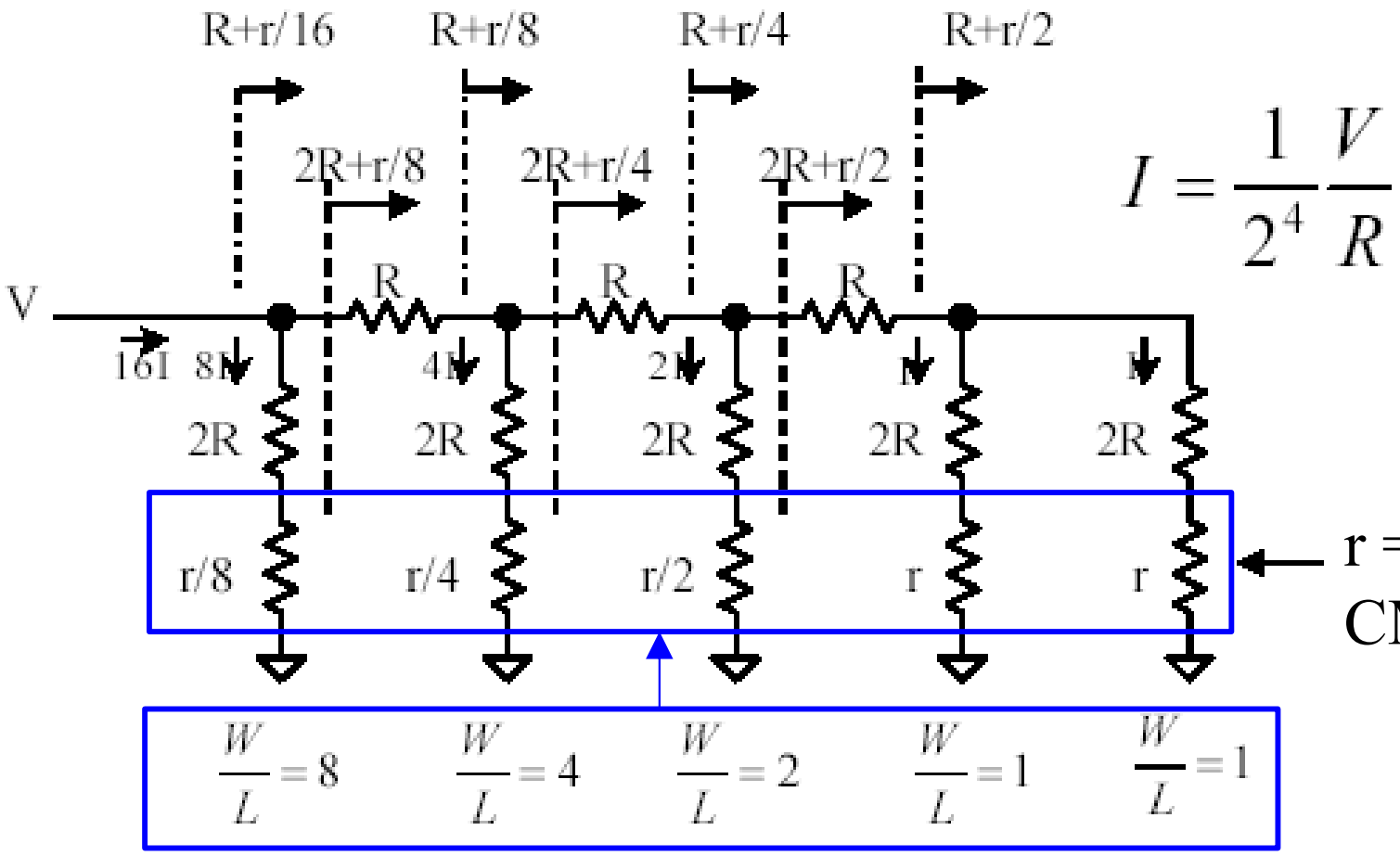
Principle of R-2R DAC

$$I = \frac{1}{2^4}\frac{V}{R}$$



The binary-weighted currents

Error reduction

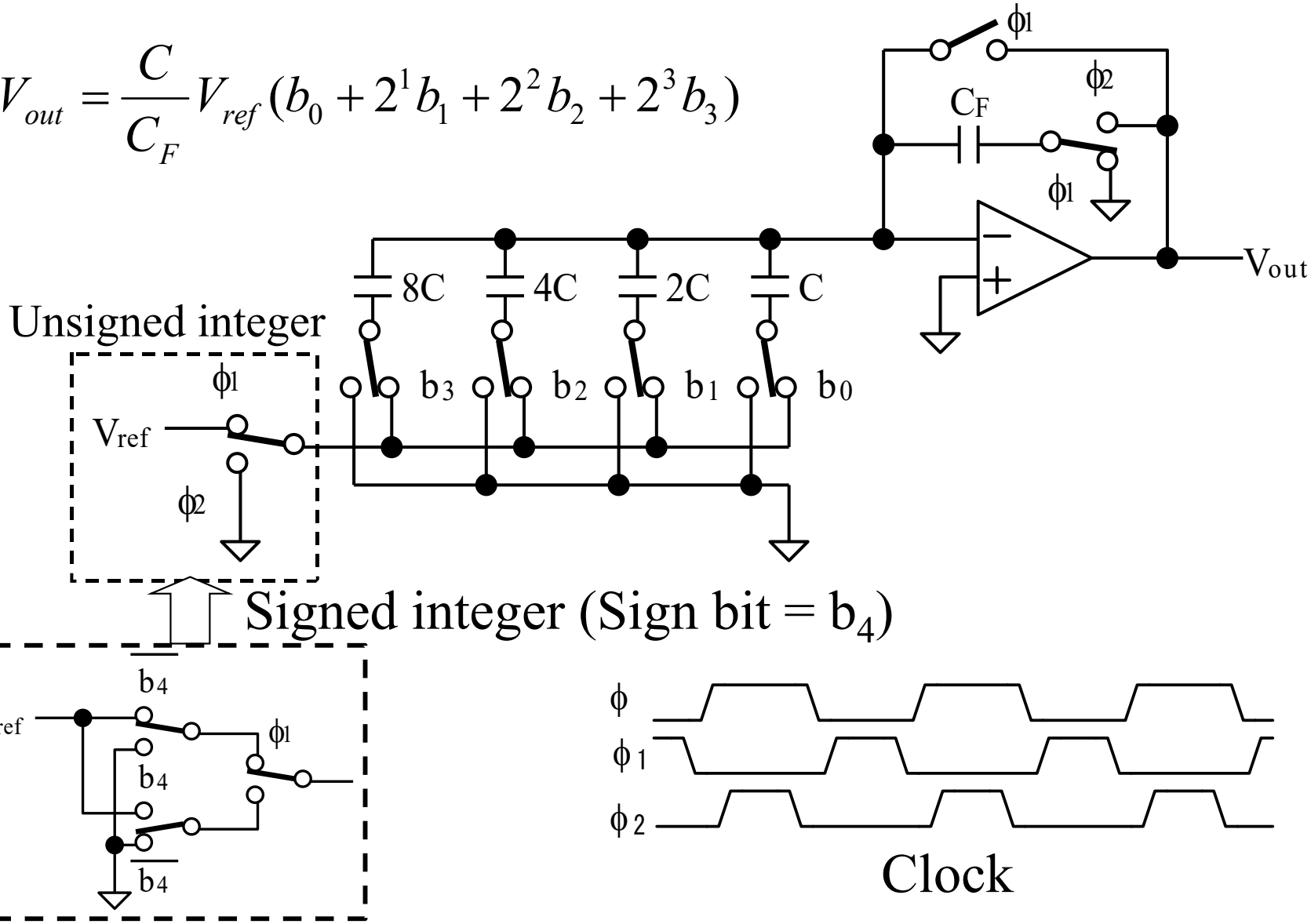


$$I = \frac{1}{2^4}\frac{V}{R}$$

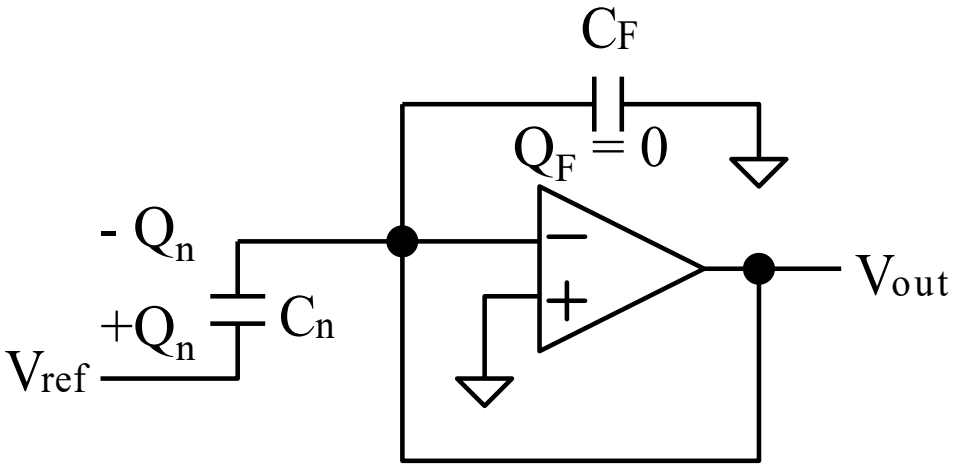
5.3 Charge scaling DAC (High precision and low power consumption)

Basic circuit

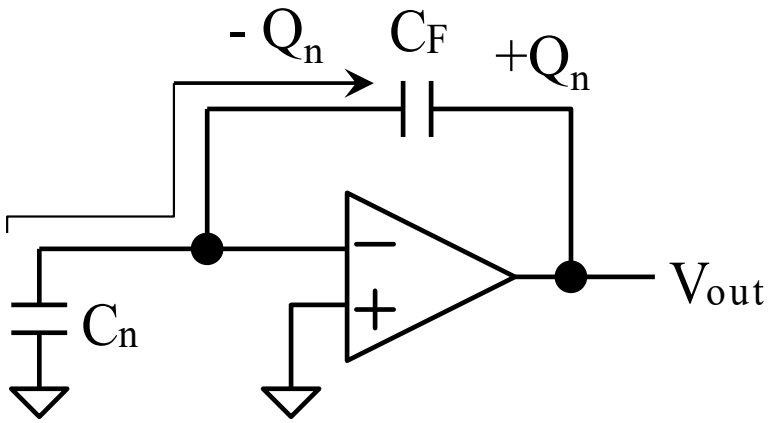
$$V_{out} = \frac{C}{C_F} V_{ref} (b_0 + 2^1 b_1 + 2^2 b_2 + 2^3 b_3)$$



Principle of operation



$$V_{ref} = \frac{Q_n}{C_n}$$



$$V_{out} = \frac{Q_n}{C_F} = \frac{C_n}{C_F} V_{ref}$$

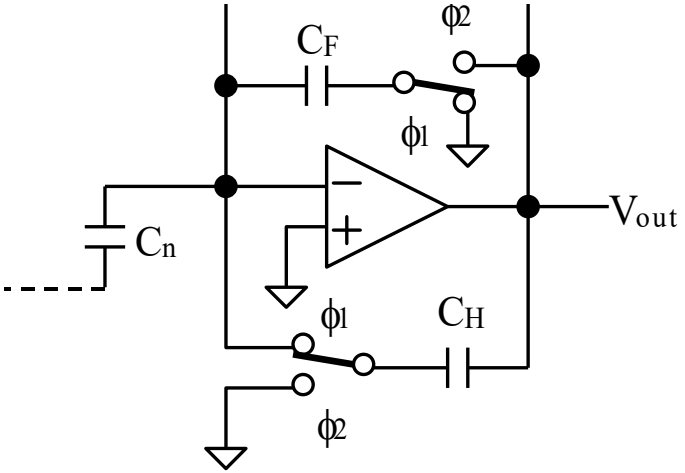
$$\text{Conversion gain} = \frac{C_n}{C_F}$$

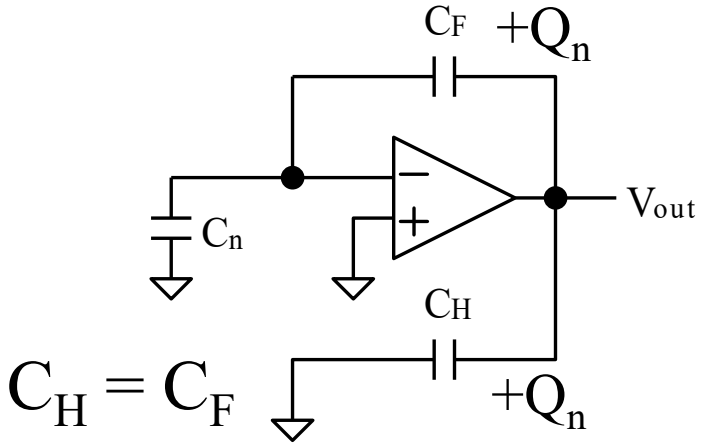
Phase ϕ_1
- Charge of C_n
- Discharge of C_F

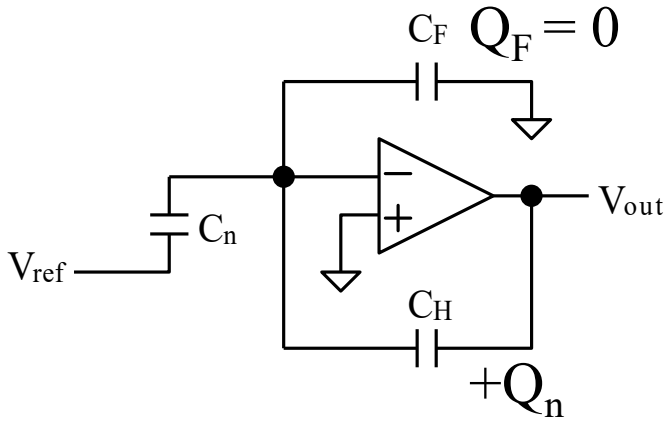
Phase ϕ_2
- Charge transfer of $-Q_n$
- Voltage output

Hold circuit of output voltage

The basic DAC circuit outputs the converted voltage only for ϕ2 phase. The hold circuit is added to hold the output for ϕ1 phase.





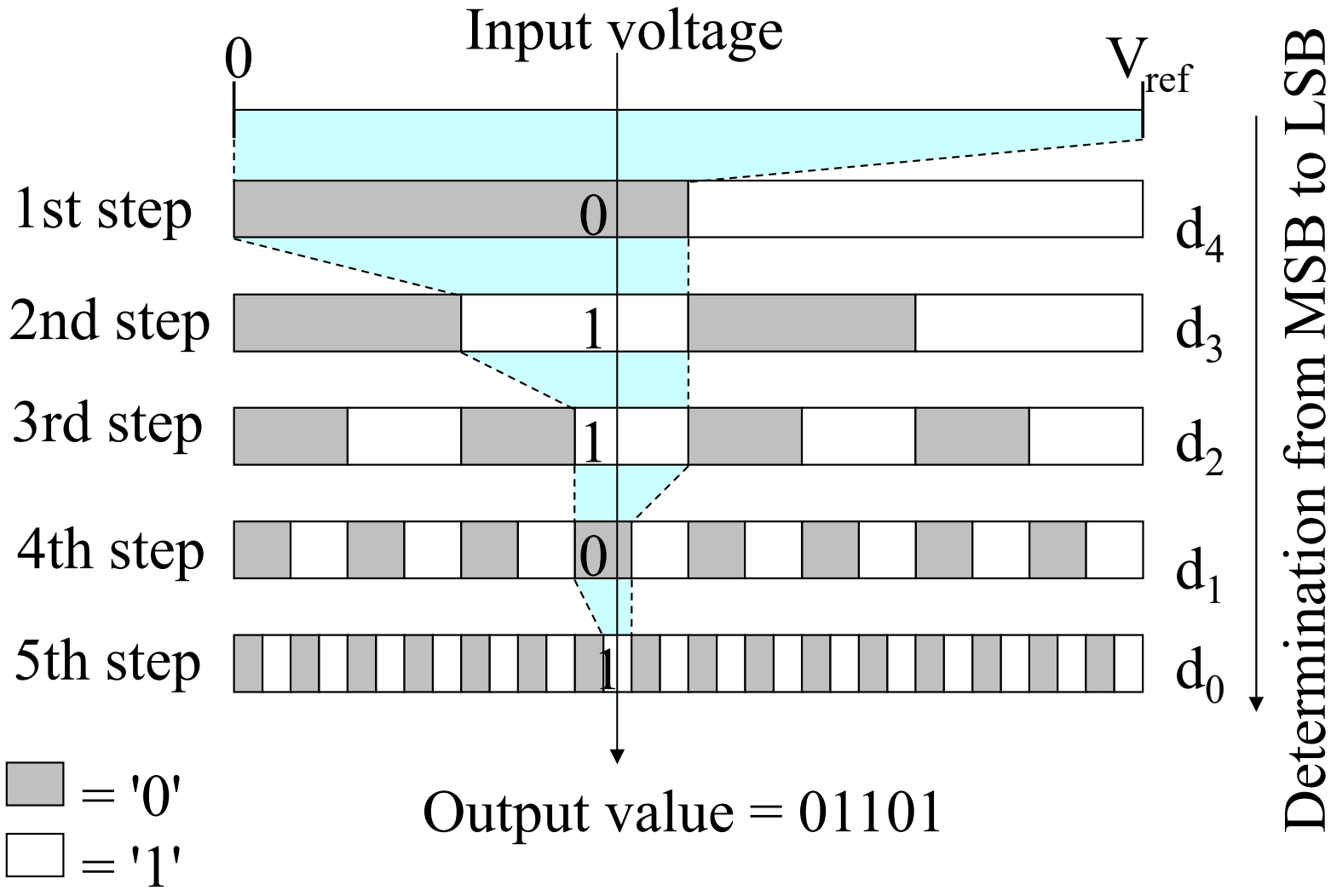


Sample mode in the phase ϕ2

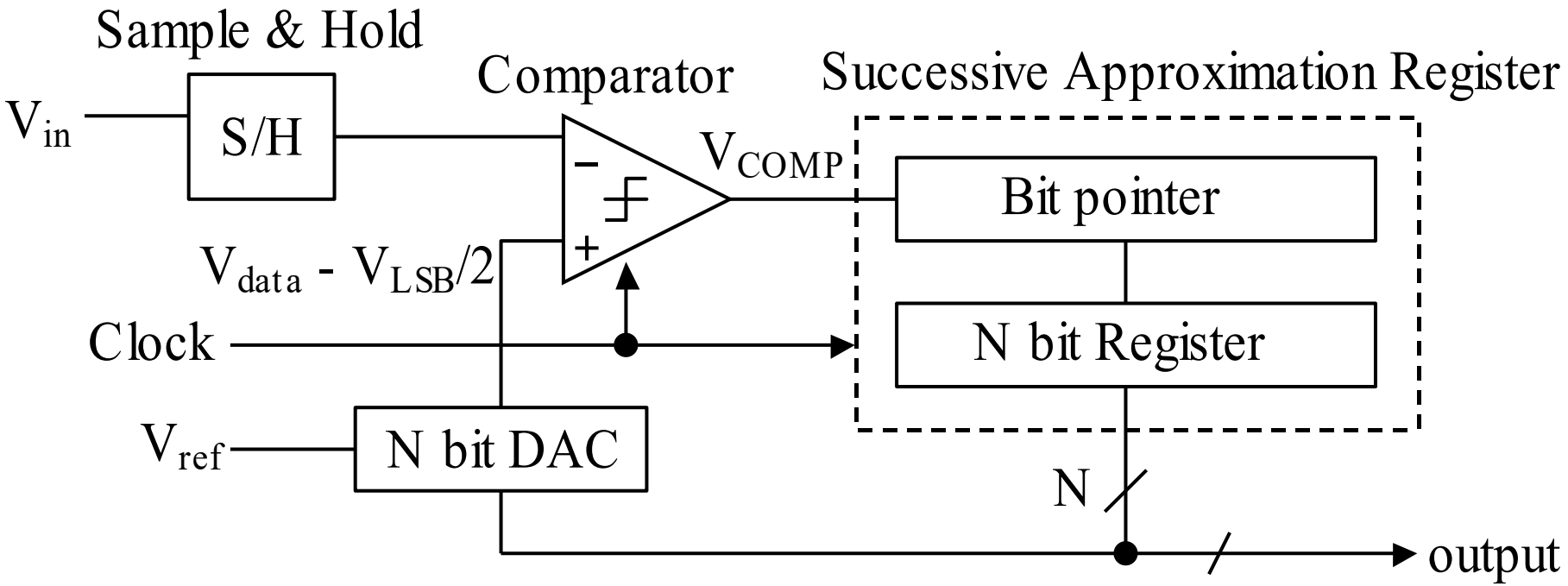
Hold mode in phase ϕ1

5.4 Successive Approximation Register (SAR) ADC (High precision and low power consumption)

Principle of operation

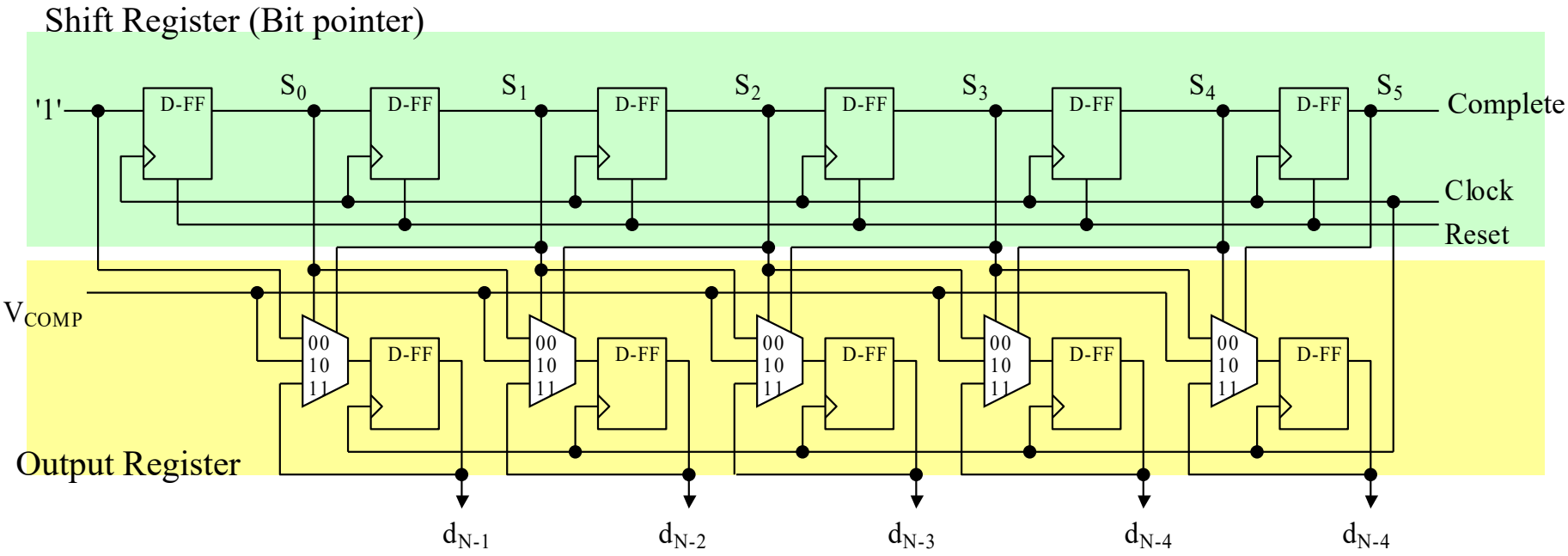


Block diagram of SAR-ADC



The SAR (Successive Approximation Register) controls holds the decided value and controls the output of DAC.

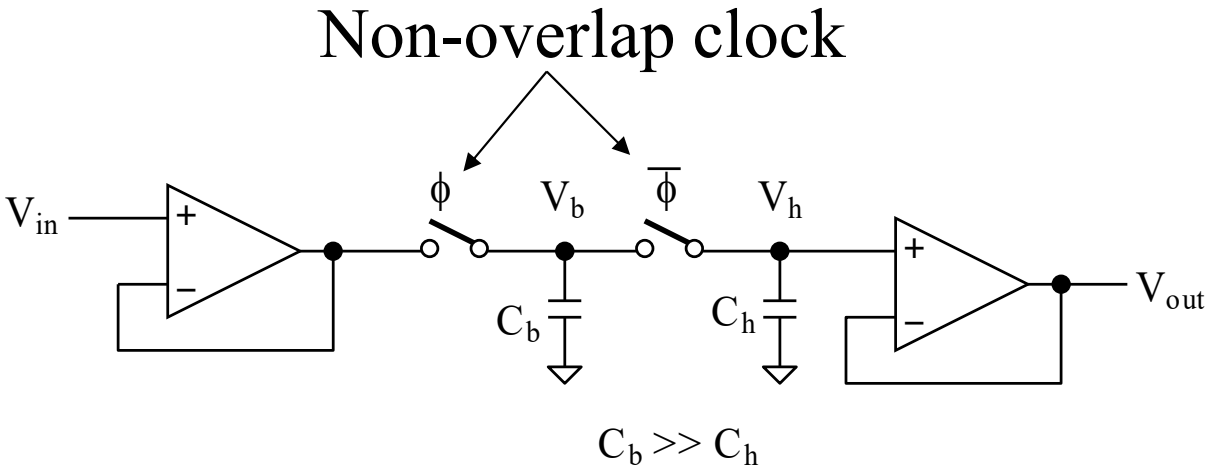
Circuit of SAR



Reset	0	0	0	0	0
1	1	0	0	0	0
2	d_{N-1}	1	0	0	0
3	d_{N-1}	d_{N-2}	1	0	0
4	d_{N-1}	d_{N-2}	d_{N-3}	1	0
5	d_{N-1}	d_{N-2}	d_{N-3}	d_{N-4}	1
6	d_{N-1}	d_{N-2}	d_{N-3}	d_{N-4}	d_{N-5}

Sample and Hold circuit (S/H)

- The input voltage of SAR-ADC have to hold for the conversion to prevent the conversion error.
- SAR-DAC requires an S/H circuit for the input stage.

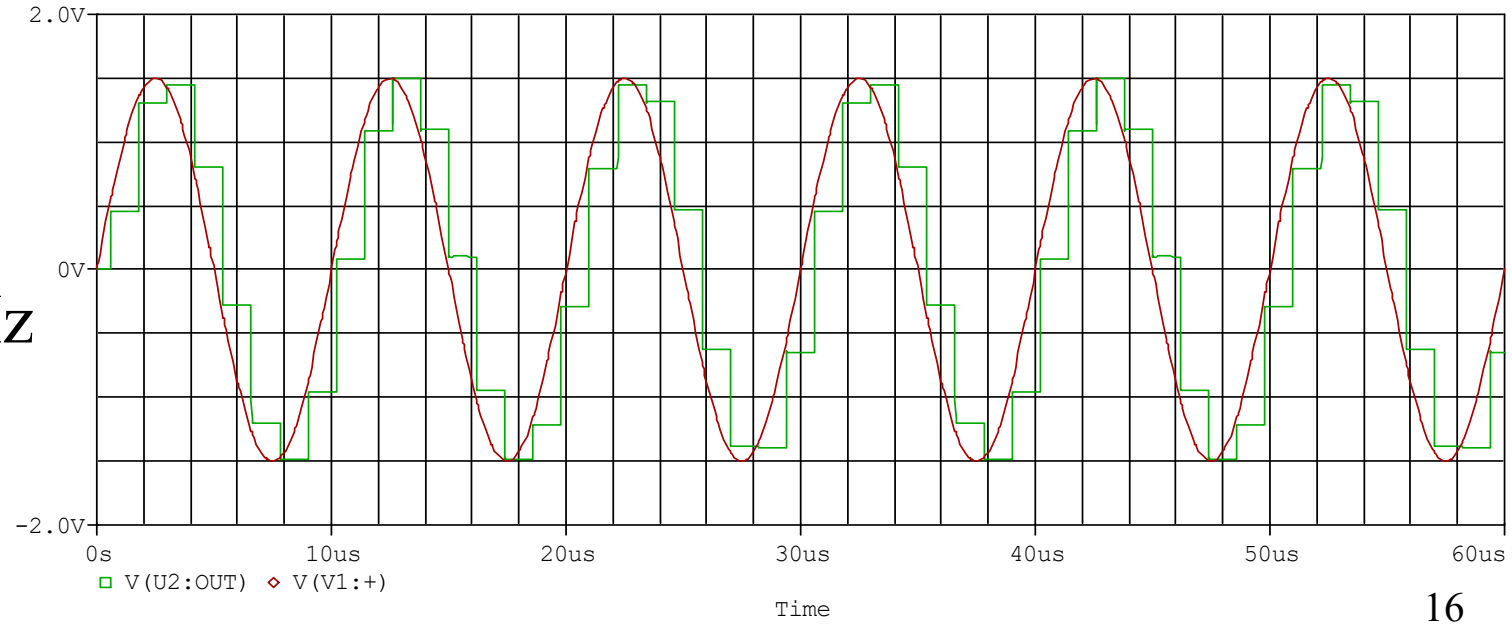


Simulation

$f_{in} = 100kHz$

$C_b = 10pF$

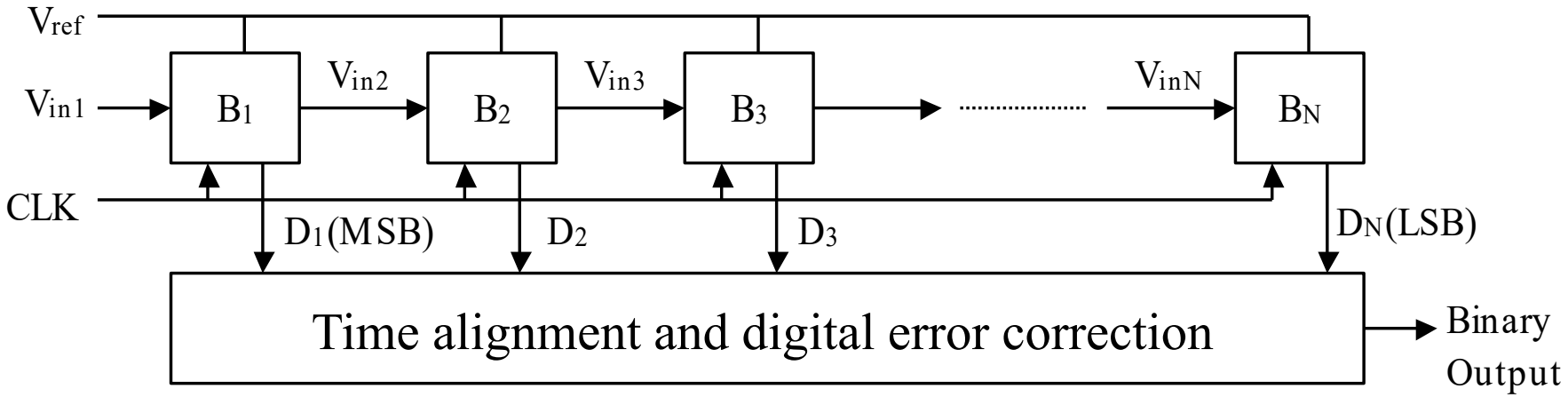
$C_h = 100fF$



5.5 Pipeline ADC
(High precision and high speed)

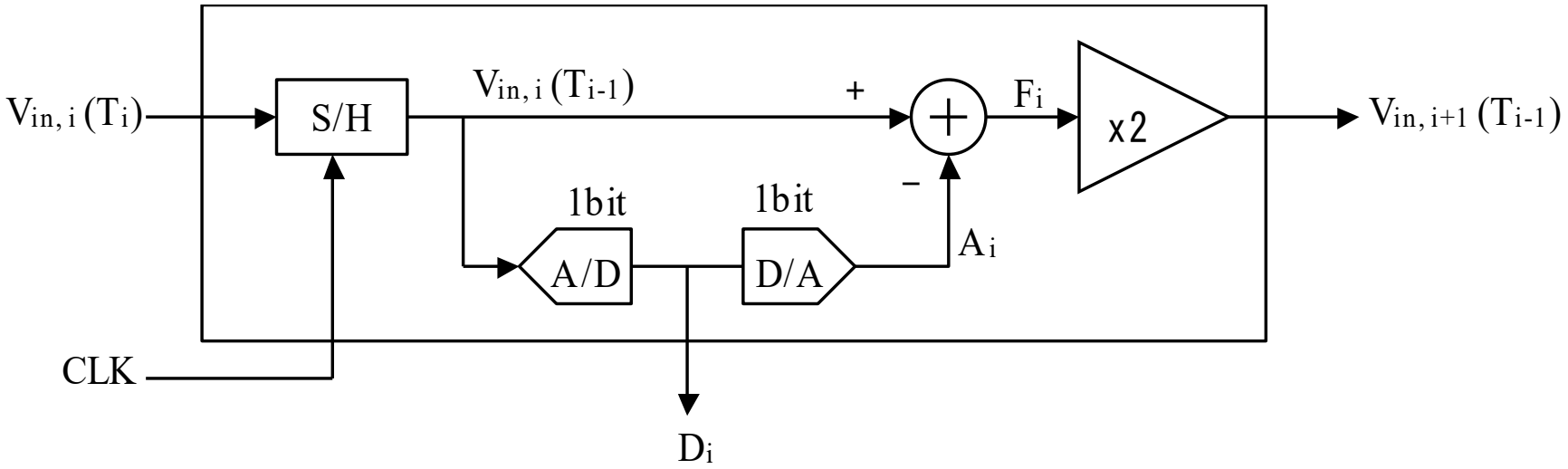
Block diagram of pipeline ADC

Instead of cycling the analog output of the 1-bit/stage section back to the input, the error output of the stage is fed into the subsequent stage, that is, this ADC is an open loop architecture.



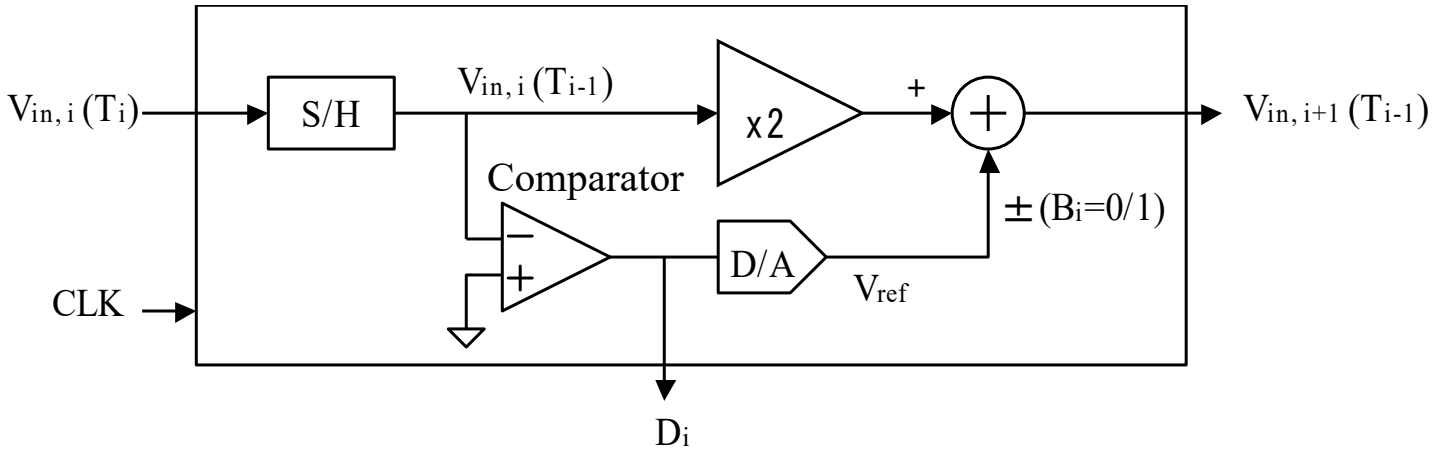
Each stage of $B_{1,2,\ldots N}$ has the digital output and the analog output of the quantization error. Each bit is determined for one clock cycle and N-bit conversion requires the N-clock cycles. The throughput of the conversion is 1-word per clock cycle through the pipeline processing.

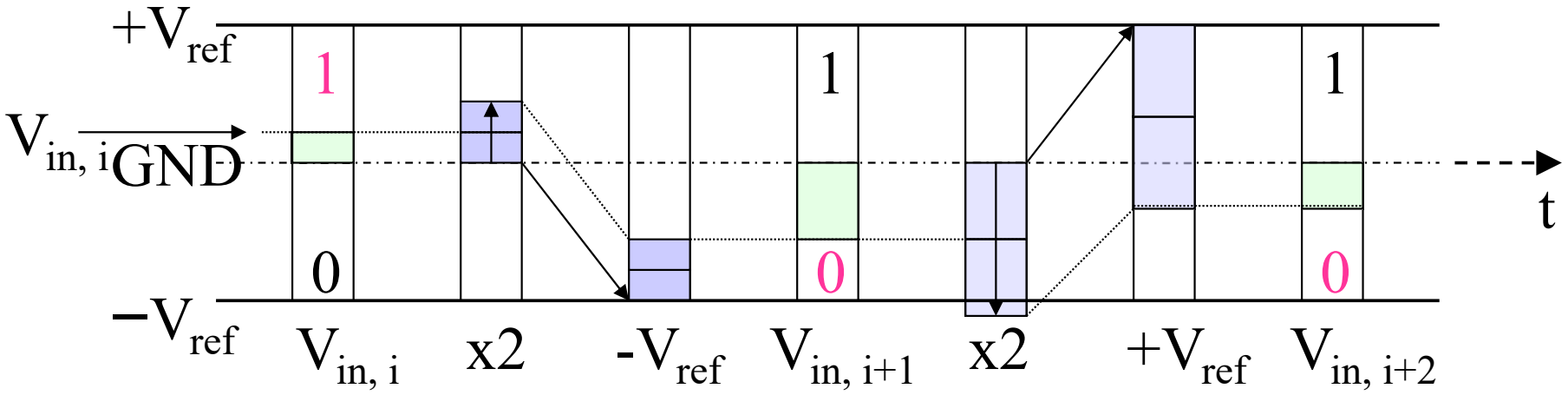
Basic operation in 1-bit/stage section



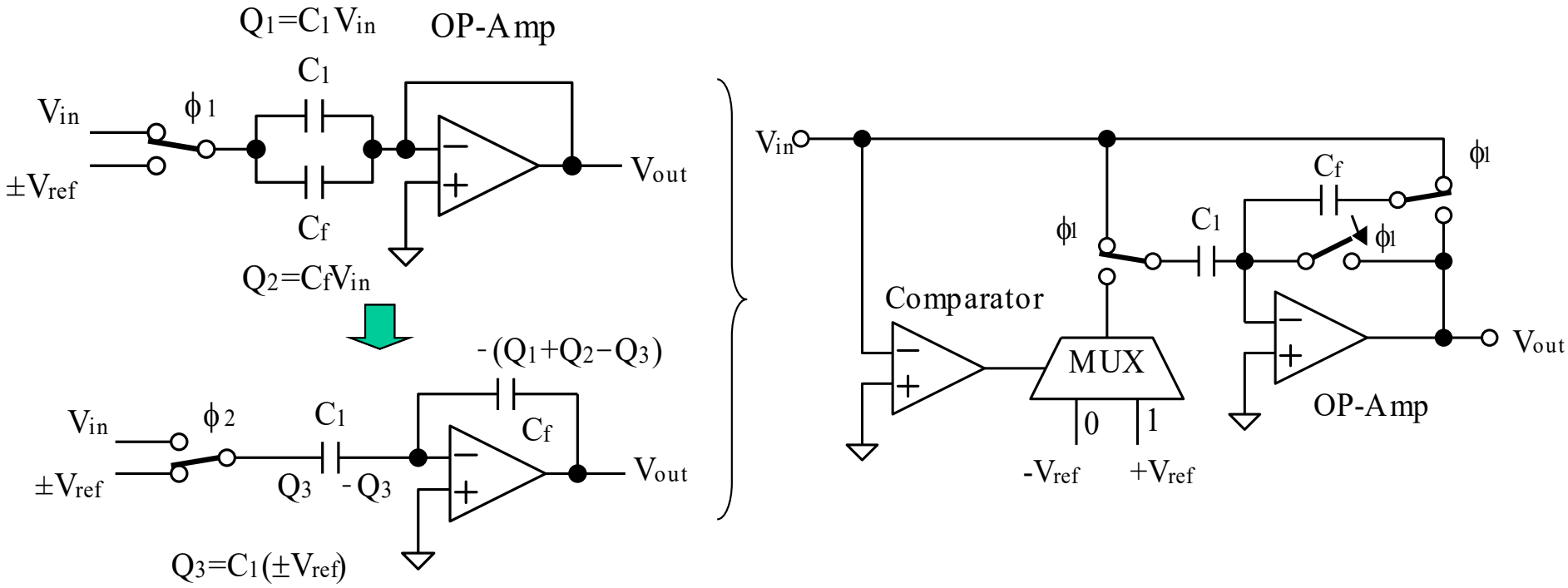
1. Sampling and holding analog signal $V_{in,\,i}$ with S/H circuit
2. Converting the analog signal into the 1 bit digital output Di
3. Converting Di into analog value A_i
4. Calculating the residual analog value $F_i = V_{in,\,i} - A_i$
5. Scaling the residual analog value F_i and sending it to the next stage

Practical implementation for double ended input





Design example of 1-bit/stage section

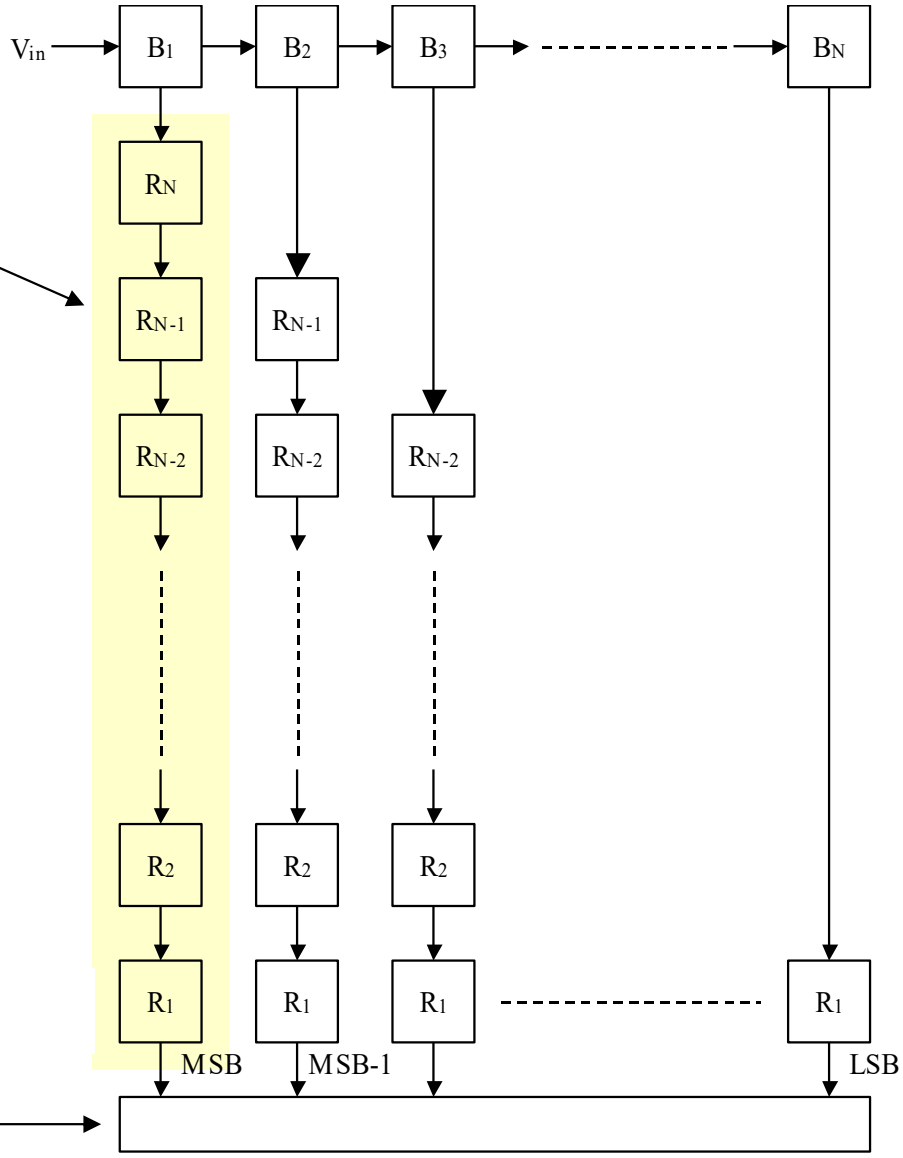


$$V_{out} = \frac{1}{C_f}(Q_1 + Q_2 - Q_3) = \frac{1}{C_f}\{(C_1 + C_f)\cdot V_{in} - C_1(\pm V_{ref})\} = \frac{C_1 + C_f}{C_f}V_{in} \mp \frac{C_1}{C_f}V_{ref}$$

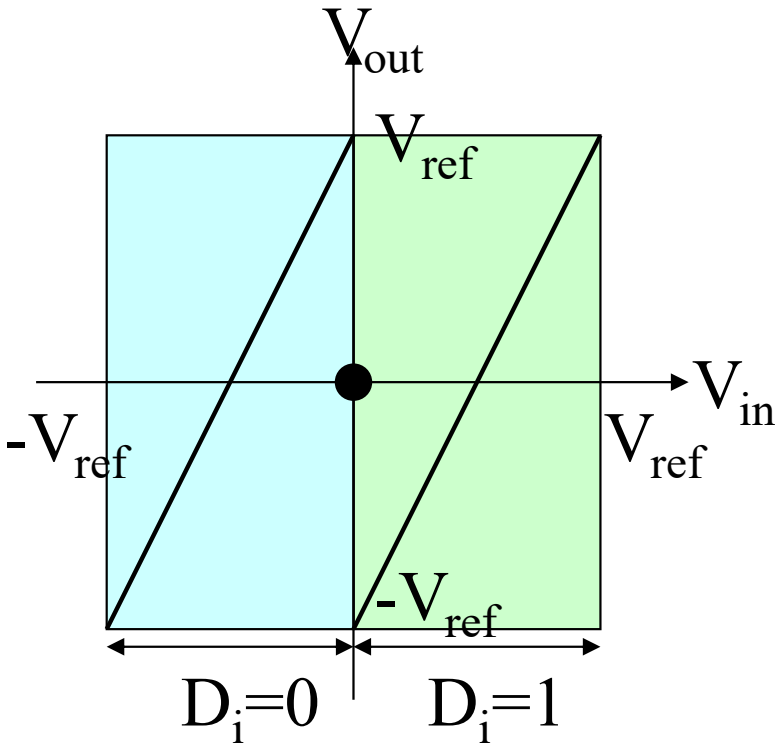
$$= 2V_{in} \mp V_{ref} \quad (\text{if } C_1 = C_f)$$

Time alignment

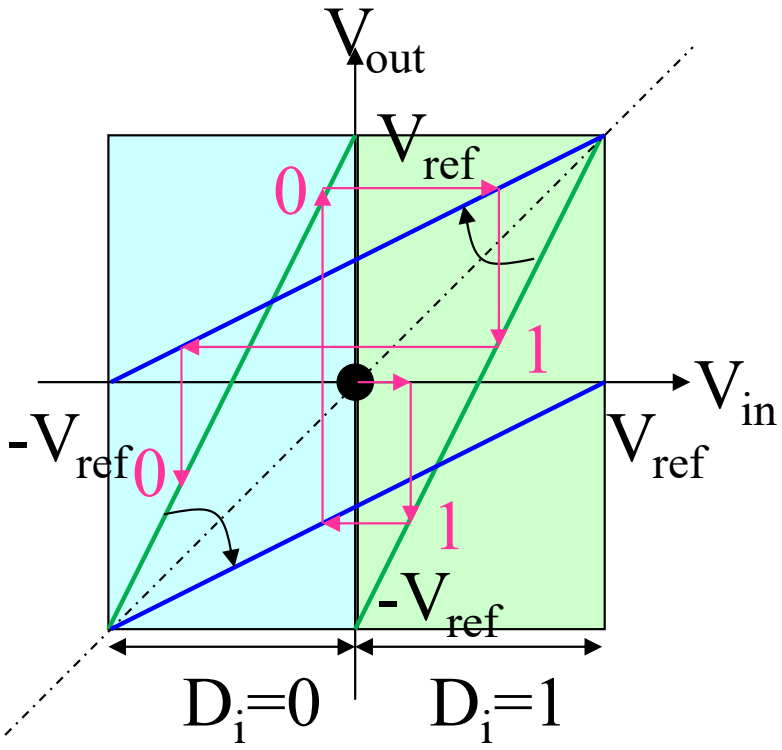
The output timing is aligned with the shift-registers.



Transfer characteristic of 1-stage



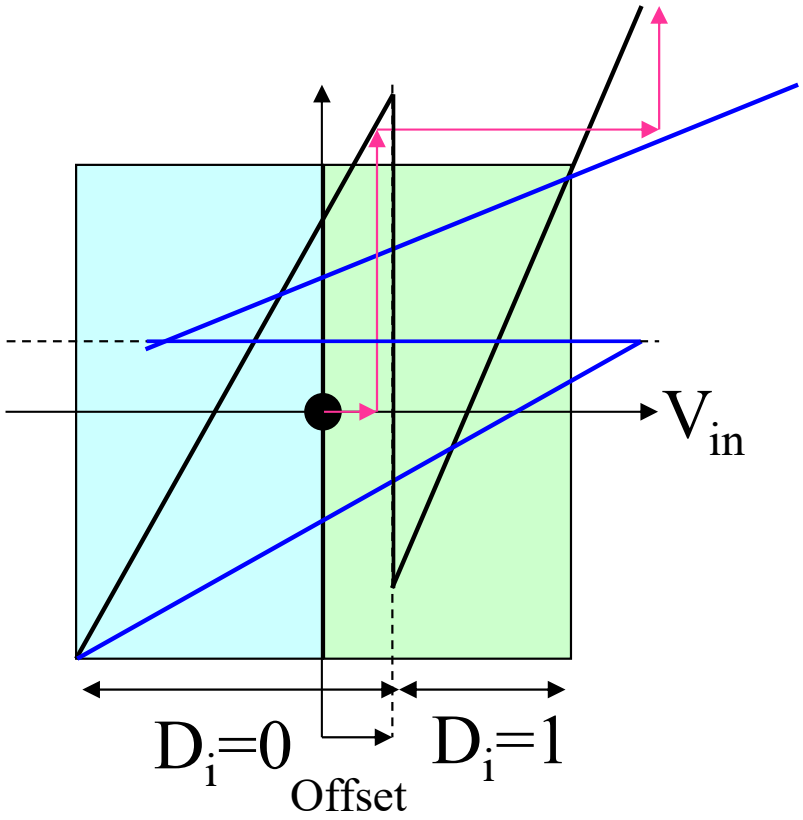
Transfer curve

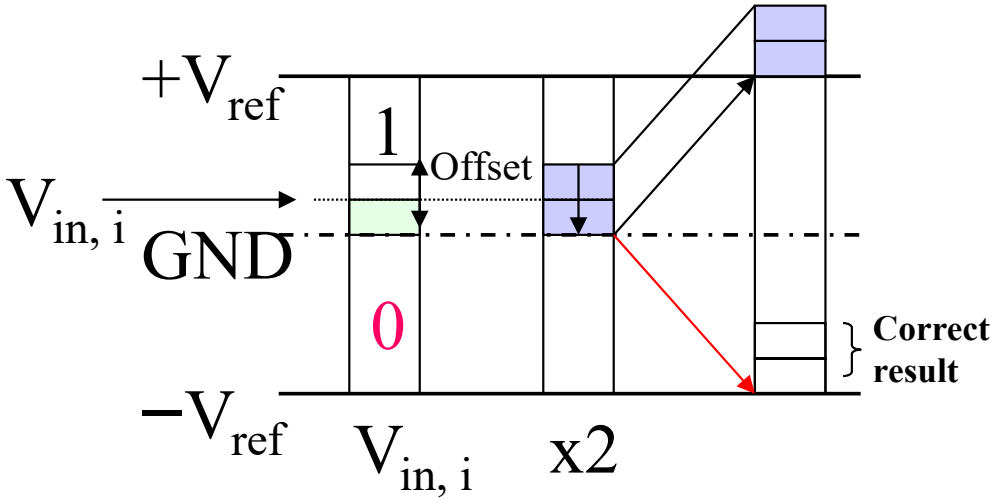


Transfer curve of B_n (Green) and B_{n+1} (Blue)

Error propagation

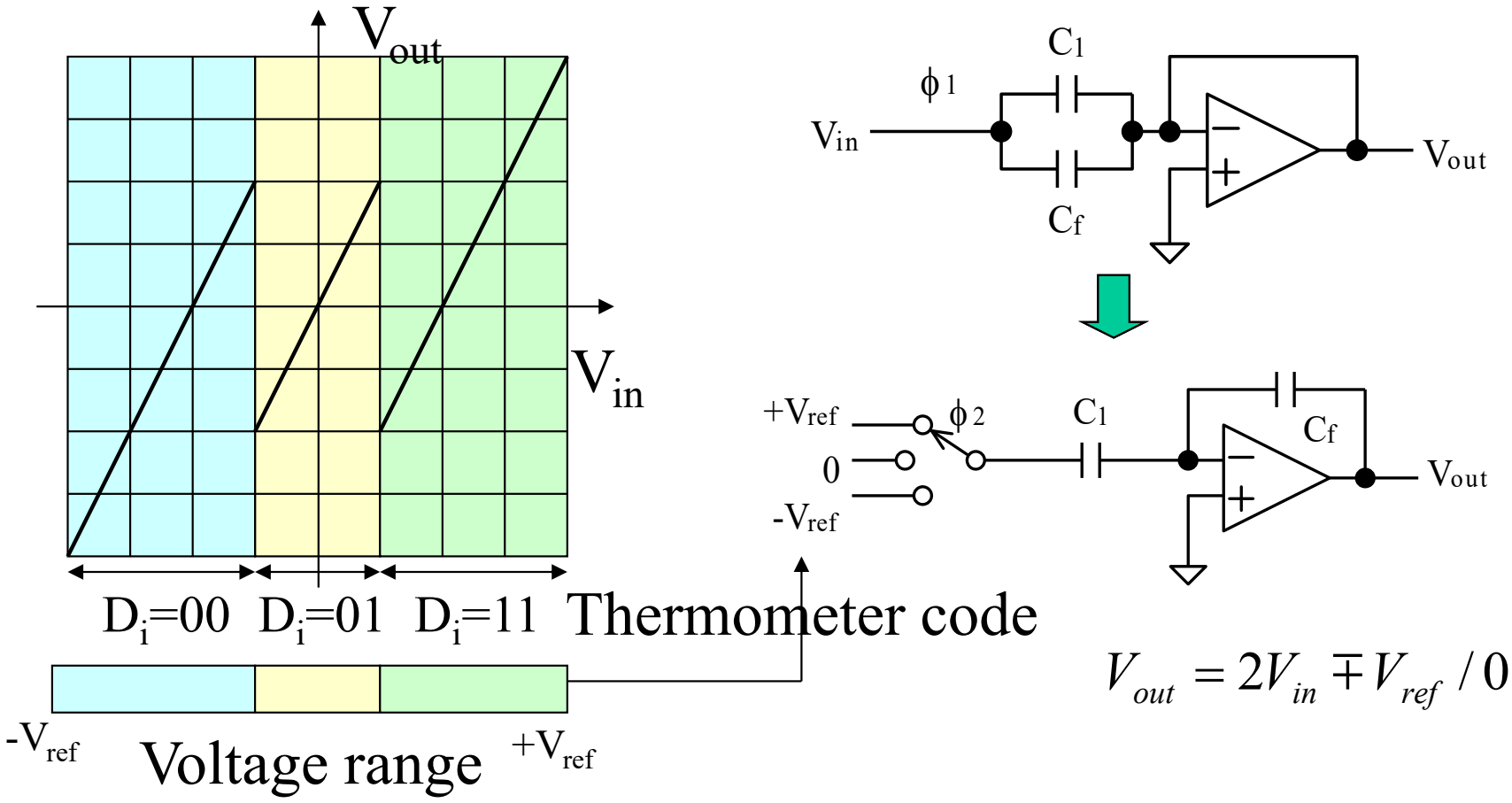
Transfer characteristic considering the comparator offset





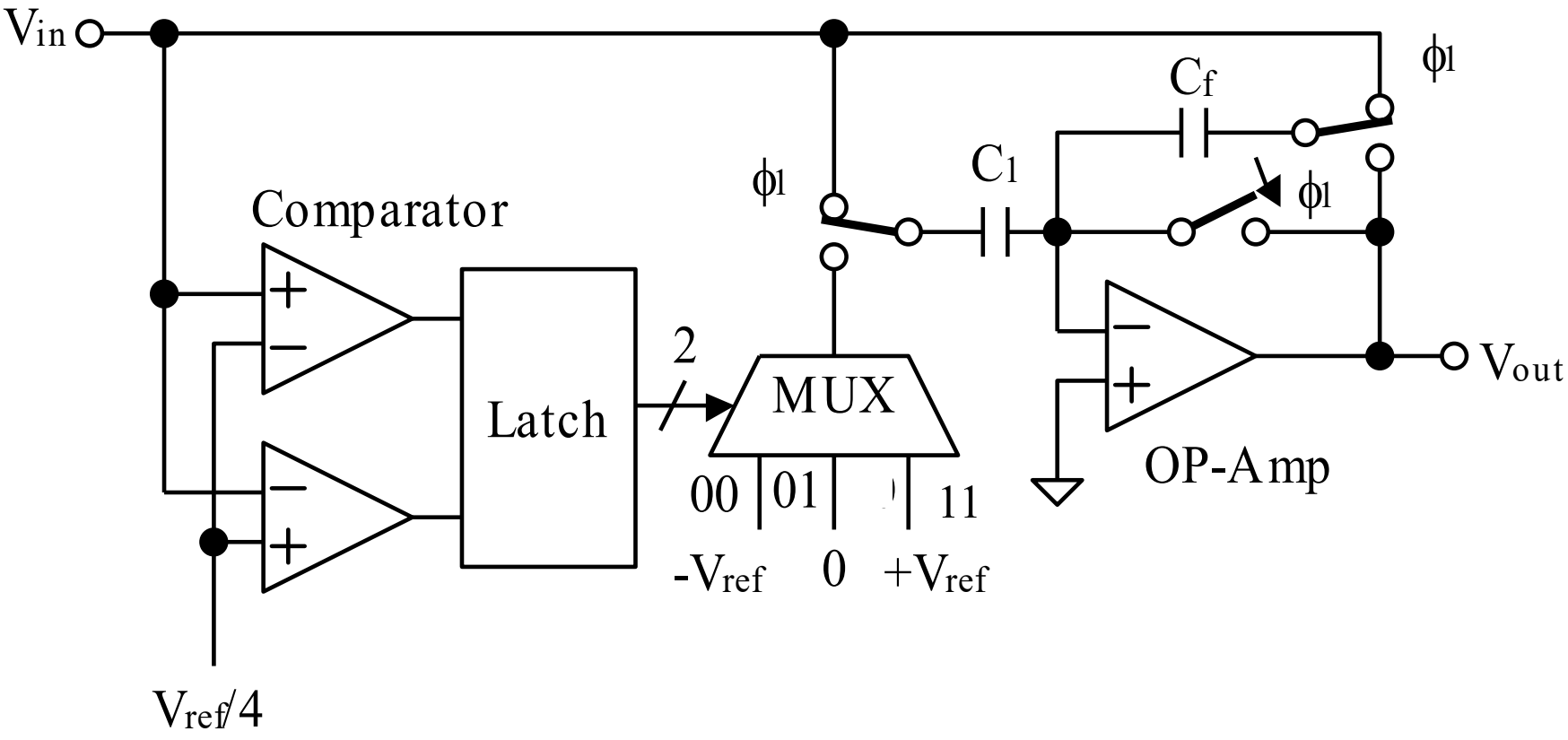
The comparator offset disturbs the convergence of the conversion result.

Transfer characteristic of 1.5 bit/stage



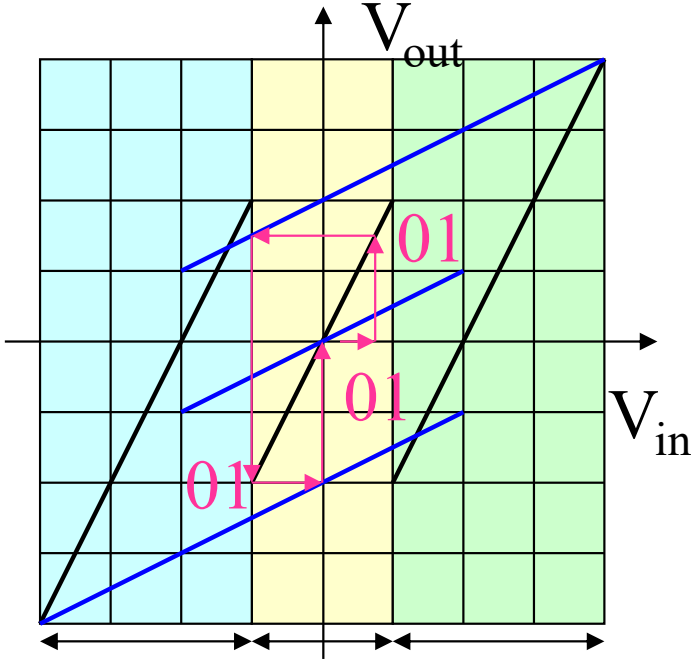
$$V_{out} = 2V_{in} \mp V_{ref} / 0$$

Design example of 1.5-bit/stage



Error compensation by 1.5bit stage

The comparator offset V_{off} temporarily makes the conversion error, however, the error is compensated by adding the conversion result of the previous stage, under the condition with $|V_{off}| < V_{ref}/4$.



$D_i=00 \quad D_i=01 \quad D_i=11 \rightarrow 10$

Decode

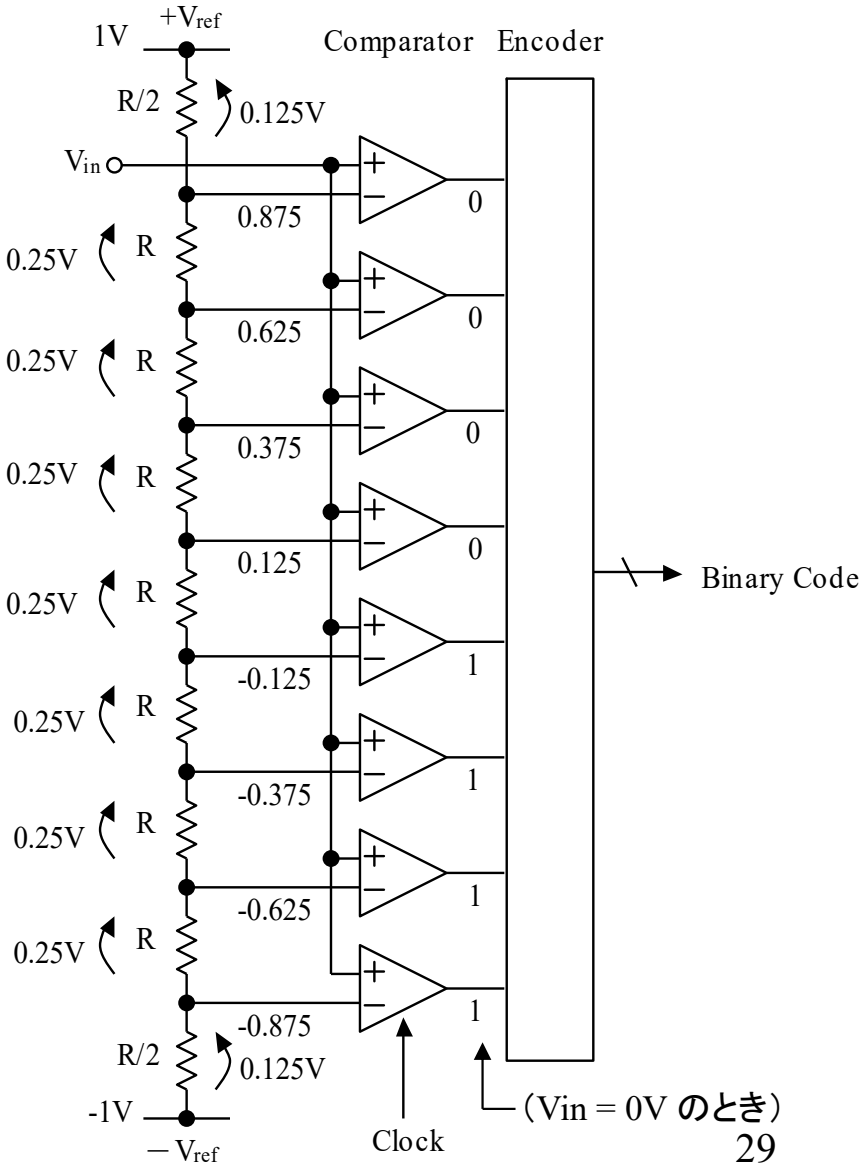
$$\begin{array}{r} 01 \\ 01 \\ +\ 01 \\ \hline 0111 \end{array}$$

Digital output

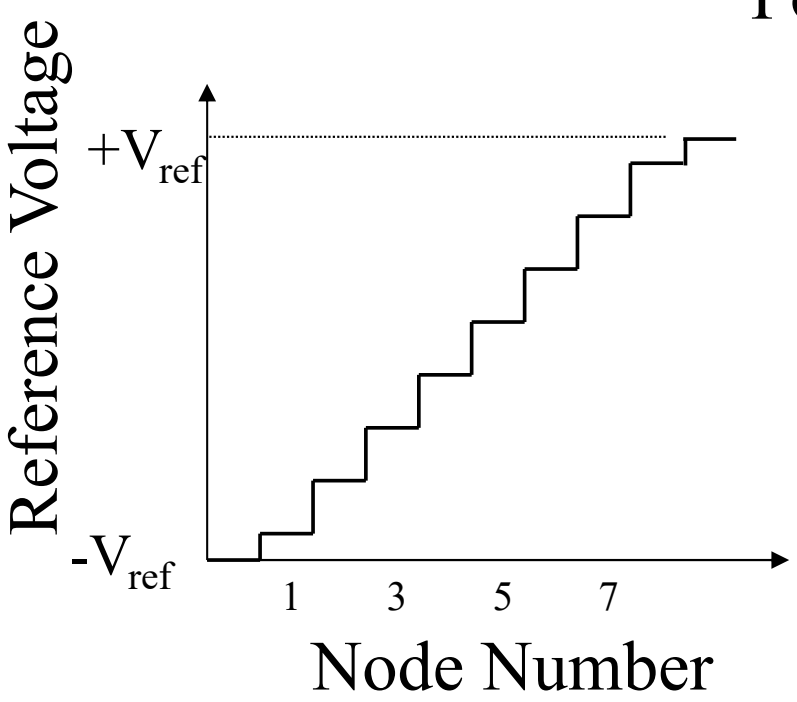
5.6 Flash and ADC (Very high speed and low latency)

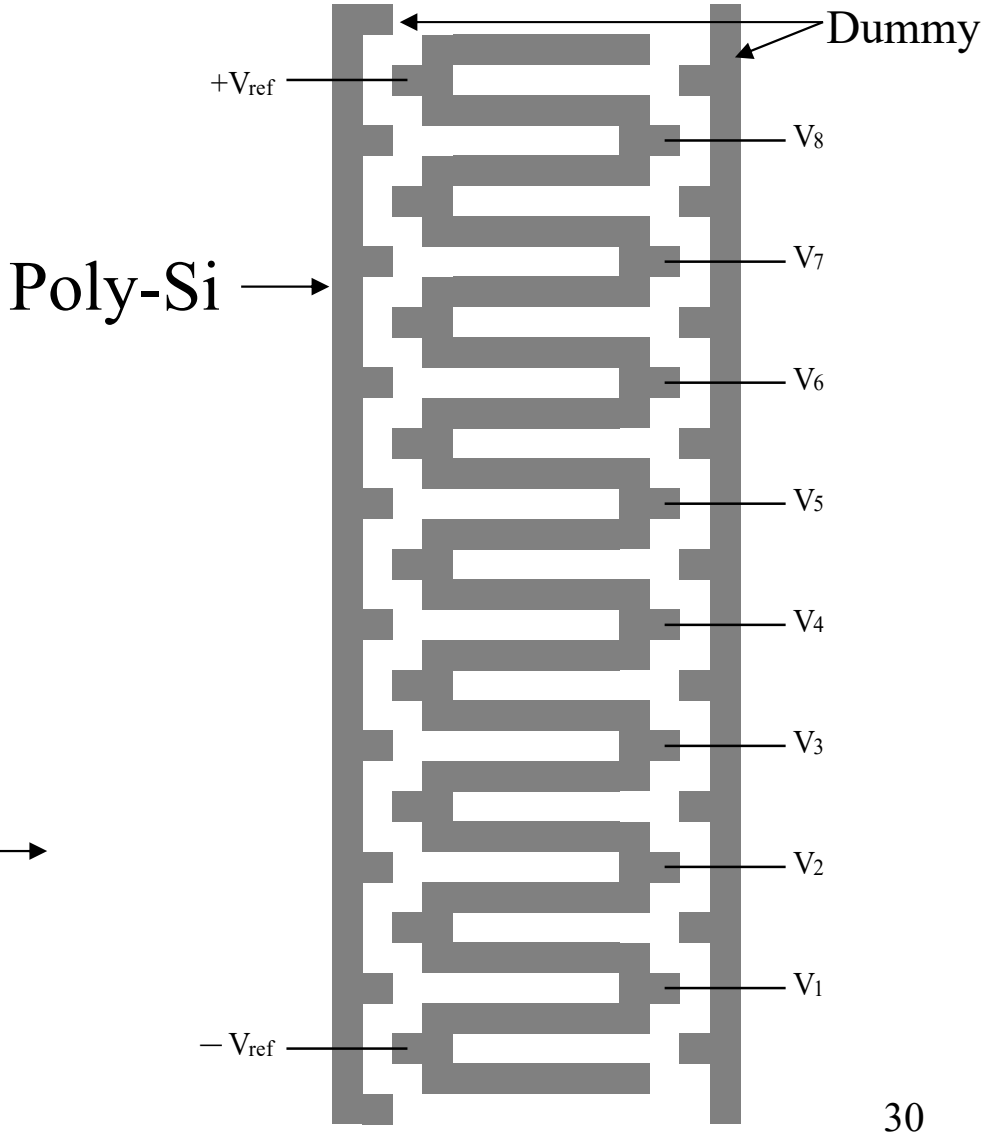
Basic circuit

- 予め N bit 分用意された比較用電圧と入力電圧をコンパレータで比較する
  - 全ビットを1回の比較で同時に決定するので高速
  - Nビットの精度では、2^N-1個のコンパレータが必要となり、回路規模と消費電力が大きい（8bit程度まで）



Reference voltage

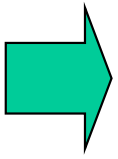




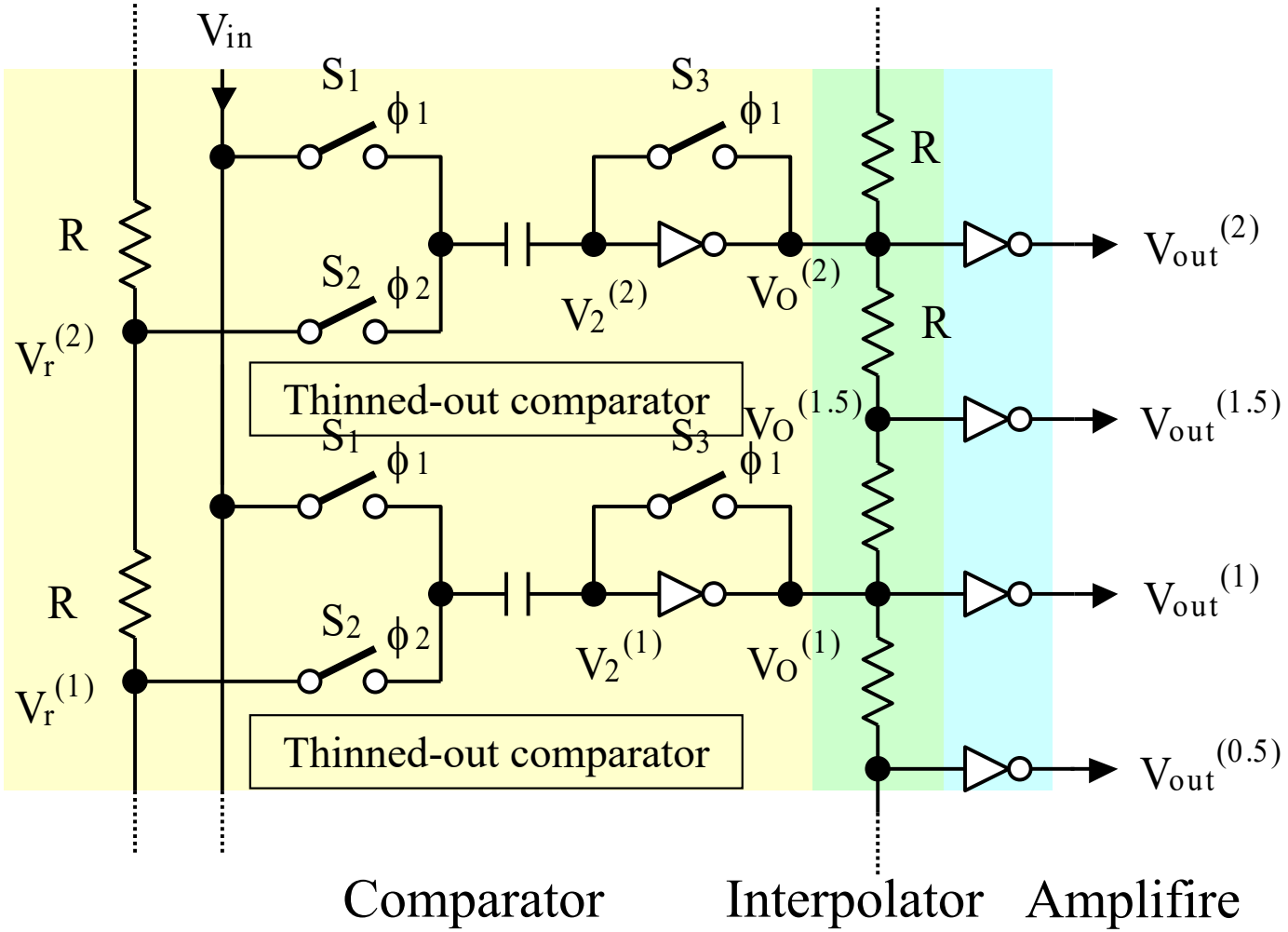
Thermometer encoder

Vin (V) (V_{ref} = 1V)	Thermometer Code (Comparator Output)		Binary Code (Encoder Output)
~ -0.875	0 0 0 0	0 0 0 0	0 0 0
-0.875 ~ -0.625	0 0 0 0	0 0 0 1	0 0 1
-0.625 ~ -0.375	0 0 0 0	0 0 1 1	0 1 0
-0.375 ~ -0.125	0 0 0 0	0 1 1 1	0 1 1
-0.125 ~ 0.125	0 0 0 0	1 1 1 1	1 0 0
0.125 ~ 0.375	0 0 0 1	1 1 1 1	1 0 1
0.375 ~ 0.625	0 0 1 1	1 1 1 1	1 1 0
0.625 ~ 0.875	0 1 1 1	1 1 1 1	1 1 1
0.875 ~	1 1 1 1	1 1 1 1	(1) 0 0 0

Encode

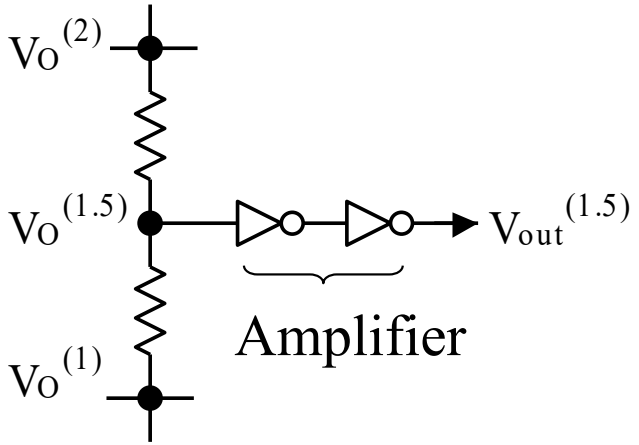


Reduction of the number of comparators

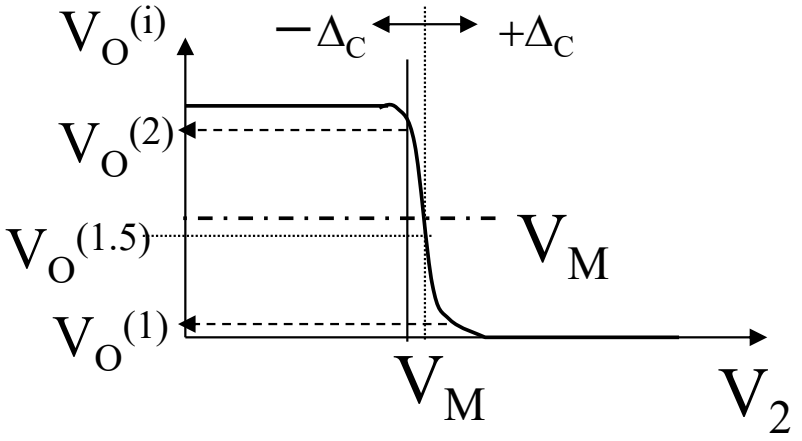


Interpolation methods of comparator

$V_O^{(1)}$	$V_O^{(2)}$	$V_{out}^{(1.5)}$
H	H	H
H	L	Error
L	H	Interpolation
L	L	L



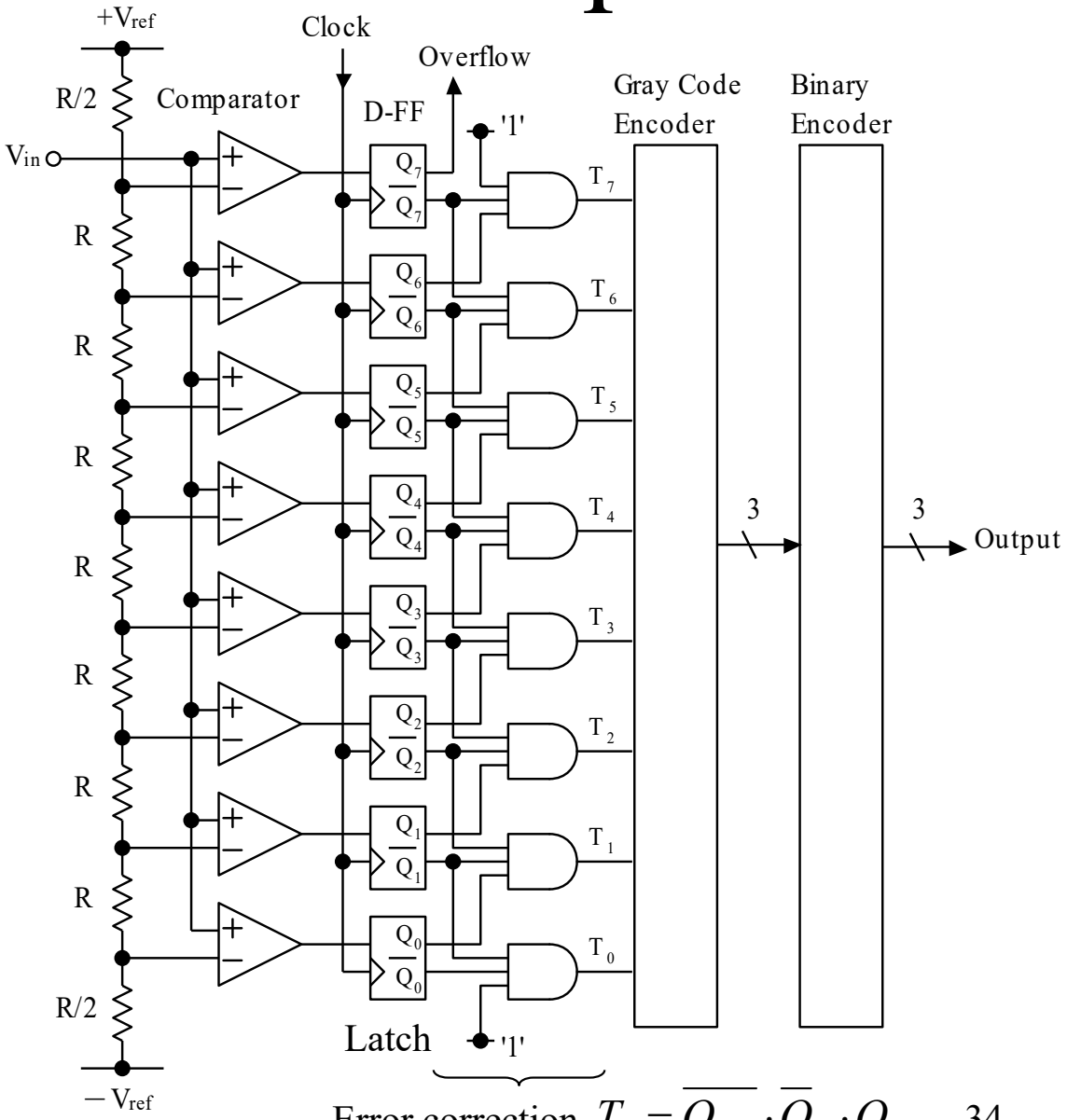
When $V_r^{(2)} < V_{in} < V_r^{(1)}$, $V_O^{(1.5)} = (V_O^{(1)} + V_O^{(2)})/2$ is compared with the threshold voltage V_M of the subsequent inverter.



Error correction of comparator

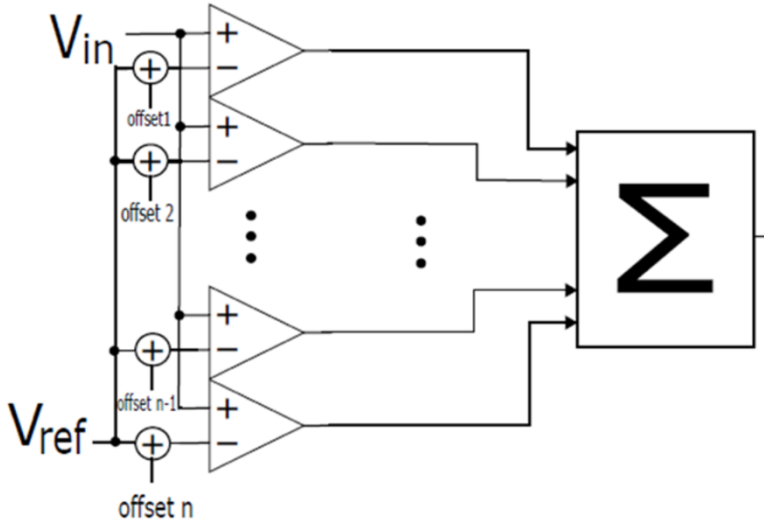
The error correction circuit corrects the bit inversion in the thermometer code.
Gray code encoder converts the adjacent 1-bit error into the error of LSB.

Q_{n+1}	Q_n	Q_{n-1}	T_n
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



5.7 Stochastic ADC (Very high precision)

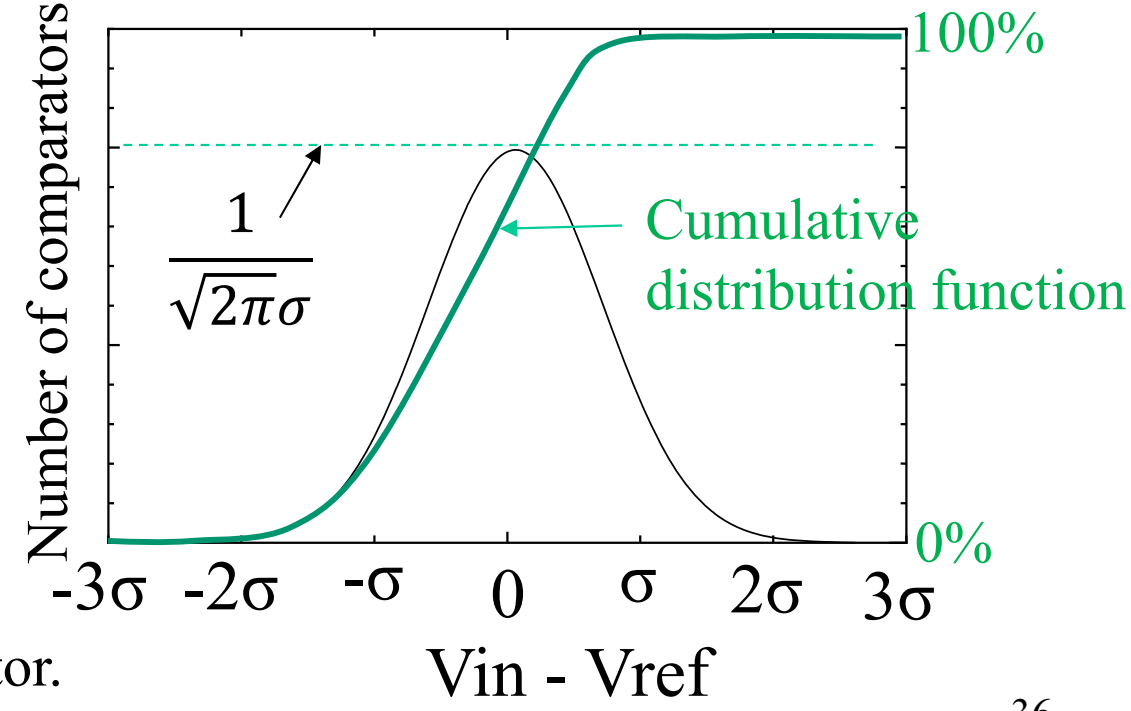
Principle of operation



$$N_{ENOB}(\text{bit}) = log_4 \frac{N_{comparators}}{2}$$

Digital output

Statistical dispersion of comparators

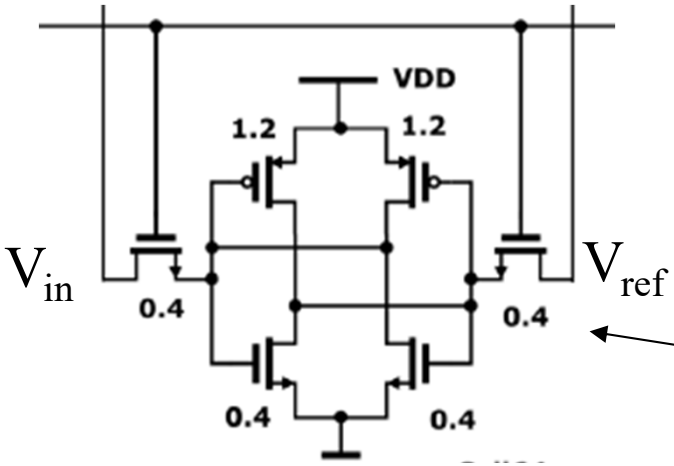


NOTE: The effective number of bits does not depends on the operational precision of the comparators, but it depends on the number of comparators.

⇩

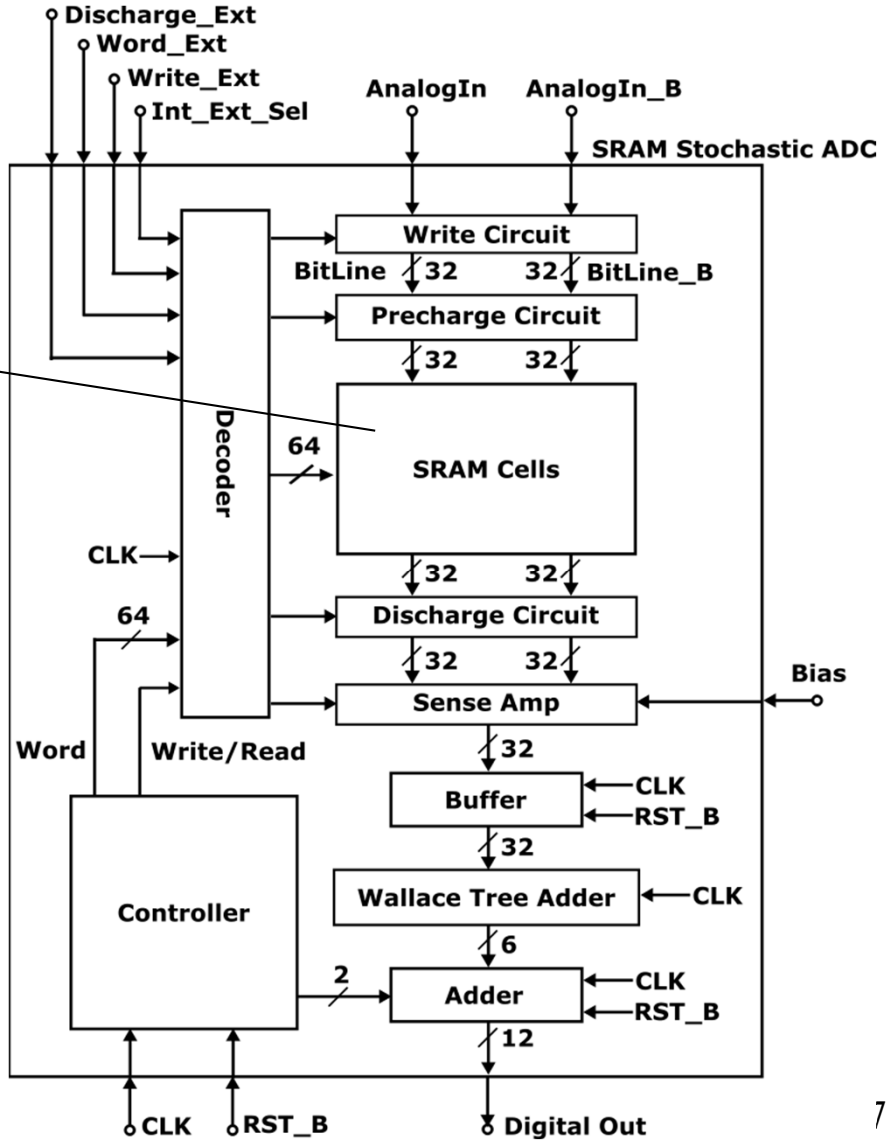
A latch can be used as a comparator.

Block diagram of stochastic ADC



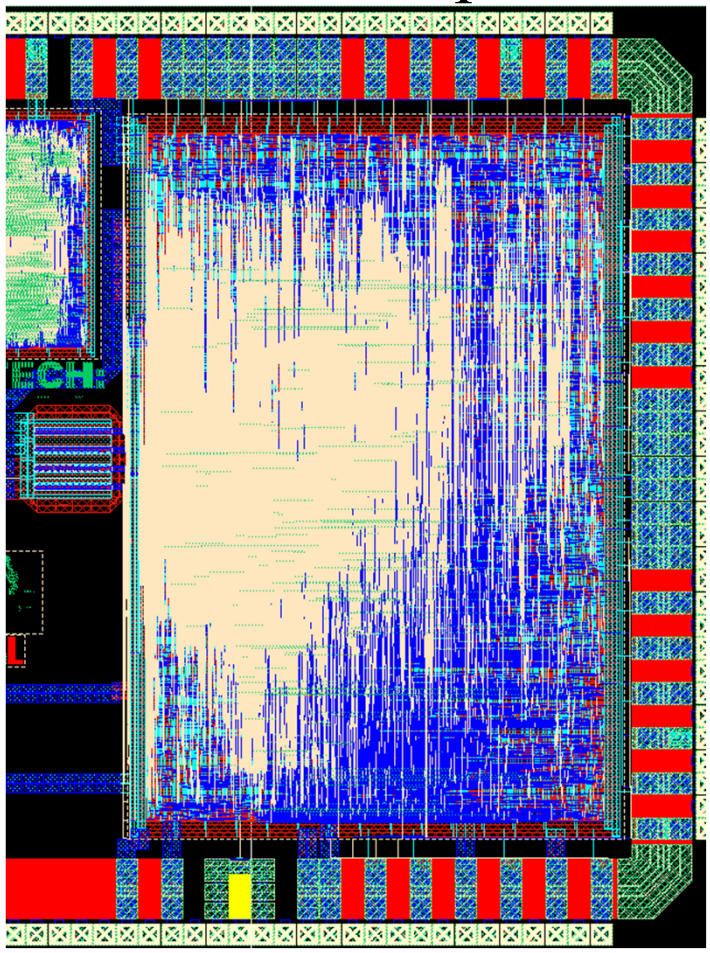
SRAM cell

The design example of stochastic ADC. The SRAM array is used as 64 x 64 comparator array. The circuit is synthesizable, because it can be composed of digital circuit.



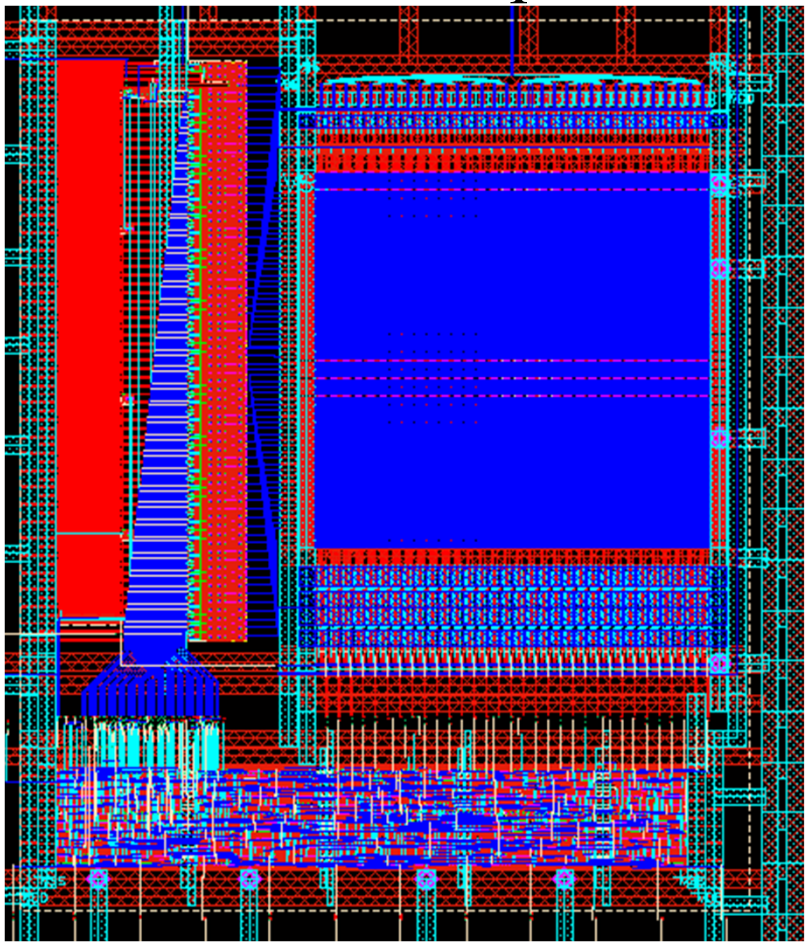
Design example of 2 step stochastic ADC

4-inverter-comparators



CMOS 65nm, 1930 um x 1315 um

6T-SRAM-comparators



CMOS 180nm, 525 um x 430 um