6. Layout design

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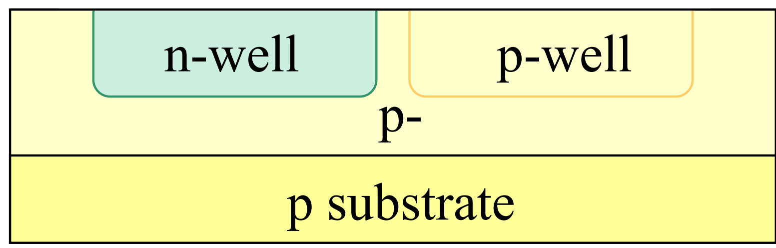
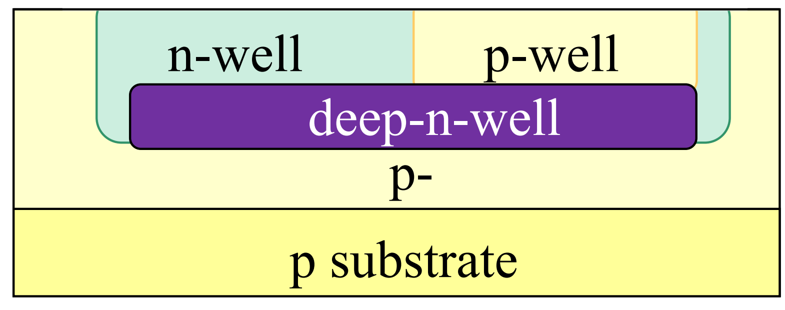
6.1 Structures and design rules

Well structures



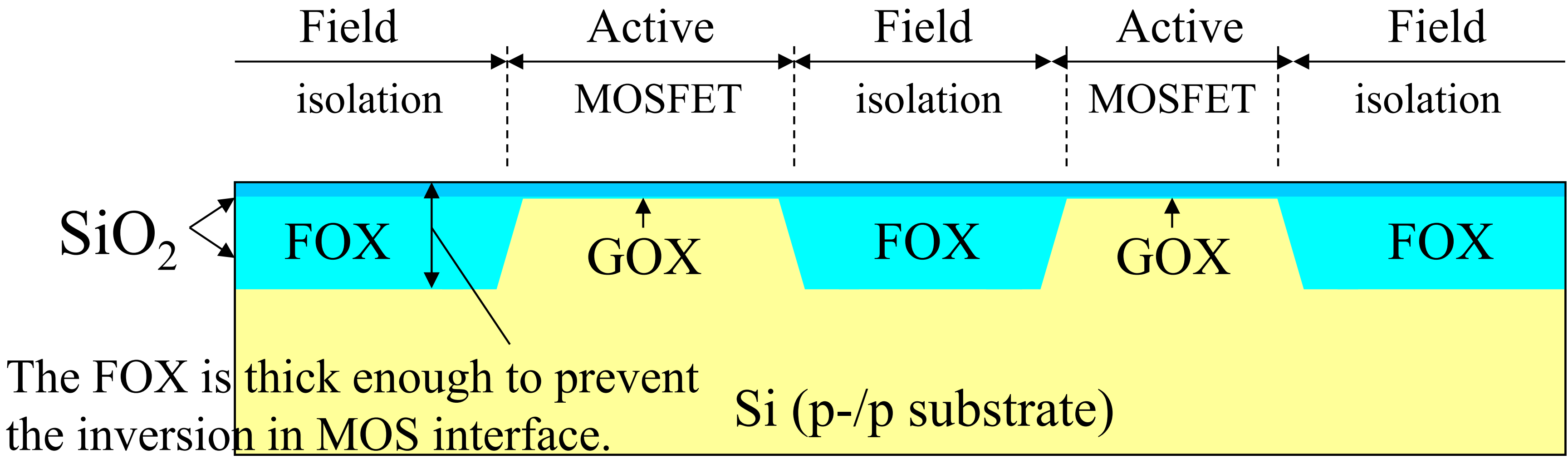
Twin-well process
(The impurity concentration in the well is optimized, but p-wells are not electrically isolated.)



Triple-well process
(The n-wells and the p-wells are electrically isolated each other.)

Isolation structure

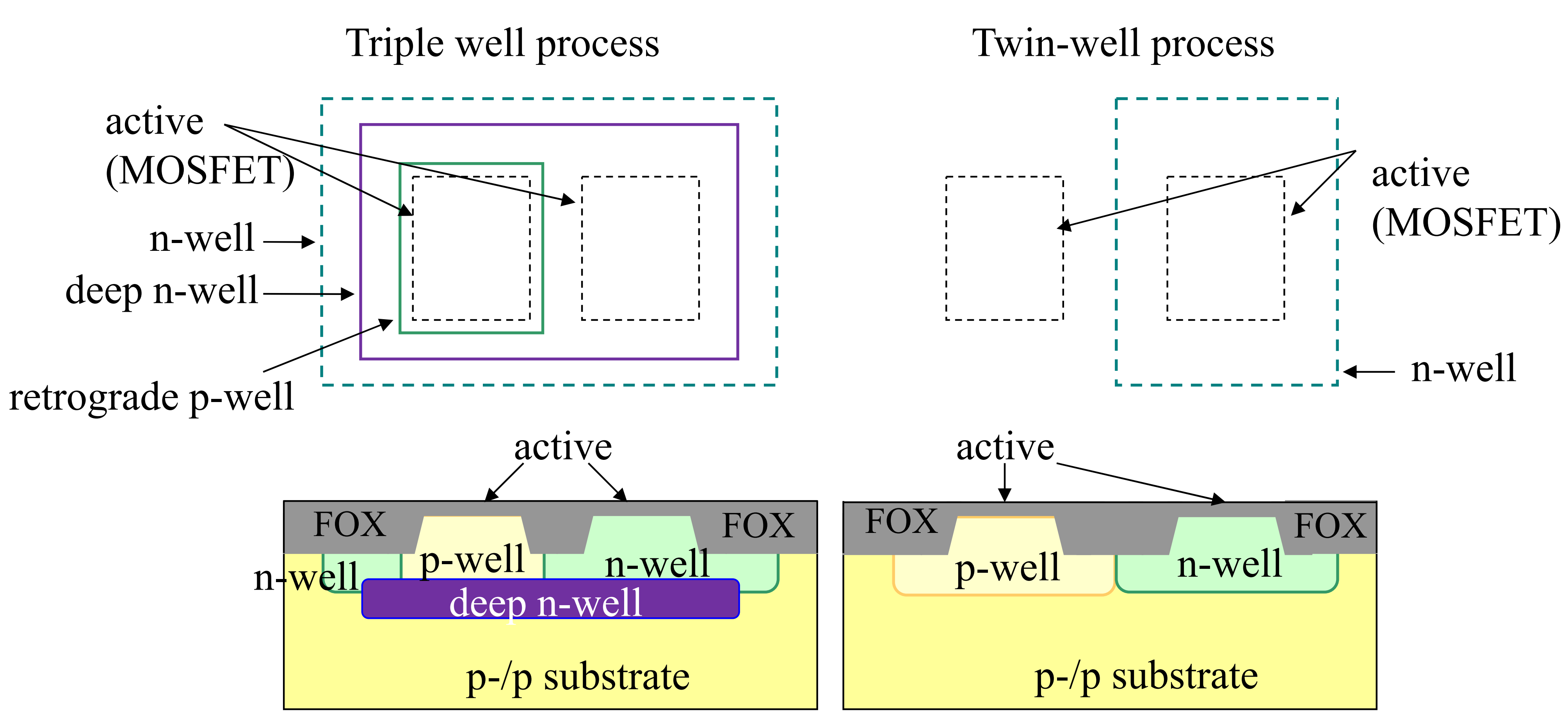
Shallow trench isolation (STI)



FOX: Field Oxide (Thickness = 100nm)
GOX: Gate Oxide (Thickness = several nm)

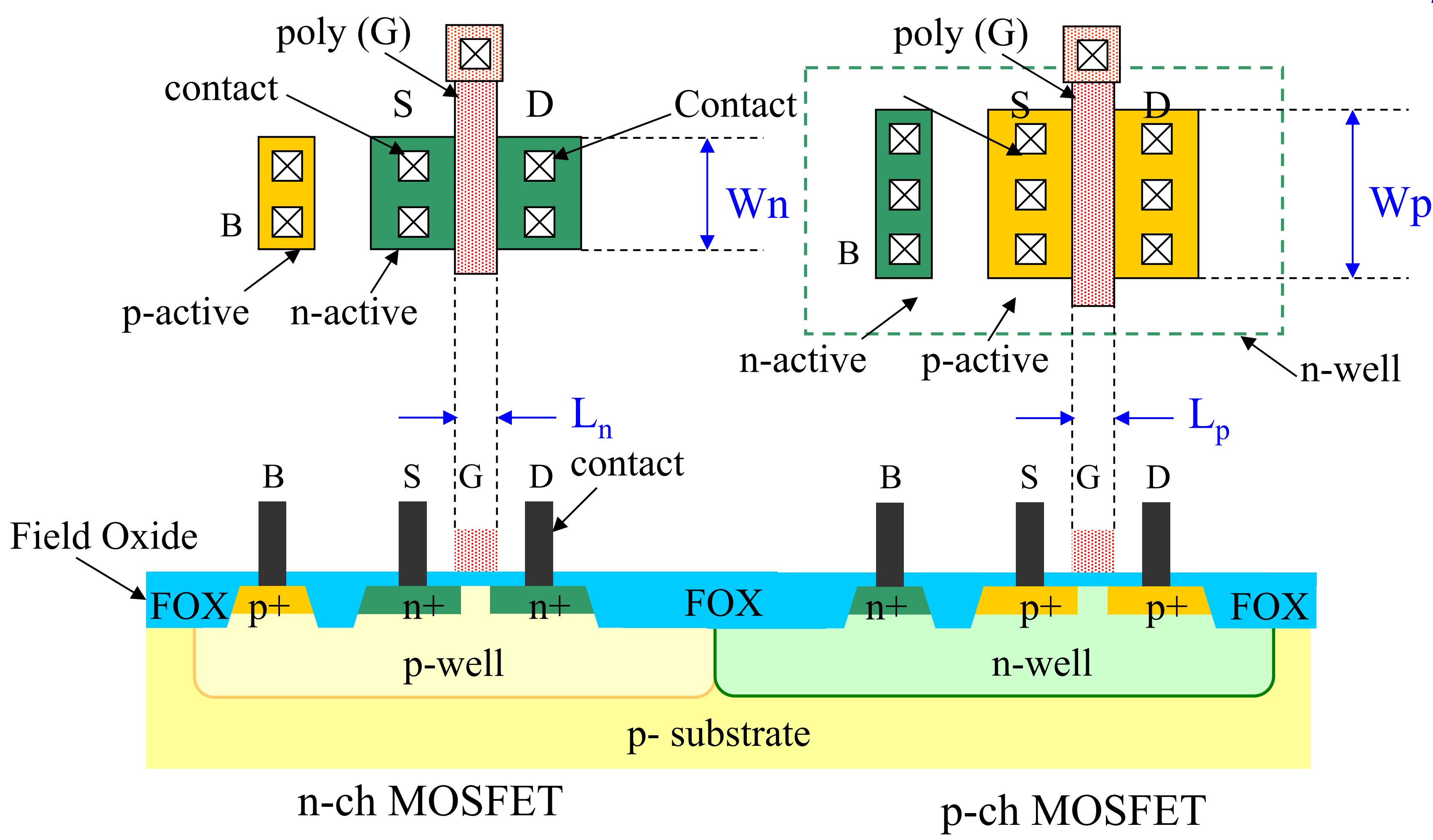
NOTE: FOX is built by the shallow trench isolation (STI) process. Therefore, it also be written as STI.

Layout design of well and active area

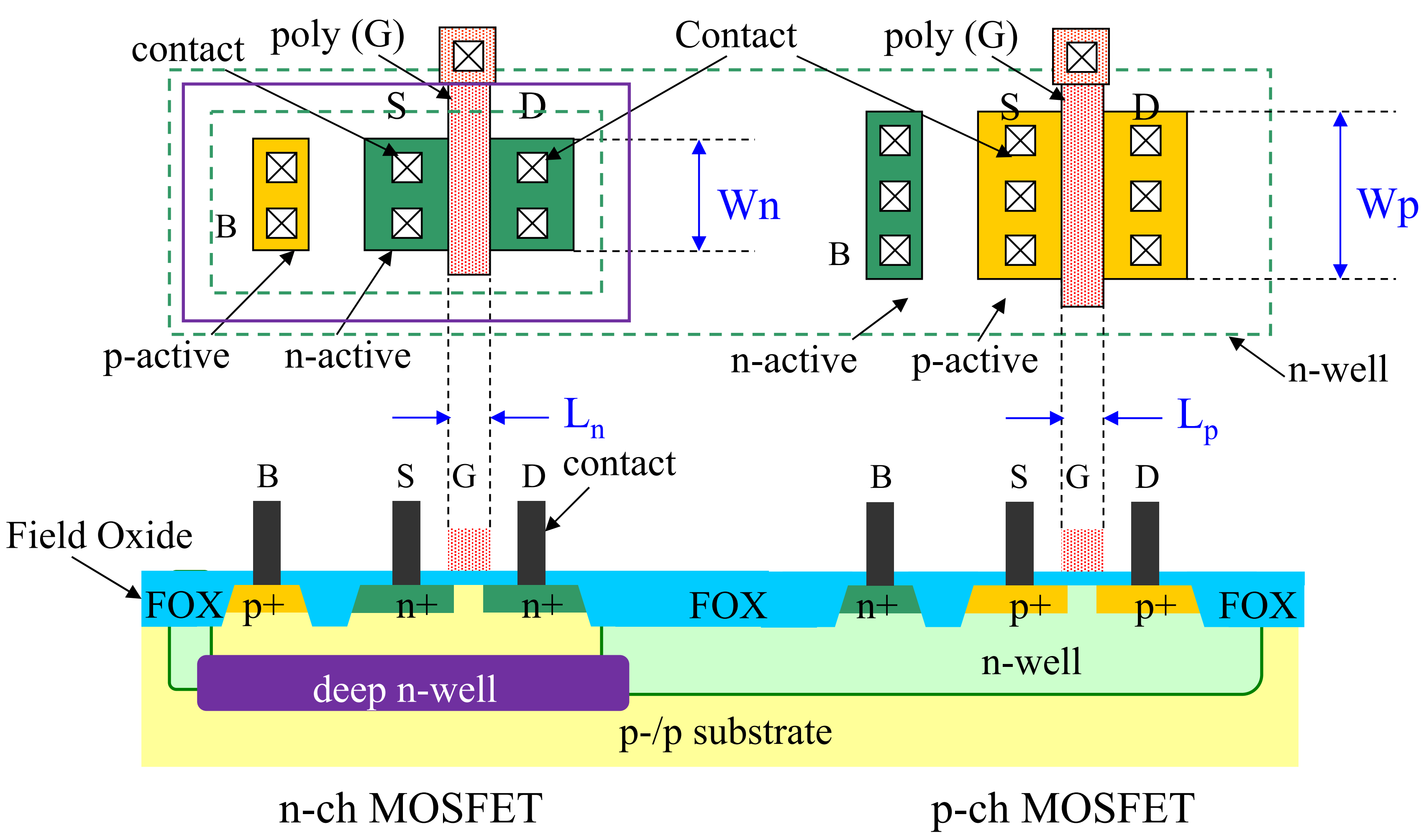


Layout of MOSFET (Twin well)

The electrical characteristics of MOSFET are dominantly depends on $\frac{W_n}{L_n}$ *and* $\frac{W_p}{L_p}$.

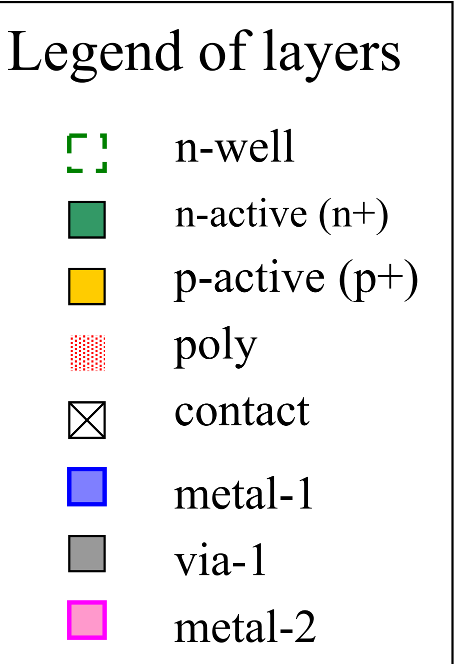


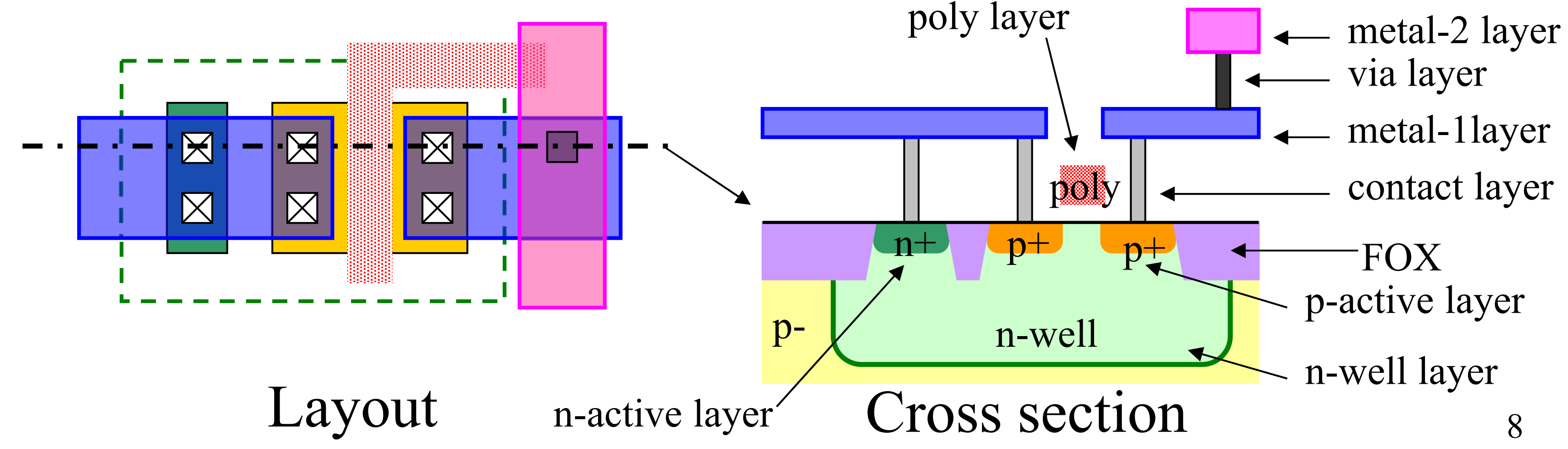
Layout and MOSFET (Triple well)



Layers

- Layer numbers are assigned to Well, Active, Poly, Contact, Metal, Via, Silicide block, and Dummy, respectively.
- Some layer is automatically generated from the patterns in the drawn layers.
  - ex. FOX and GOX is generated from the pattern of the active layer.





Design Rules

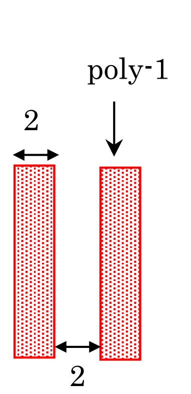
- A semiconductor foundry allows the designers to design only the layout pattern on the top view.
  - The thickness of layers are fixed by the semiconductor foundry.
- The designers have to follow the design rules prescribed for the technology. The purpose of design rule is as follows.
  - Warranty of dimensional precision in micro or nano fabrication
  - Warranty of precision on electrical characteristics
  - Prevention of latch-up(NOTE) triggered by parasitic bipolar-transistors
- Design rule violation is automatically detected and reported in DRC (Design Rule Check).
- A semiconductor company accepts only the design that is passed the specified design rules.

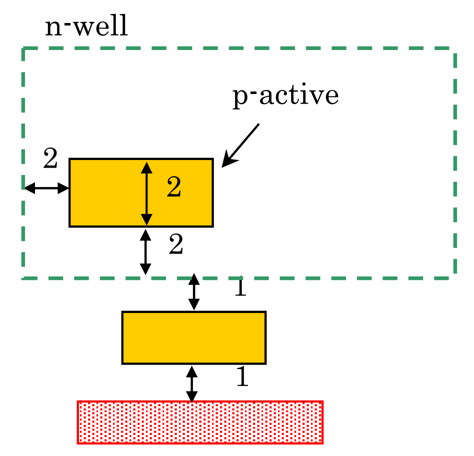
NOTE: Latch-up

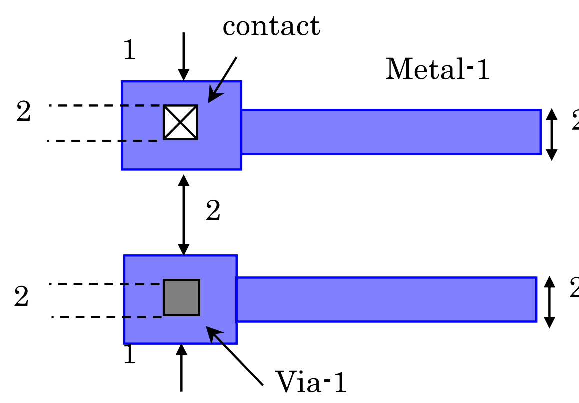
The inadvertent creation of a low-impedance path between the power supply rails of a CMOS circuit, triggering a parasitic pnpn or npnp structure.

Example of design rules (1)

Geometry Rules







poly rule
min. width = 2
min. spacing 2

active (p+, n+) rule
min. width = 2
min. spacing to well = 2 (inside)
min. spacing to well = 1 (outside)
min. spacing to poly = 1

metal-1 rule
min. width = 2
min. spacing = 2
min. extension beyond contact = 1
min. extension beyond via-1 = 1

Example of design rules (2)

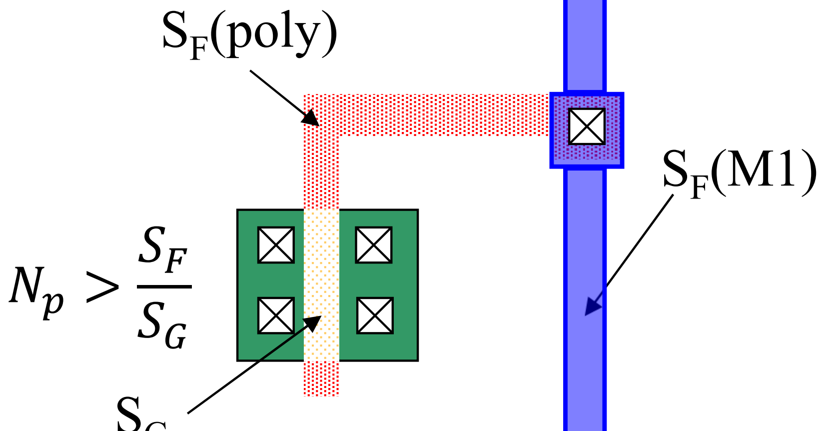
Minimum Density Rules

Fine featured processes utilize CMP (Chemical-Mechanical Polishing) to achieve planarity. Effective CMP requires that the variations in feature density on a layer be restricted.

Antenna Rules

(Process-Induced Damage Rules)

The "Antenna Rules" deal with process induced gate oxide damage caused when exposed poly-silicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide. The rules require that the area of the poly-silicon and metal over field oxide divided by the area of the transistor gate (thin oxide area) must be less than Np (where Np is a limit that depends on the process and on design targets).



Verifications of the layout design

- **DRC (Design Rule Check)**
  - Detection of the design rule violation
- **ERC (Electrical Rule Check)**
  - Detection of the open/short error
- **LVS (Layout VS Schematic)**
  - Equivalence checking between layout and schematic

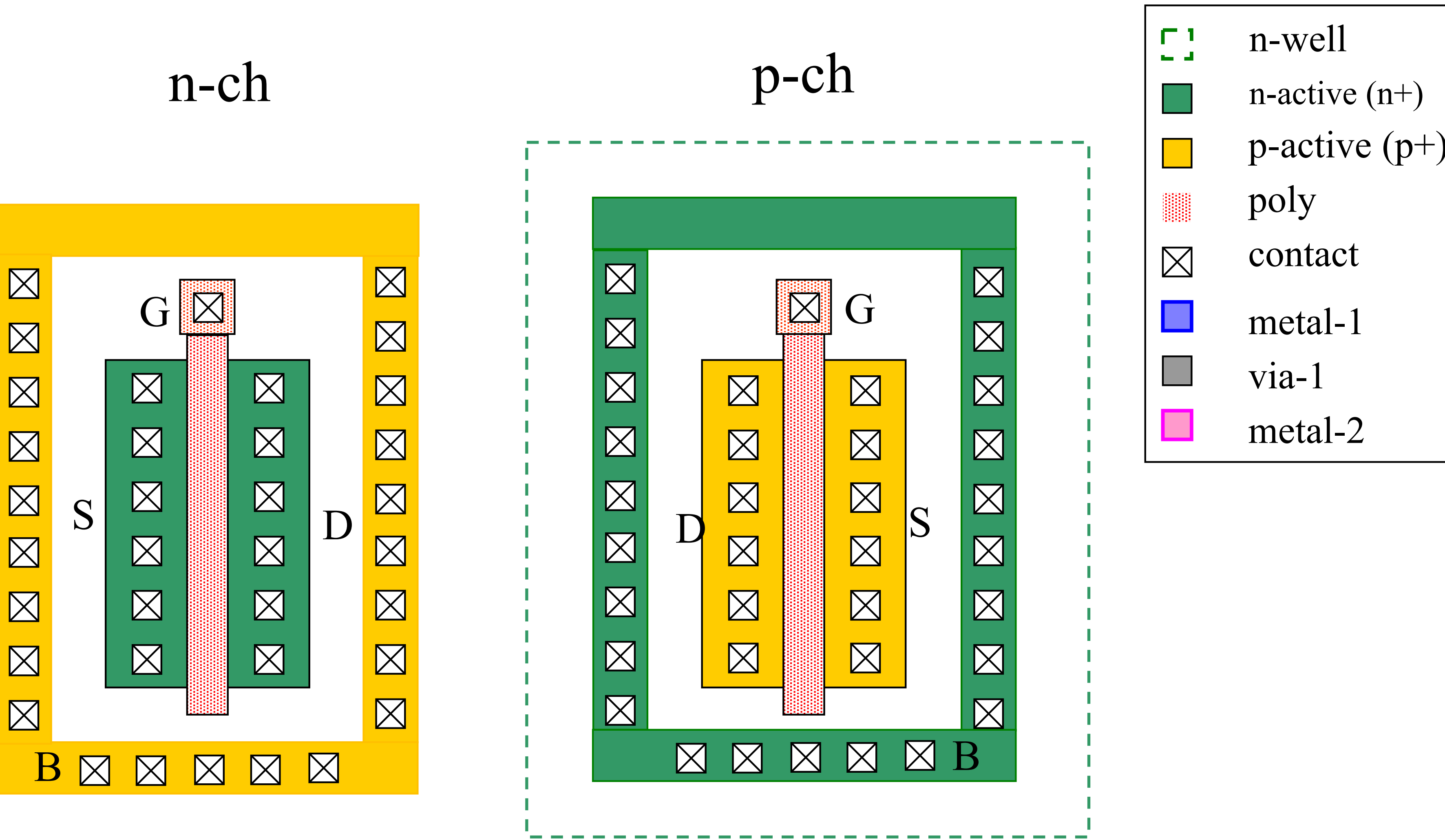
The layout design checker has a batch processing mode and interactive mode.

Influence on circuit performance of the layout

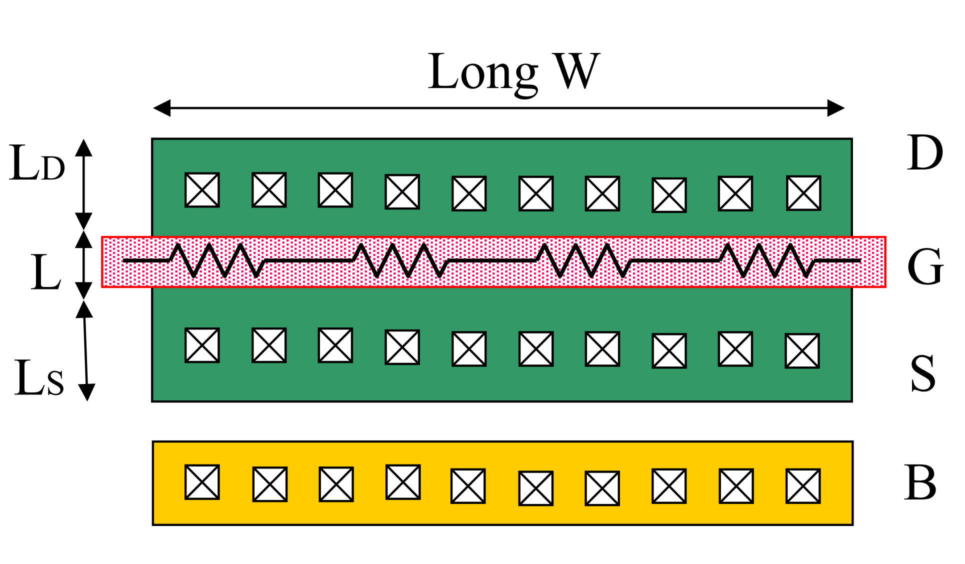
- Frequency response in high-frequency region
  - The parasitic resistance and the parasitic capacitance raise an unintended pole and zero.
  - The long interconnect acts as a parasitic inductor or LC resonator.
- Precision of the circuit operation
  - Common centroid layout of MOSFET, C, and R can improve the production tolerance and mismatch.
  - Symmetric layout of interconnect can improves the production tolerance and skew of the digital signal (delay) and analog signal (phase lag).
- Noise and jitter characteristics
  - The parasitic resistance, especially poly-Si, act as a thermal noise source.
  - The parallel placement of interconnect raise a crosstalk of signals.

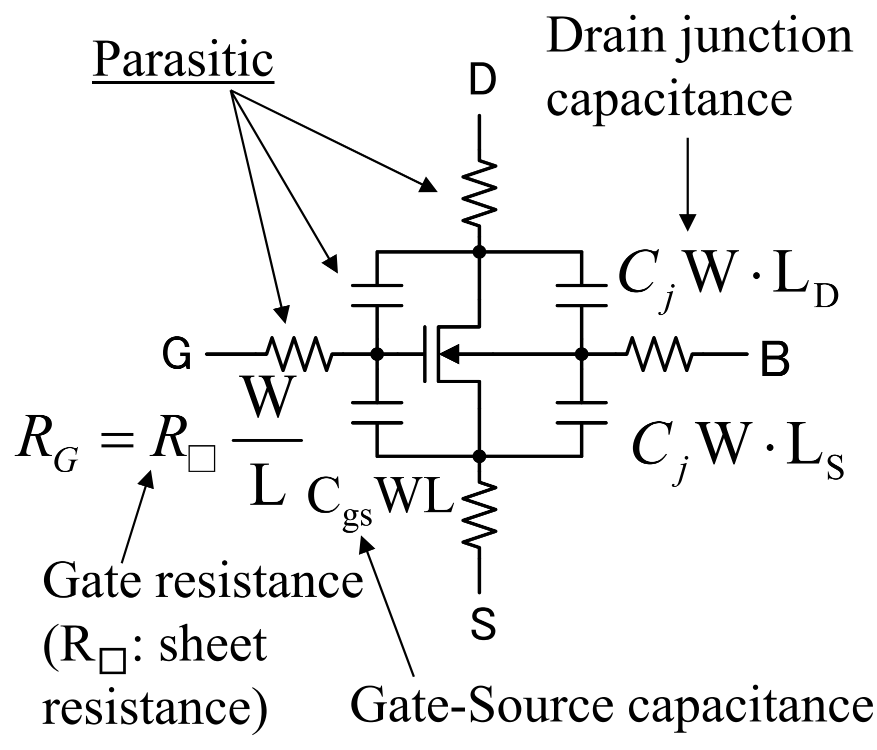
6.2 Layout of the MOSFET

Layout sample of MOSFET



Parasitic of MOSFET





- Long W: large time constant of gate poly-Si
- Long W: large thermal noise of gate poly-Si
- Long LD, LS: large parasitic capacitance and resistance of drain/source area
- Few number of contact: Shift or fluctuation of substrate potential

How can you design the MOSFET with larger W?

Fingered MOSFET

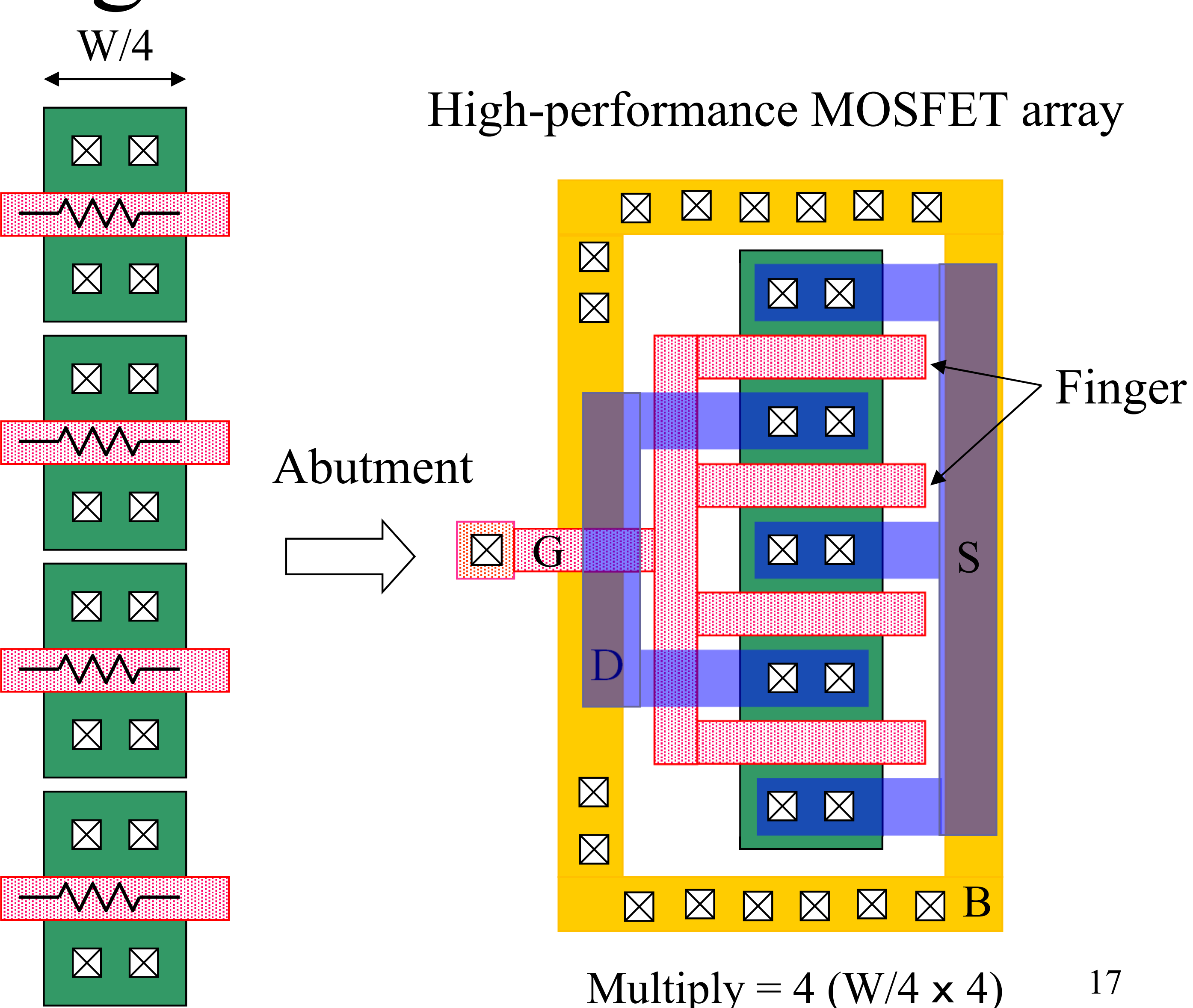
MOFET should be sectioned to reduce the gate resistance.

$$R_{\square} \frac{W}{L} << \frac{1}{g_m}$$

g_m: trans-conductance

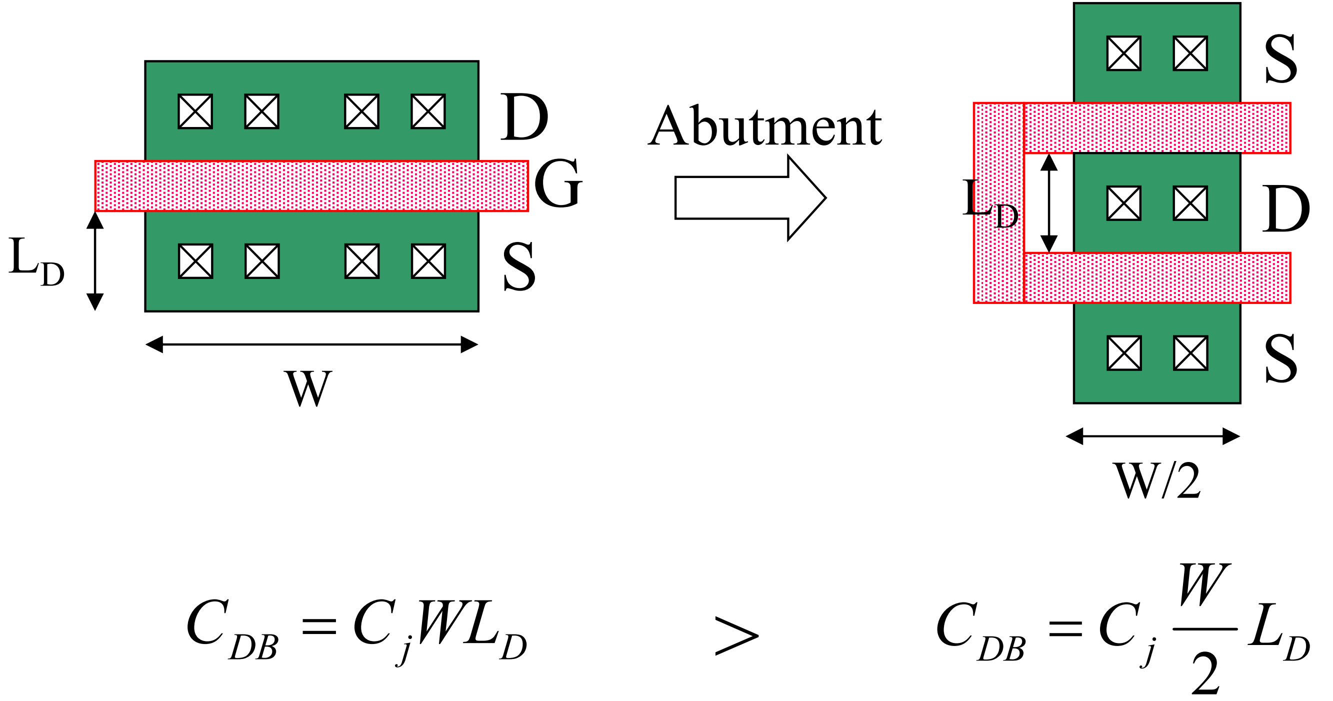
$$g_m = y_{21} = \frac{dI_{ds}}{dV_{gs}}$$

This condition is often met in the case of W/L < 20.
W/L < 10 is recommended.



Multiply = 4 (W/4 x 4)

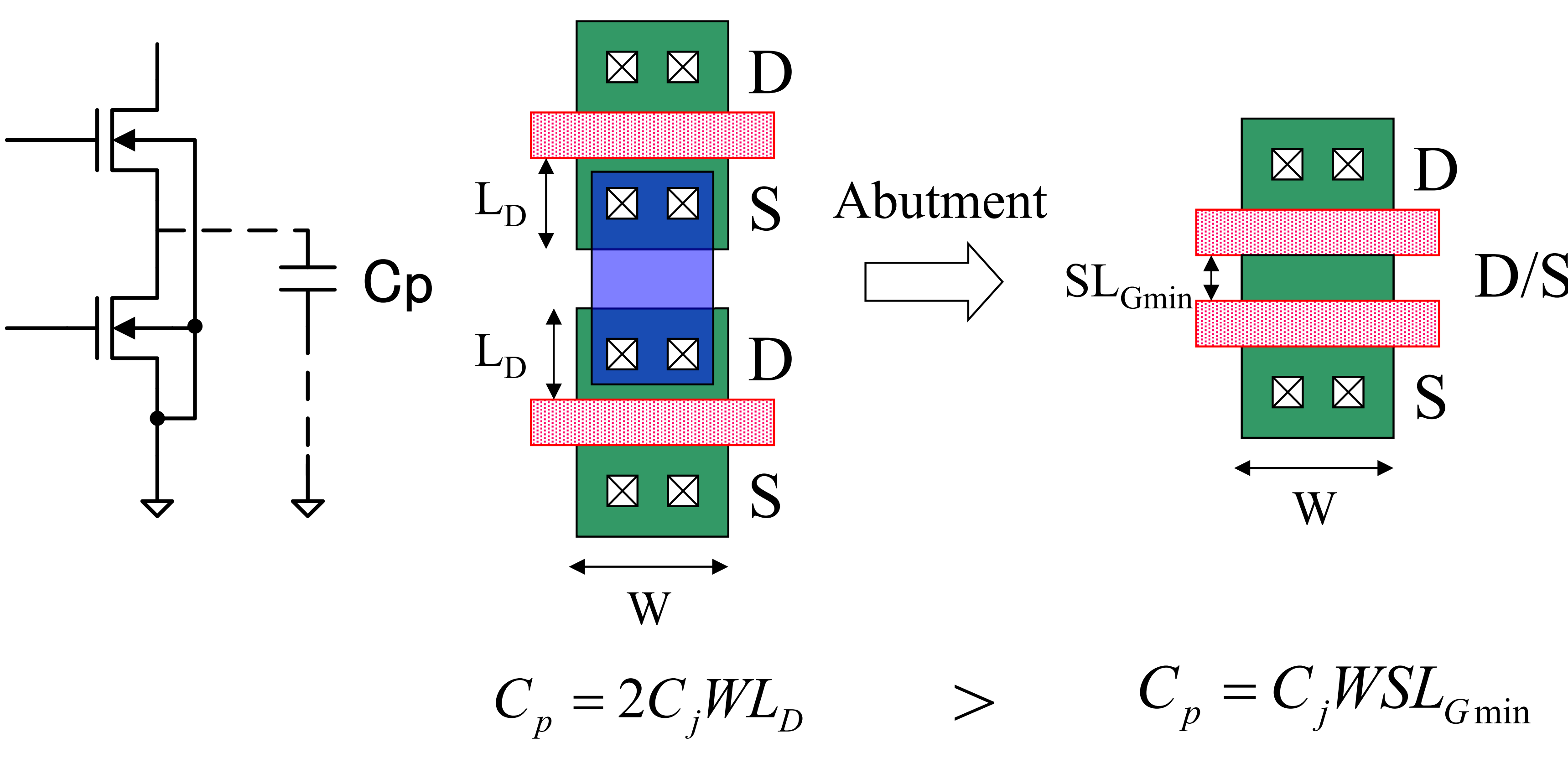
Reduction of the drain junction capacitance (single MOSFET)



$$C_{DB} = C_j W L_D \quad > \quad C_{DB} = C_j \frac{W}{2} L_D$$

C_j = Capacitance of drain bottom pn junction per area (F/m²)

Reduction of the drain junction capacitance (series MOSFET)



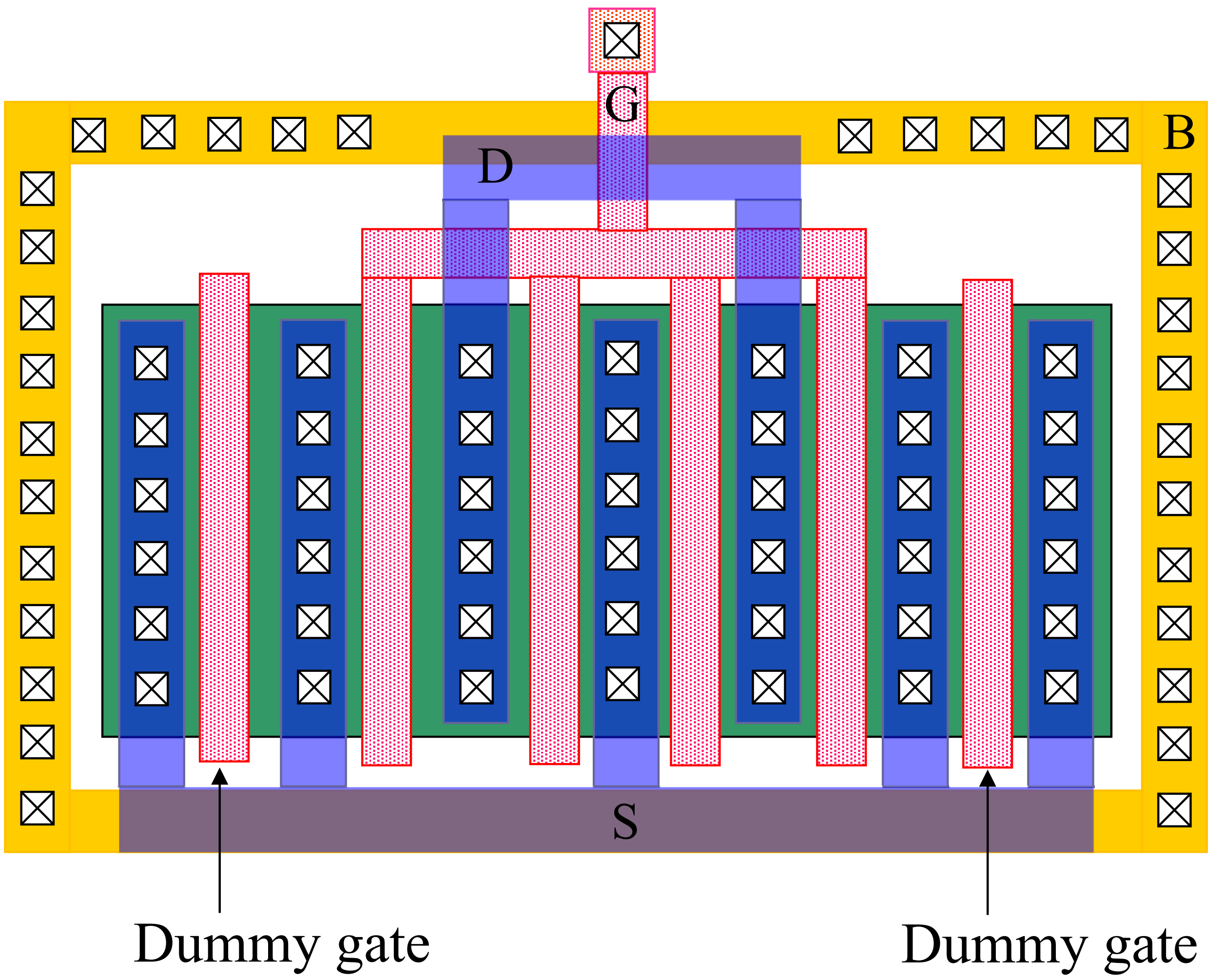
$$C_p = 2C_j W L_D \quad > \quad C_p = C_j W SL_{G\min}$$

C_j = Capacitance of drain bottom pn junction per area (F/m²)

SL_{Gmin} = minimum gate spacing

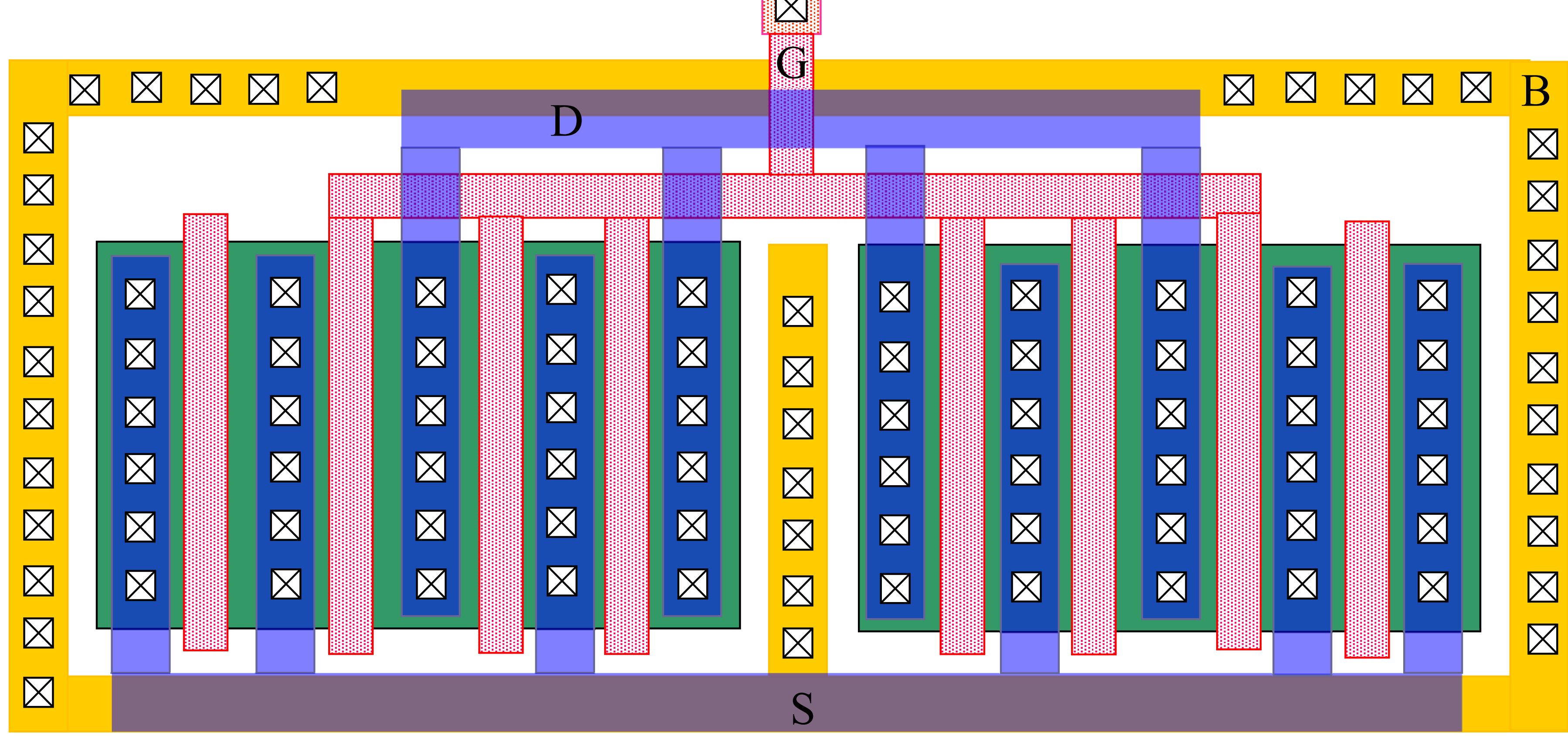
Dummy gate

The dummy pattern may be formed to reduce the production tolerance.



Interdigitated body contact

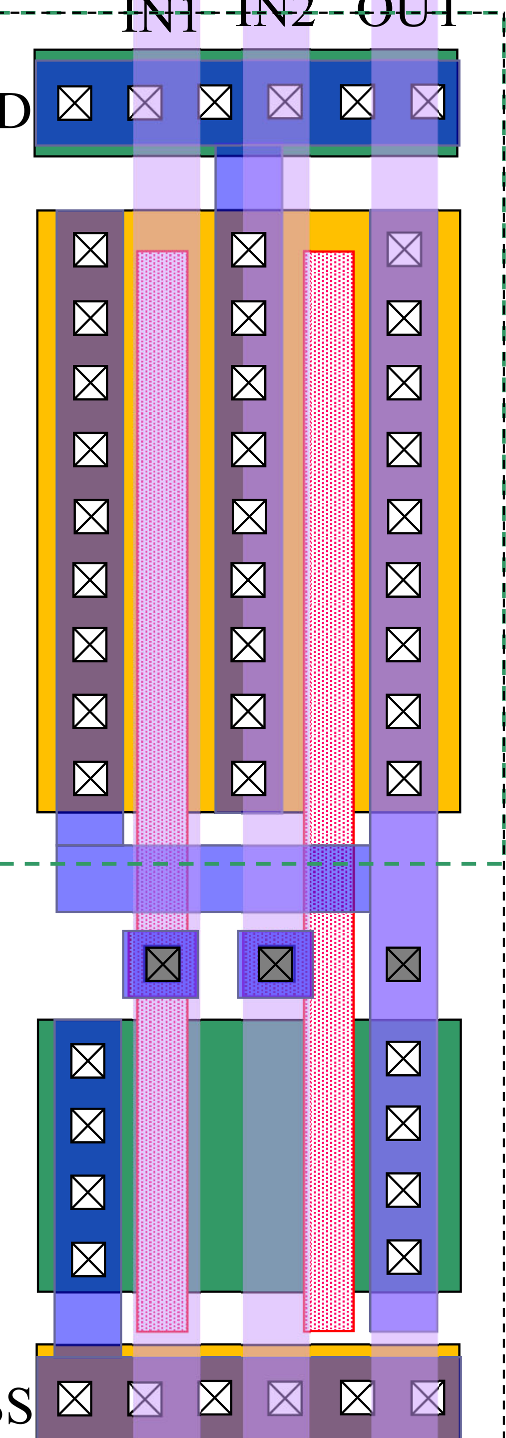
The body/well contact may be added to immobilize the substrate/well potential in the very large MOSFET.



Example of logic gate

- High area utilization
- Constant height of all cell
- Horizontal runs of metal are used to supply power (Rail), and vertical runs of metal (or poly) are used to input and to output the signals.

Outline box of the cell



poly-1

n-well

n+

Metal-1

p+

Metal-2

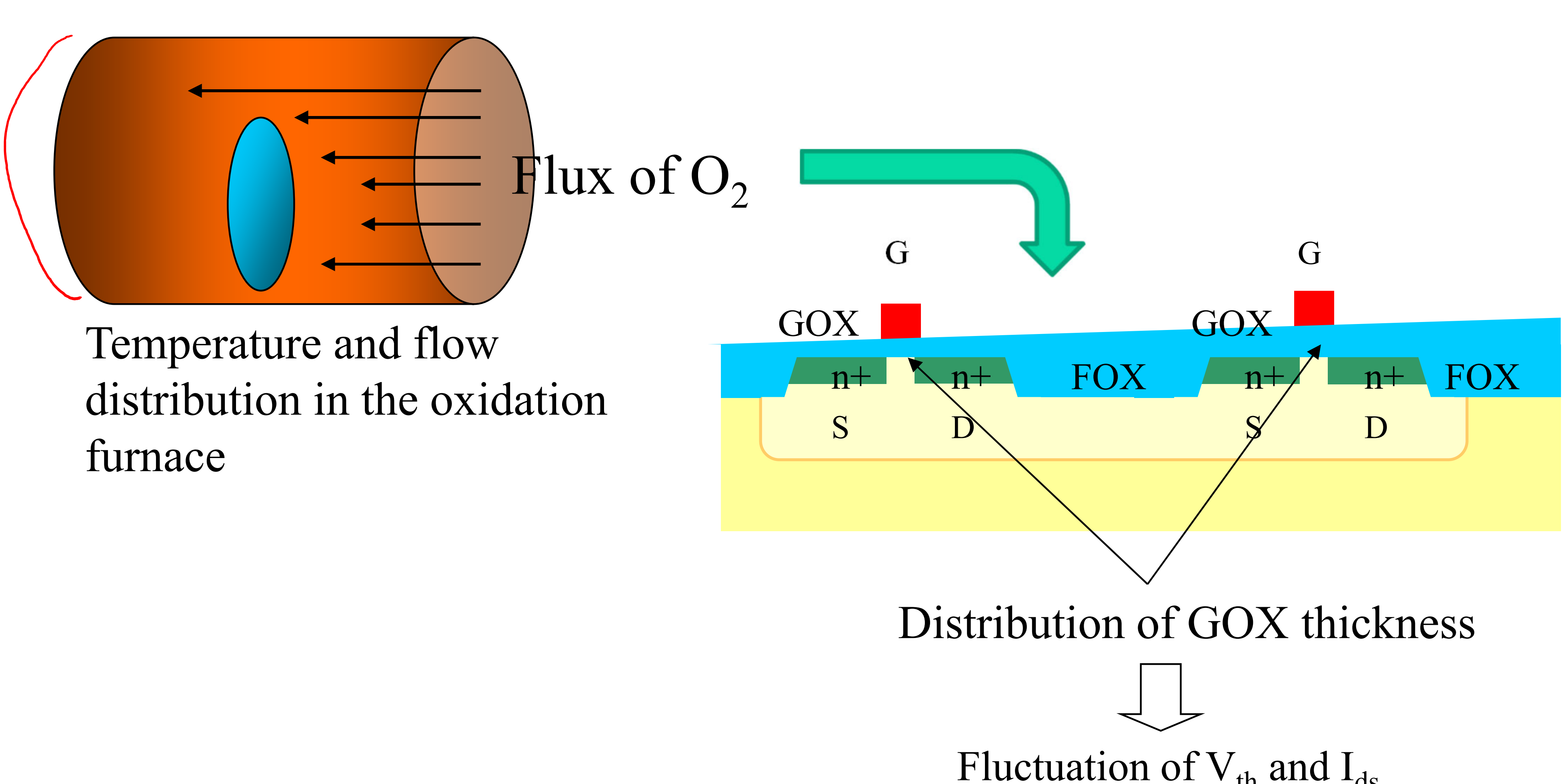
Contact

Via-1

Matching layout

- Matching layout is used to enhances the relative precision of device pair (e.g. a differential pair, a current mirror). (around ±1%)
  - Use of The repeat of warp of the fundamental unit
    - The devices of the different shape and direction match very poorly.
  - Use of the dummy pattern
  - Use of the common centroid pattern
- Trimming is necessary if you expect more precise matching.(less than ±0.1%)

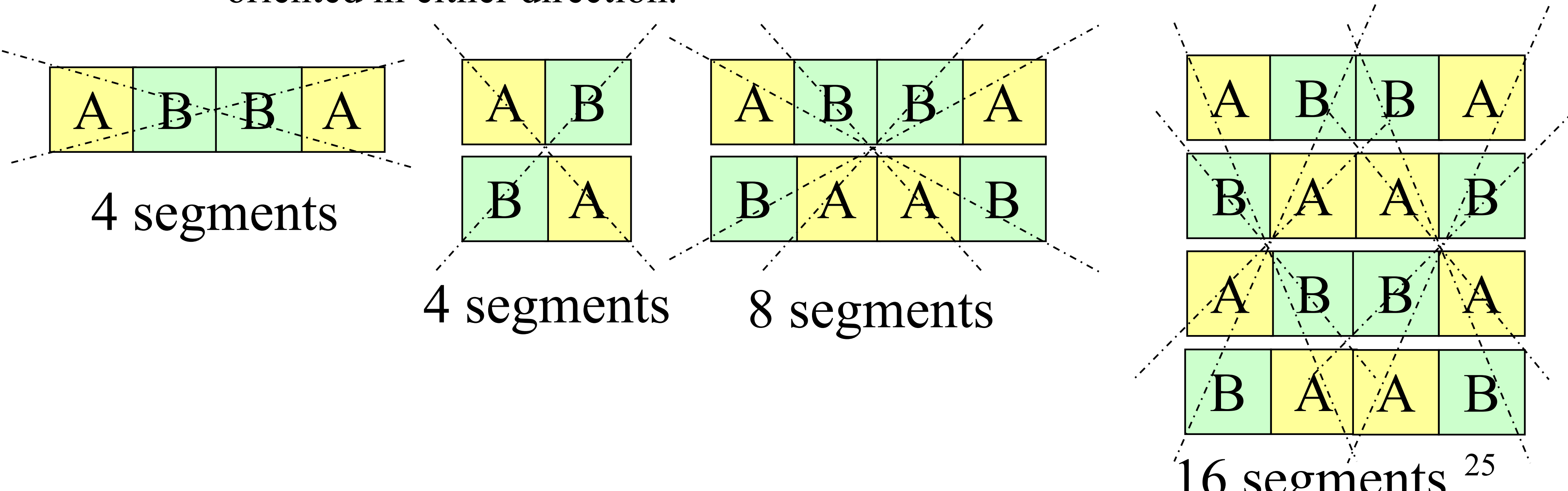
Distribution of GOX thickness



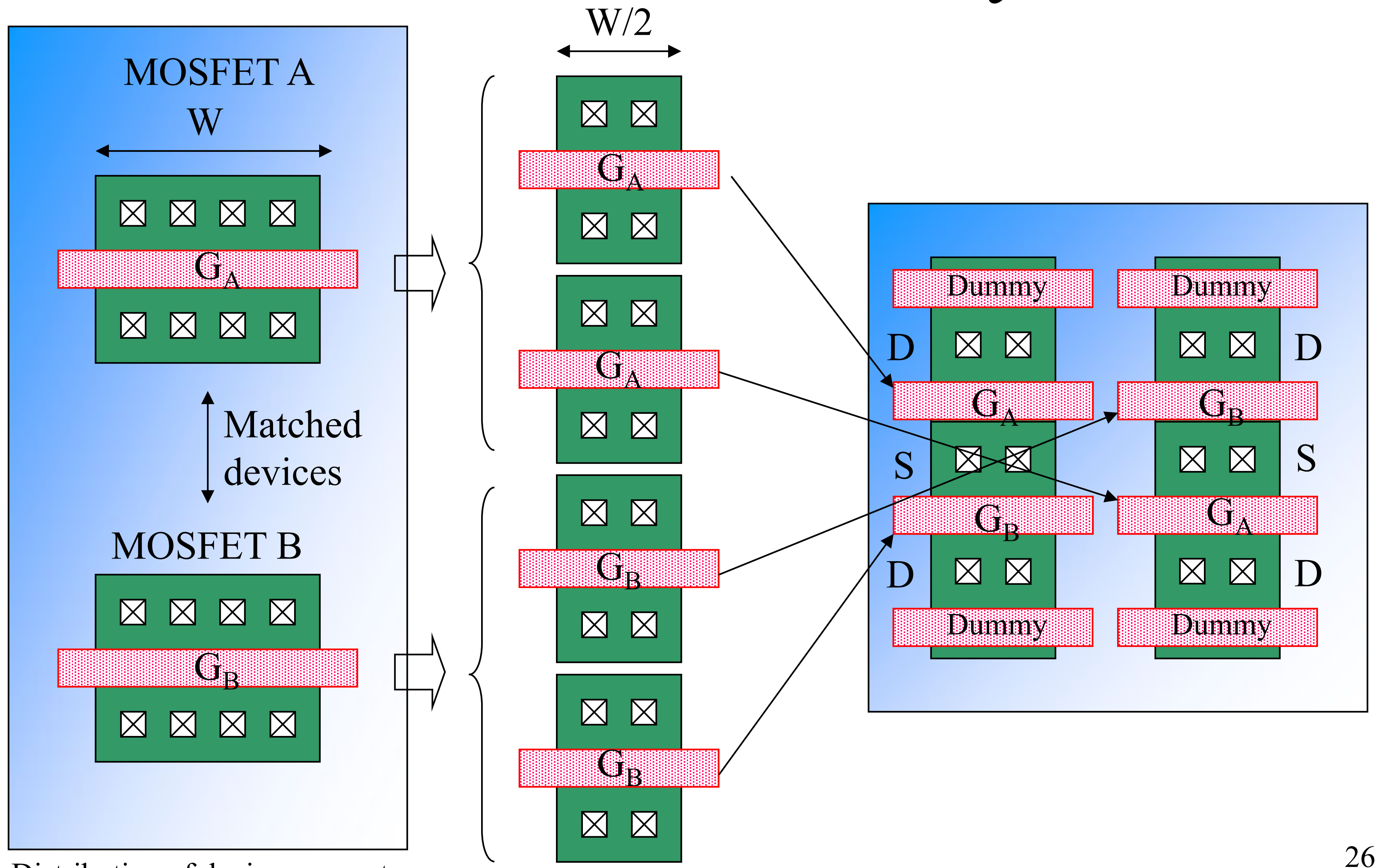
Common centroid layout

- The mismatch of the device characteristics is canceled using the common centroid layout.

1. The centroid of the matched devices should be coincident.
2. The array should be symmetric around both the x and y-axis.
3. Each matched device should consist of an equal number of segments oriented in either direction.

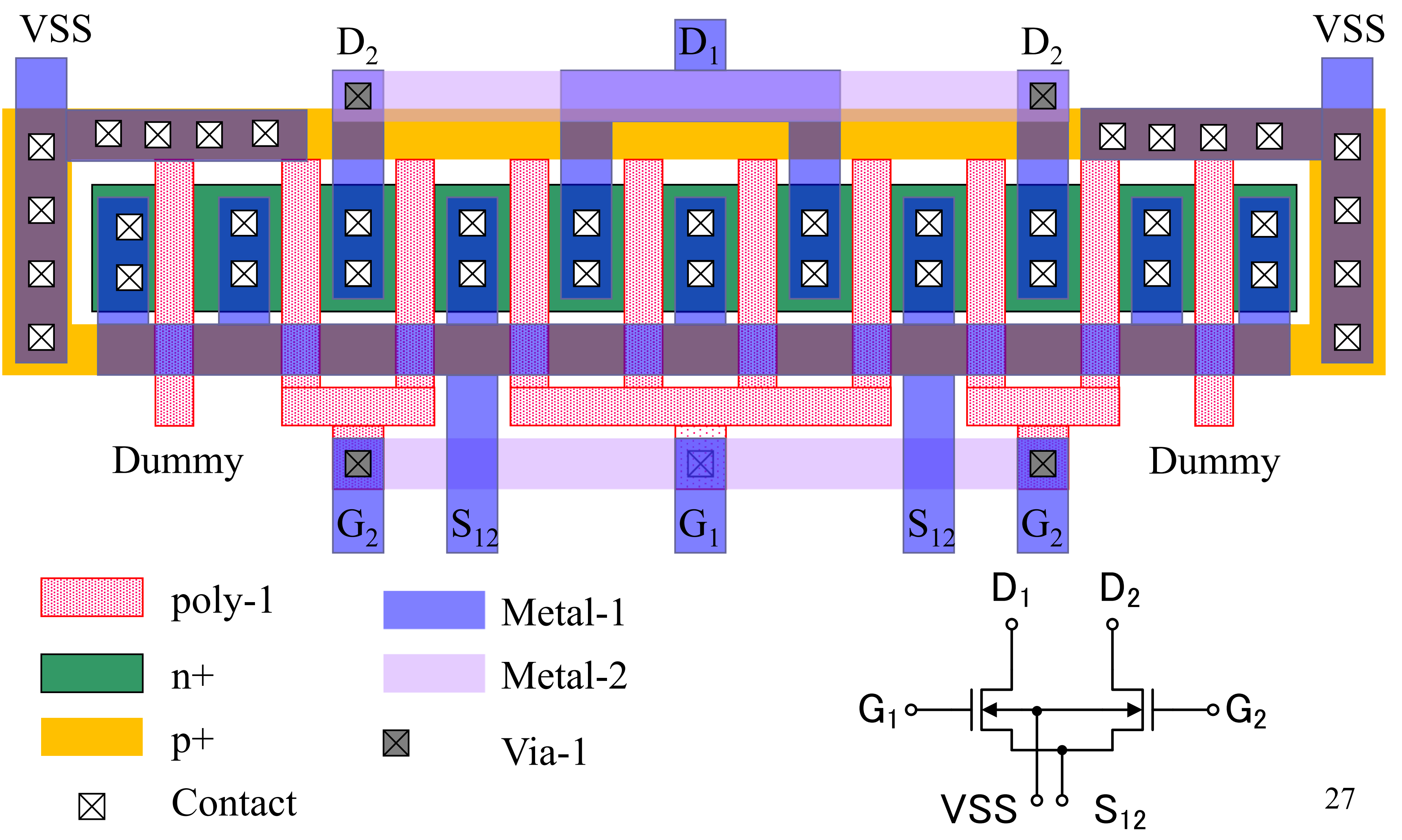


Segmentation and Placement for common centroid layout



Distribution of device parameter

Layout sample of a differential pair



6.3 Layout of the passive devices

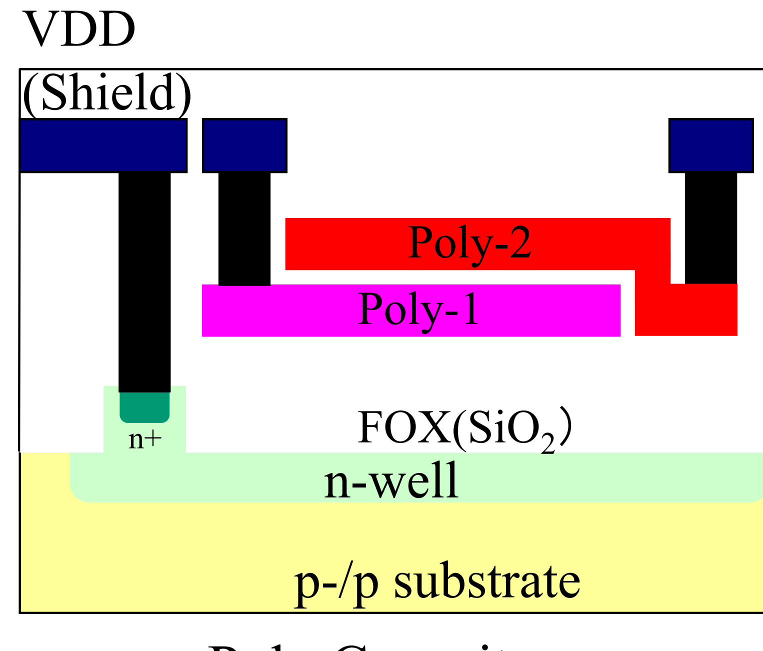
Example of the characteristics of the passive device

Component	Values	Mismatch	Temp. Coefficient	Volt. Coefficient
MOS Cap.	2.2 – 2.7 fF/μm^2	0.05%	50 ppm/°C	50 ppm/V
Poly2/Poly1 Cap.	0.8 – 1.0 fF/μm^2	0.05%	50 ppm/°C	50 ppm/V
p+ Resister	80 – 150 Ω/☐	0.4%	1500 ppm/°C	200 ppm/V
p+ diff. Resistor	50 – 80 Ω/☐	0.4%	1500 ppm/°C	200 ppm/V
Poly Resistor	20 – 40 Ω/☐	0.4%	1500 ppm/°C	100 ppm/V
N-well Resister	1 k– 2k Ω/☐	1%	8000 ppm/°C	10k ppm/V

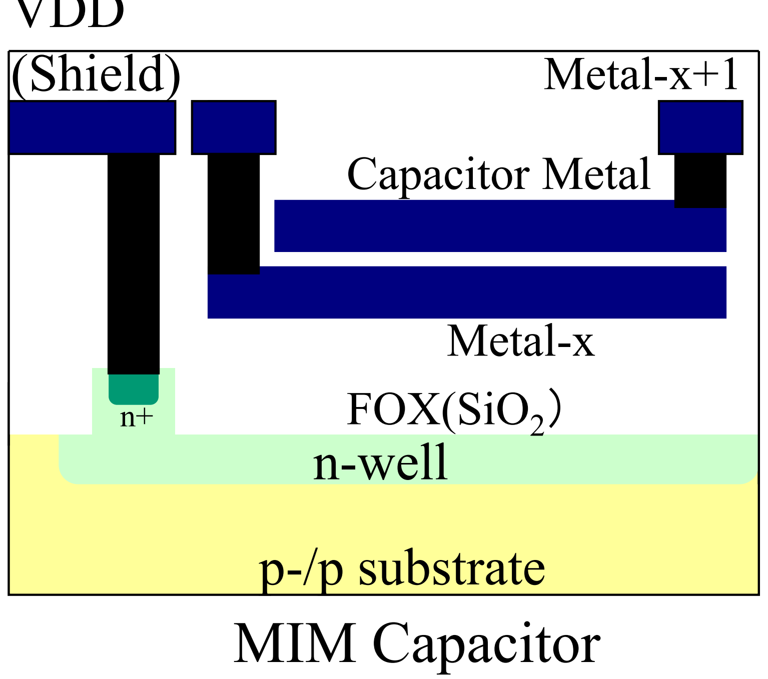
The mismatch error of the passive devices on a chip is very small.

Structure of capacitors

- Poly Capacitor (Before 0.25μm CMOS process)
- MIM Capacitor (After 0.18μm CMOS process)

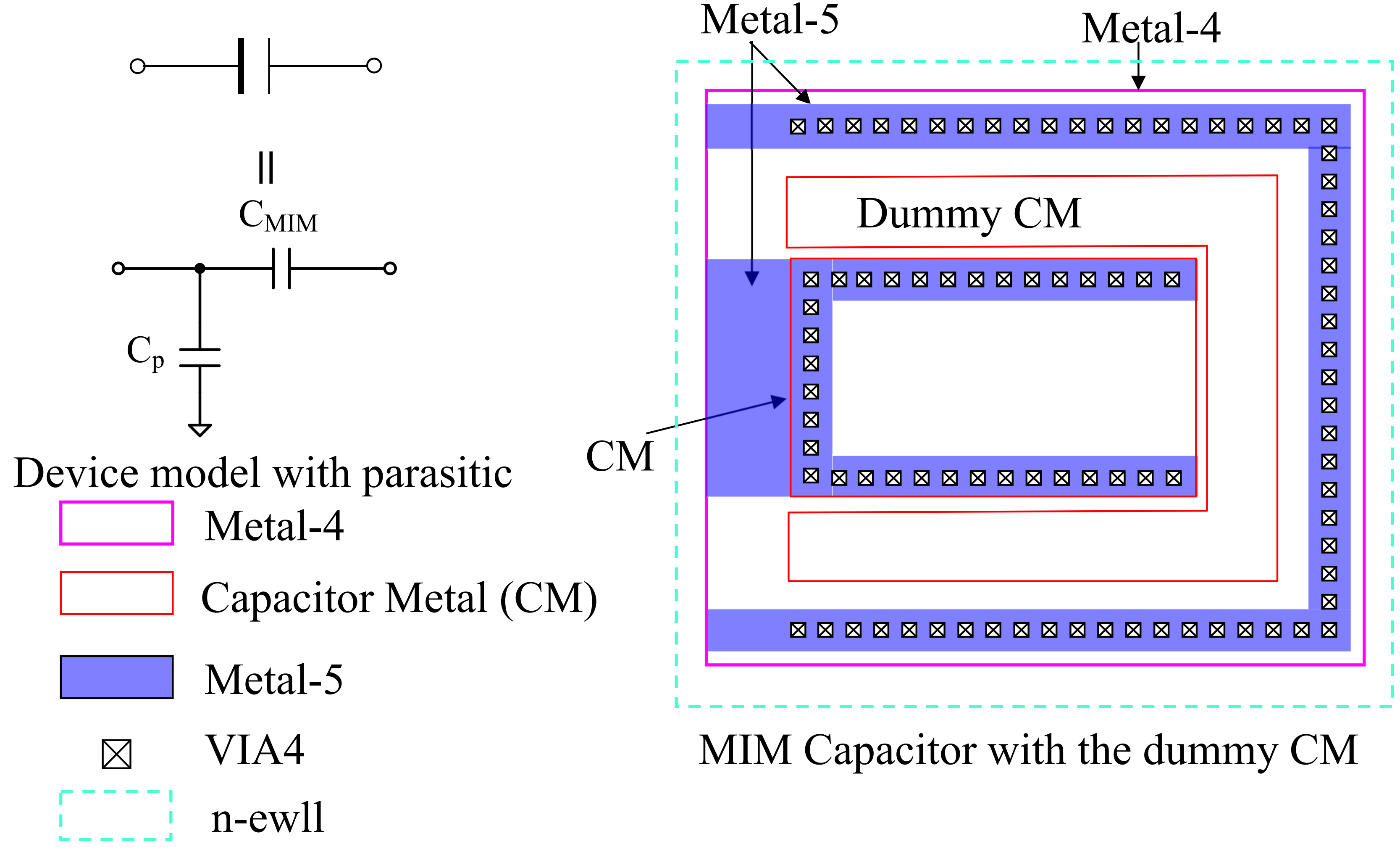


Poly Capacitor



MIM Capacitor

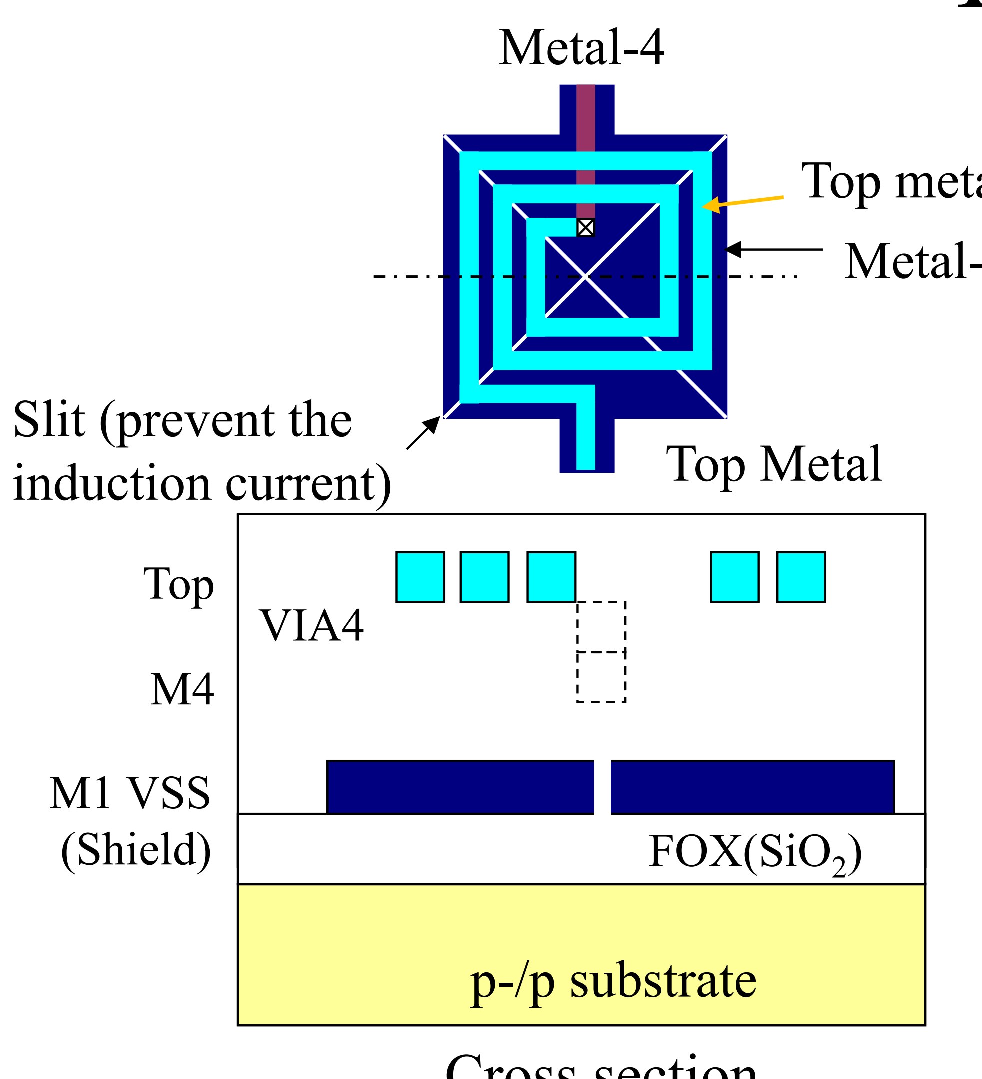
Layout sample of a MIM capacitor



MIM Capacitor with the dummy CM

The dummy metal is automatically inserted, if the dummy is not specify.
The dummy metal may work as a parasitic capacitance.

Structure of spiral inductor



Cross section

C_P

L R_S

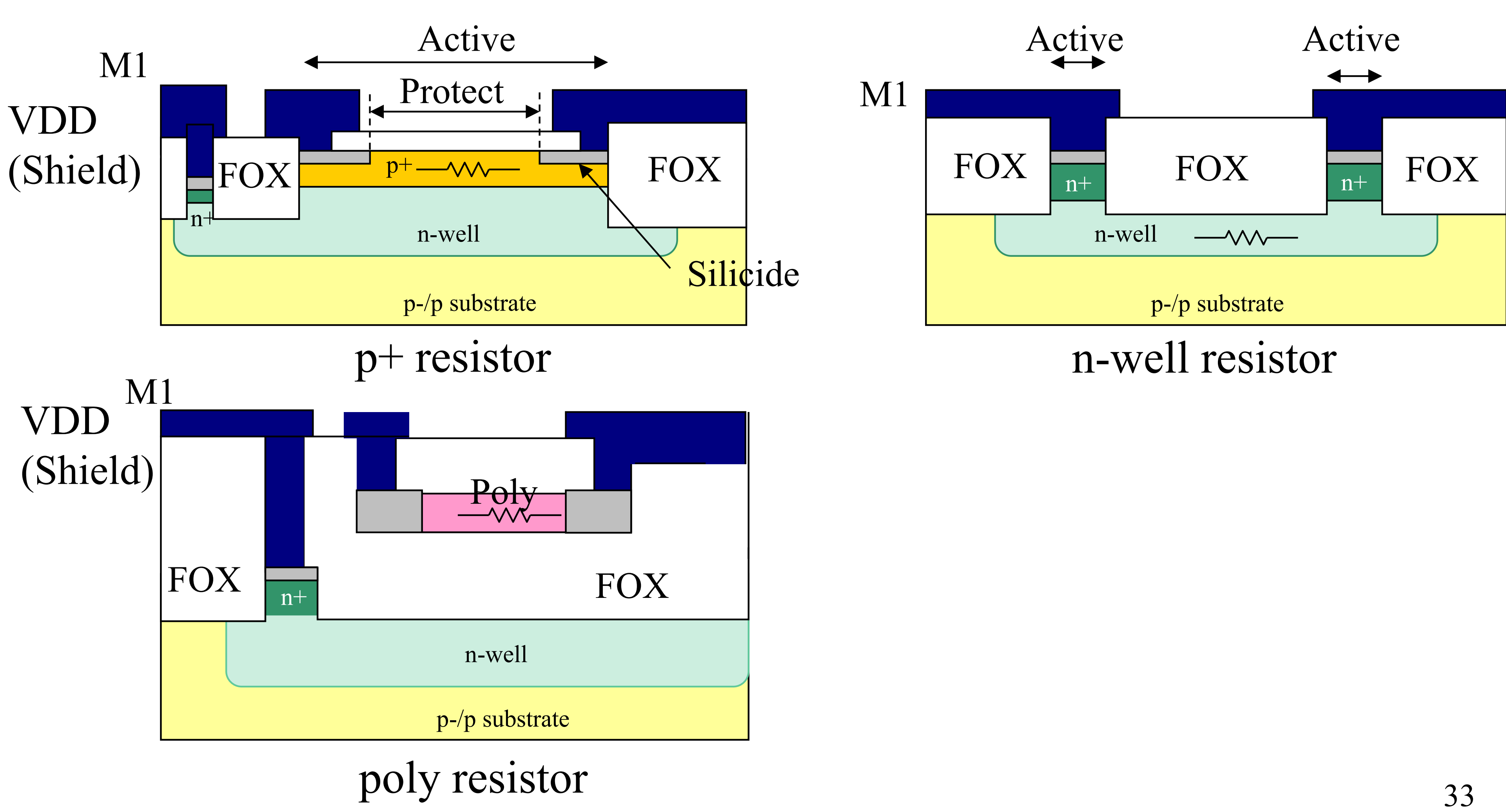
C_F C_F

Equivalent circuit with the parasitic

Top metal or dedicated layer for inductor is used.

The inductor is dissipative in the chip area.

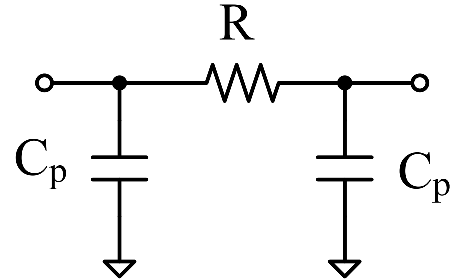
Structure of the resistance



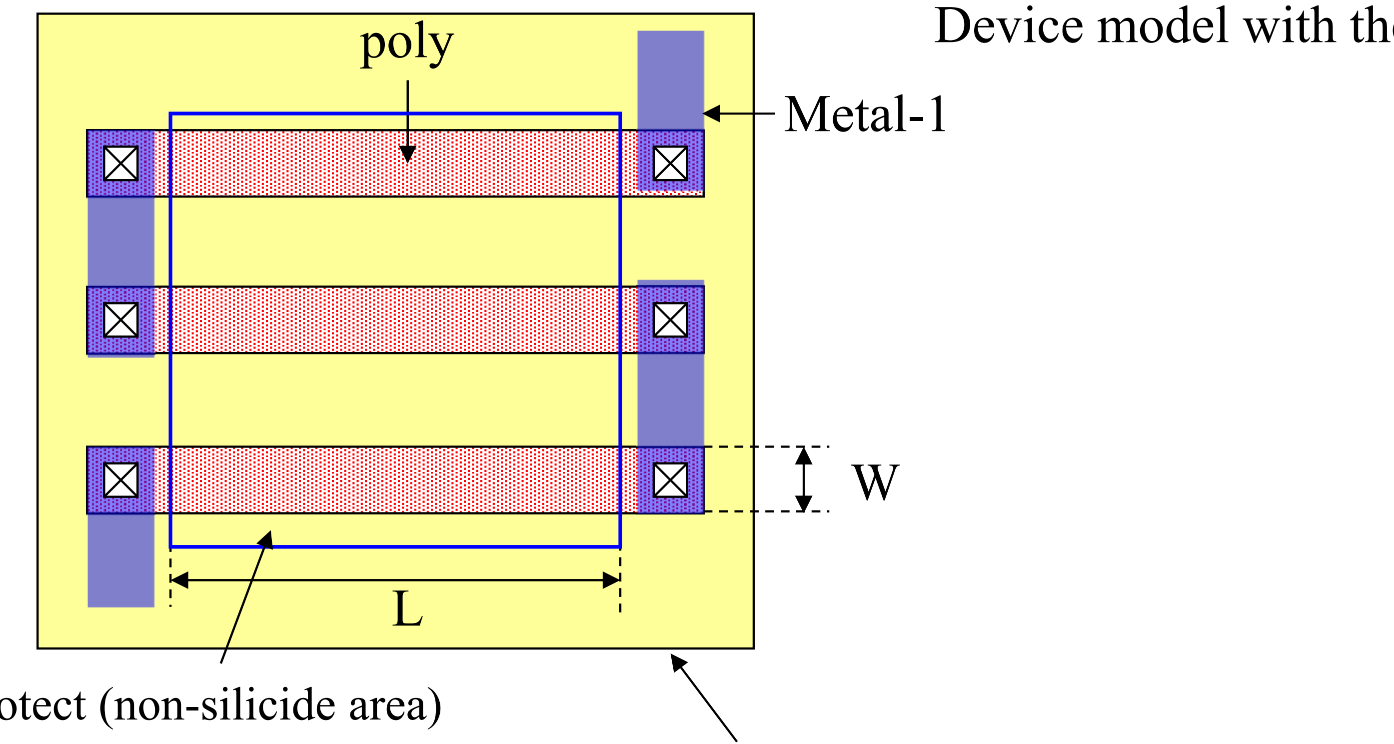
Layout sample of a poly resistor

$$R = R_S \frac{L}{W}$$ (recommended L/W > 5)

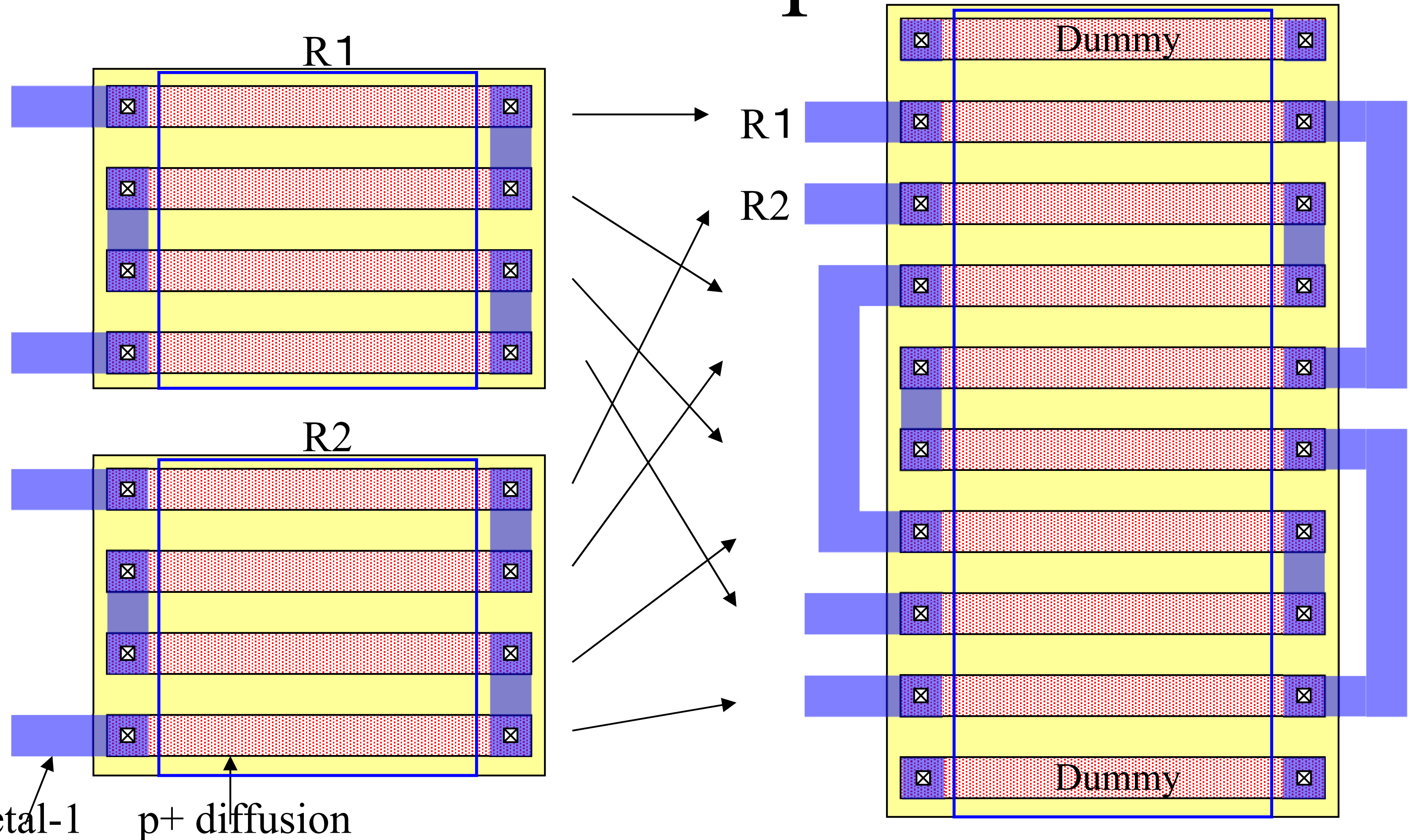
R_S : *Sheet Resistance*



Device model with the parasitic



Common centroid layout of a resistor pair



6.4 Noise countermeasure layout

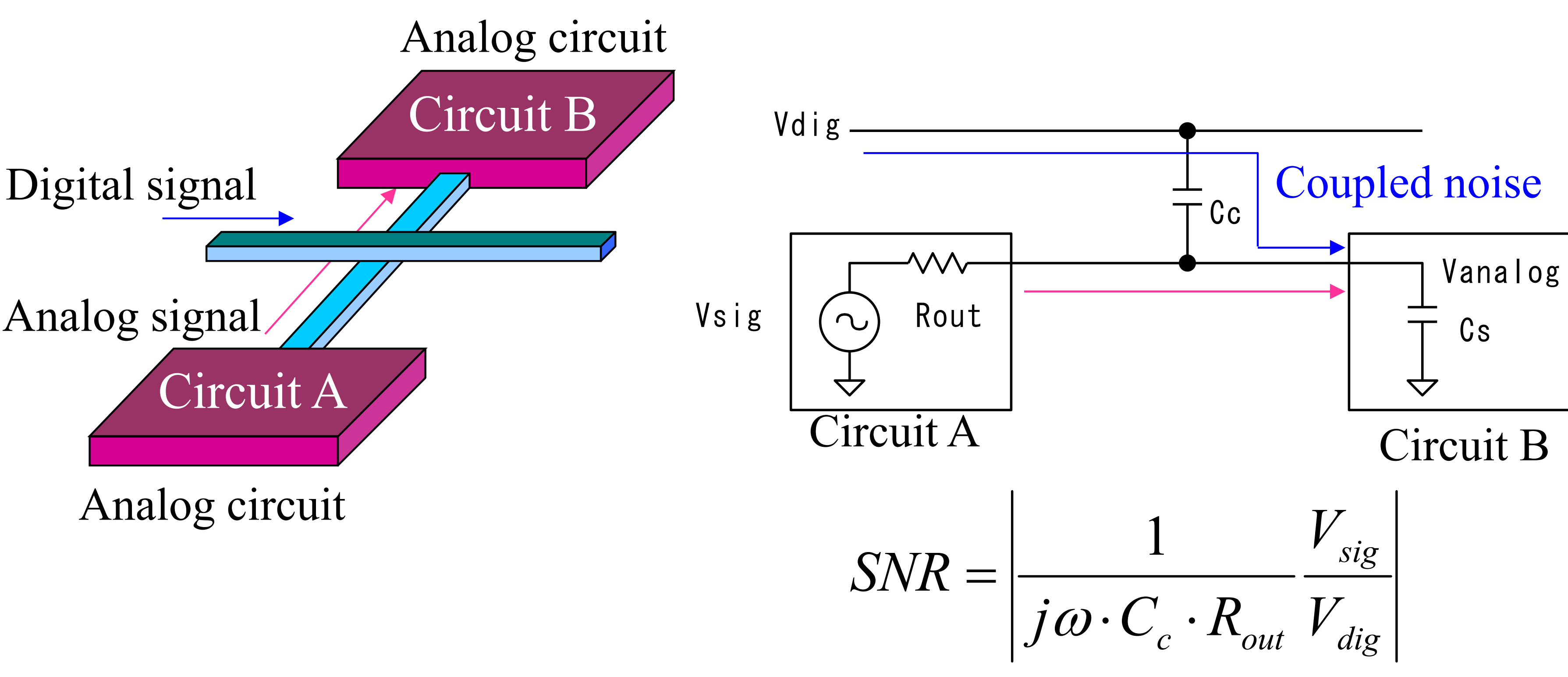
Type of noise

- Inherent noise
  - Noise resulting from the discrete and random movement of charge in a device
  - Thermal noise, Flicker noise, shot noise
  - The noise floor depends on the circuit design quality
- Quantization noise
  - Noise resulting from the finite digital word size
  - The SNR (signal-to-noise ratio) depends on the accuracy of ADC and DAC.
- Coupled noise (Crosstalk)
  - Noise resulting from the signals adjacent circuits deeding into each other
  - The noise immunity depends on a layout.

Type of coupled noise

Electromagnetic model		Circuit model
• Capacitive coupling	→	Parasitic capacitance
• Inductive coupling	→	Parasitic inductance
• Substrate current	→	Parasitic resistance

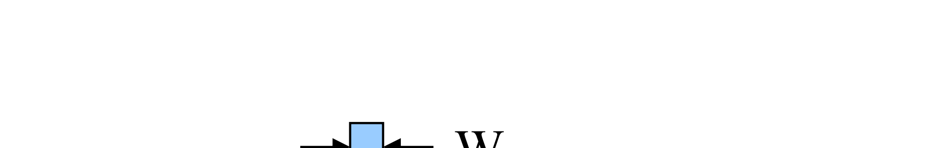
Capacitive coupling



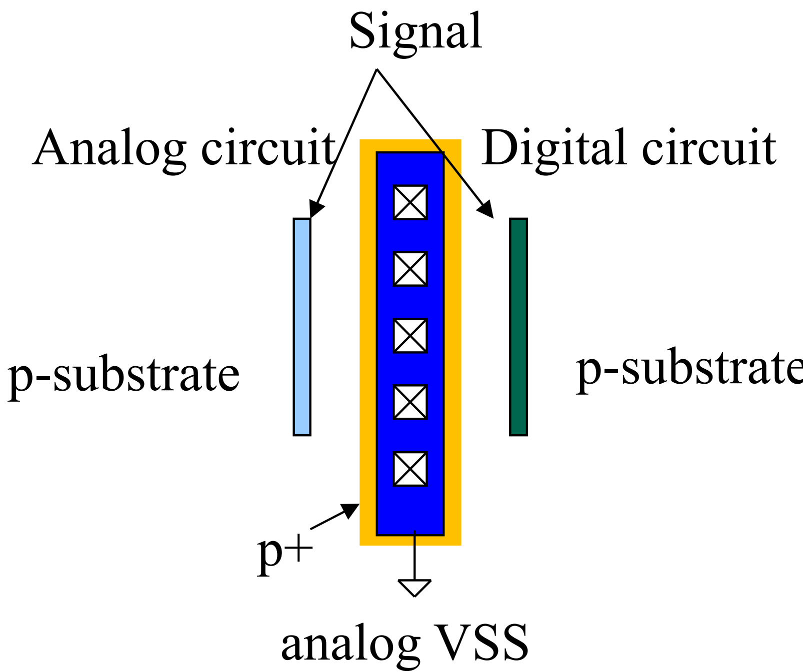
$$SNR = \left| \frac{1}{j\omega \cdot C_c \cdot R_{out}} \frac{V_{sig}}{V_{dig}} \right|$$

Shielding of interconnects

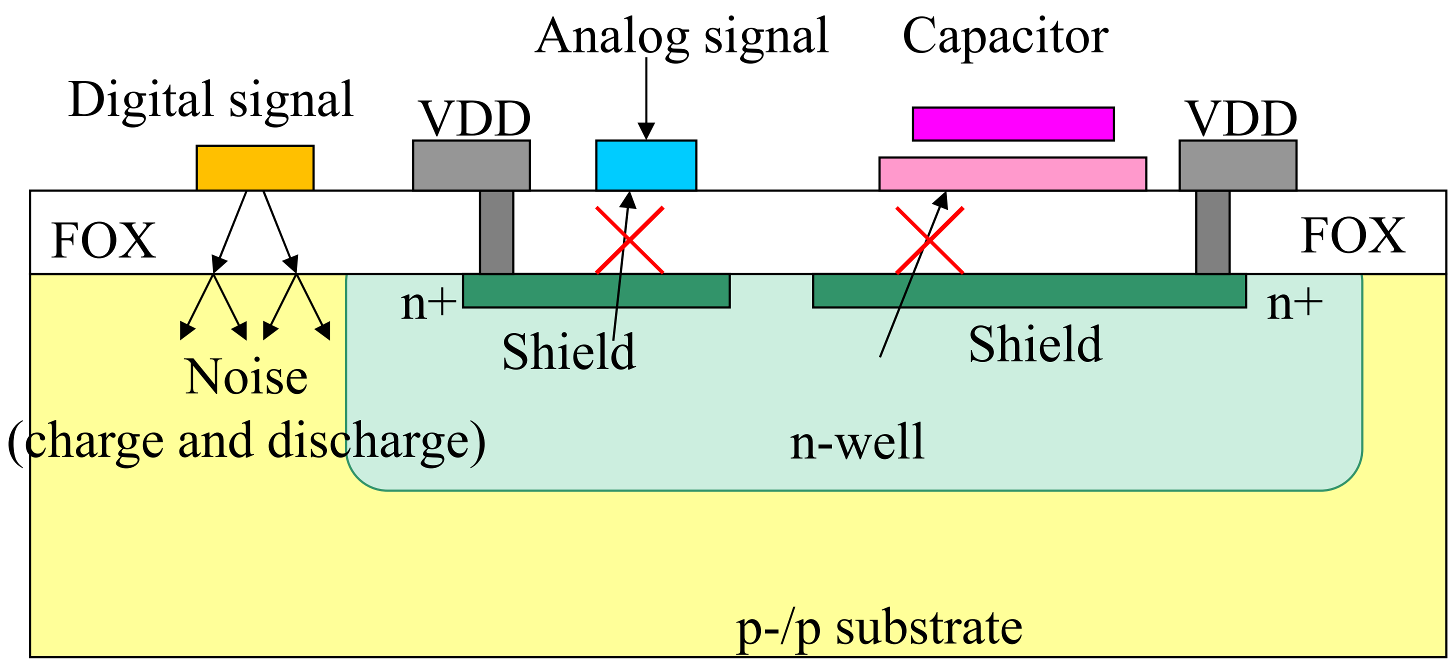
Shielding plate



Shielding line (Partition)

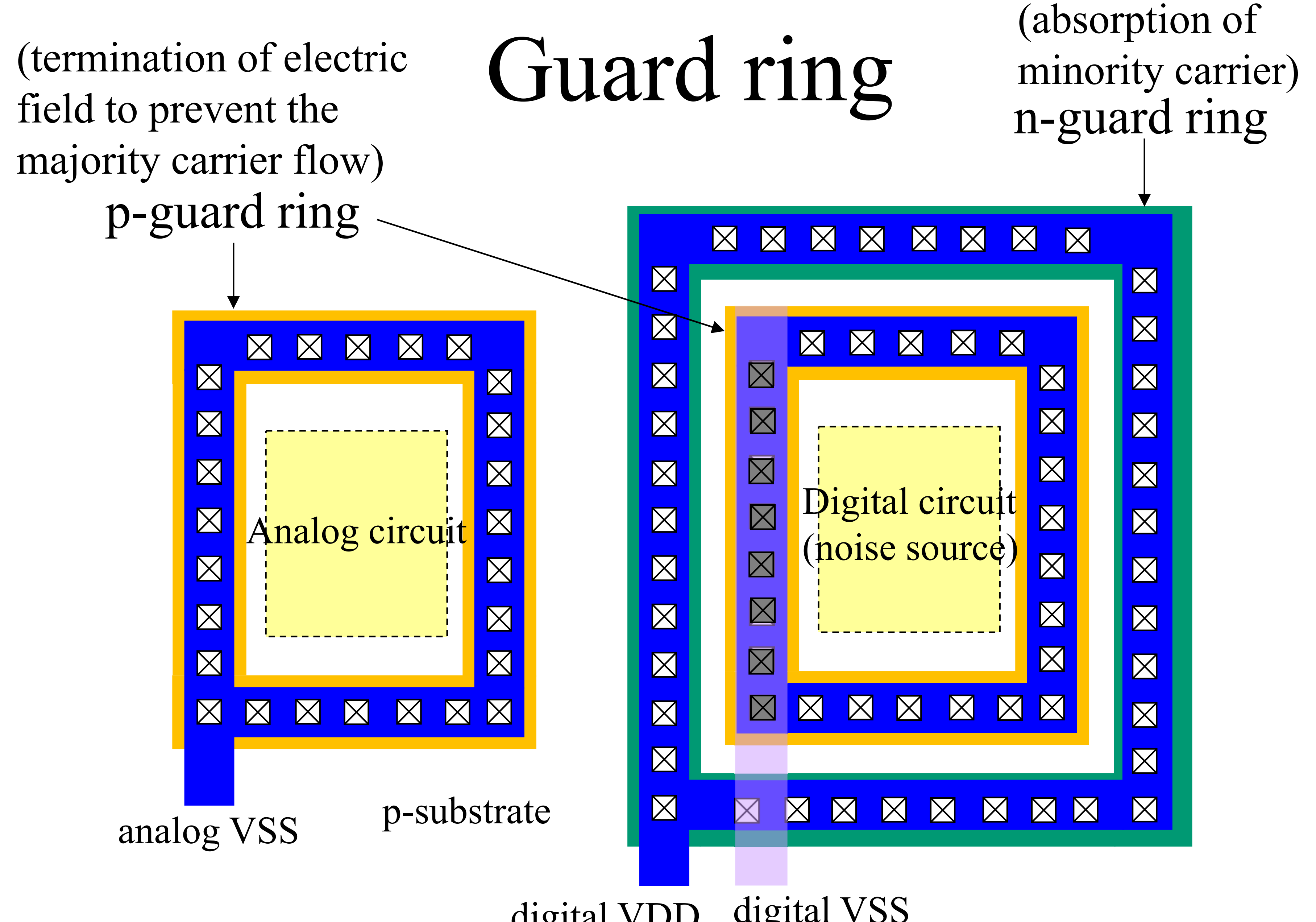


Shielding of substrate

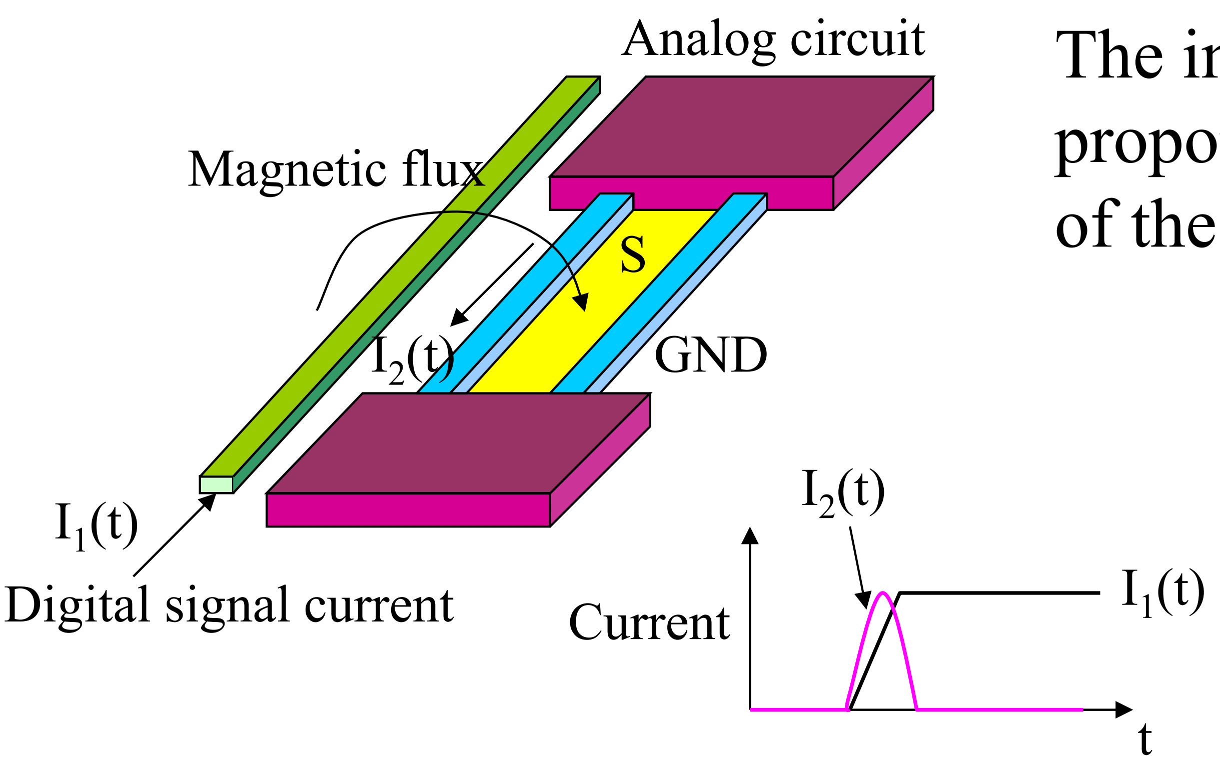


Cross section

Guard ring

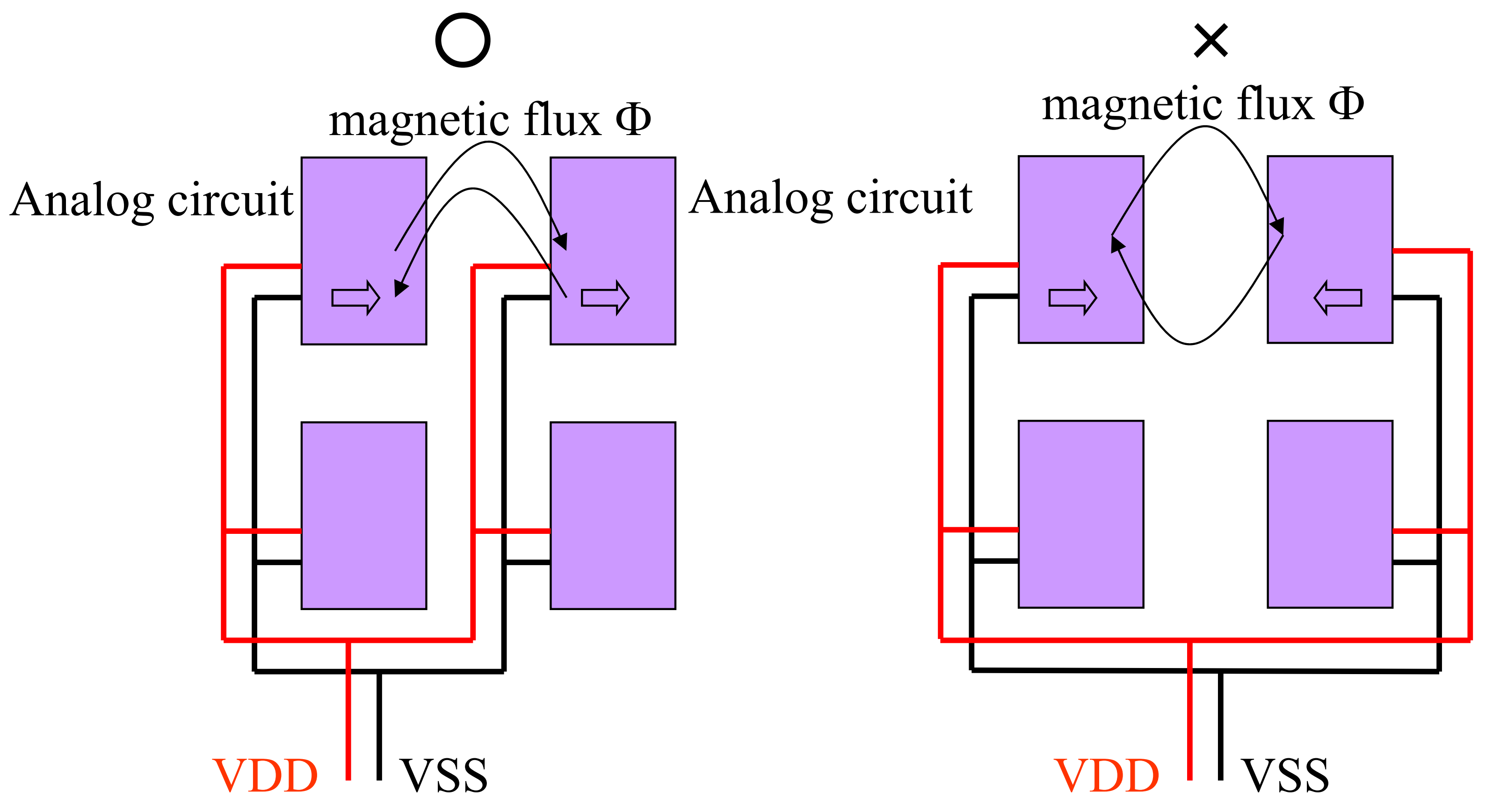


Inductive coupling



The induction noise is in proportion to the loop area S of the signal and power line.

Translational symmetric layout for In-phase circuits

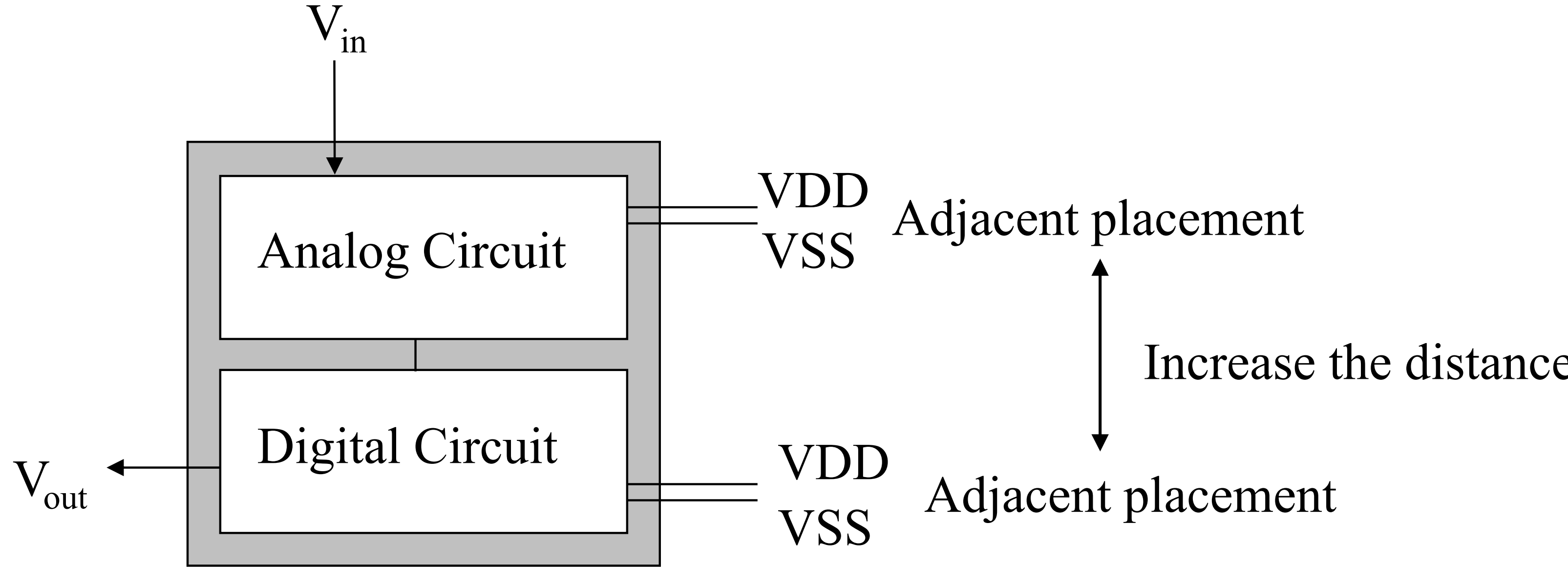


The translational symmetry reduces induced current.

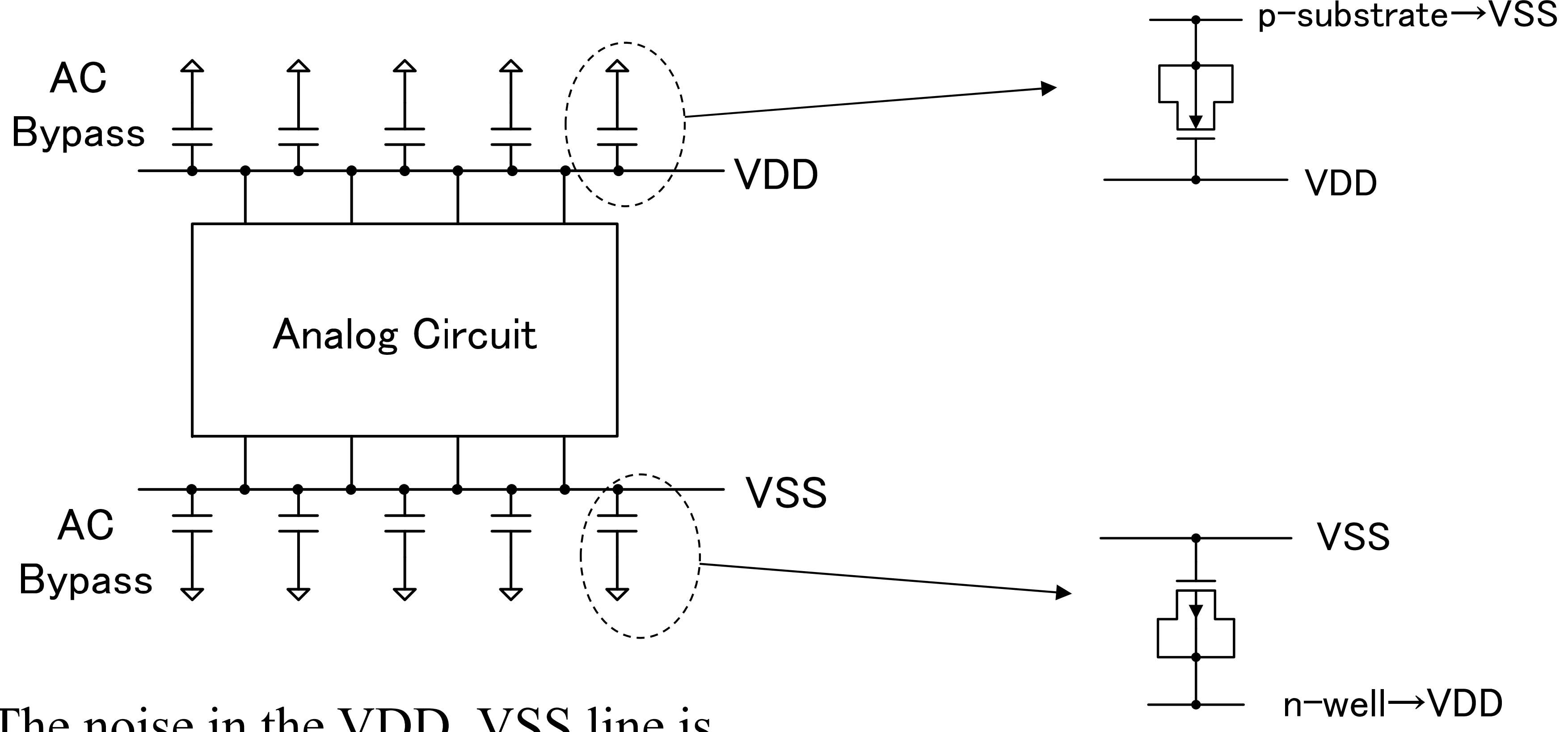
The mirror symmetry intensifies the induced current.

Pin assignment

The analog input should be arranged in a perpendicular direction on digital output and the power supply pin.



Bypass capacitors on VDD, VSS lines



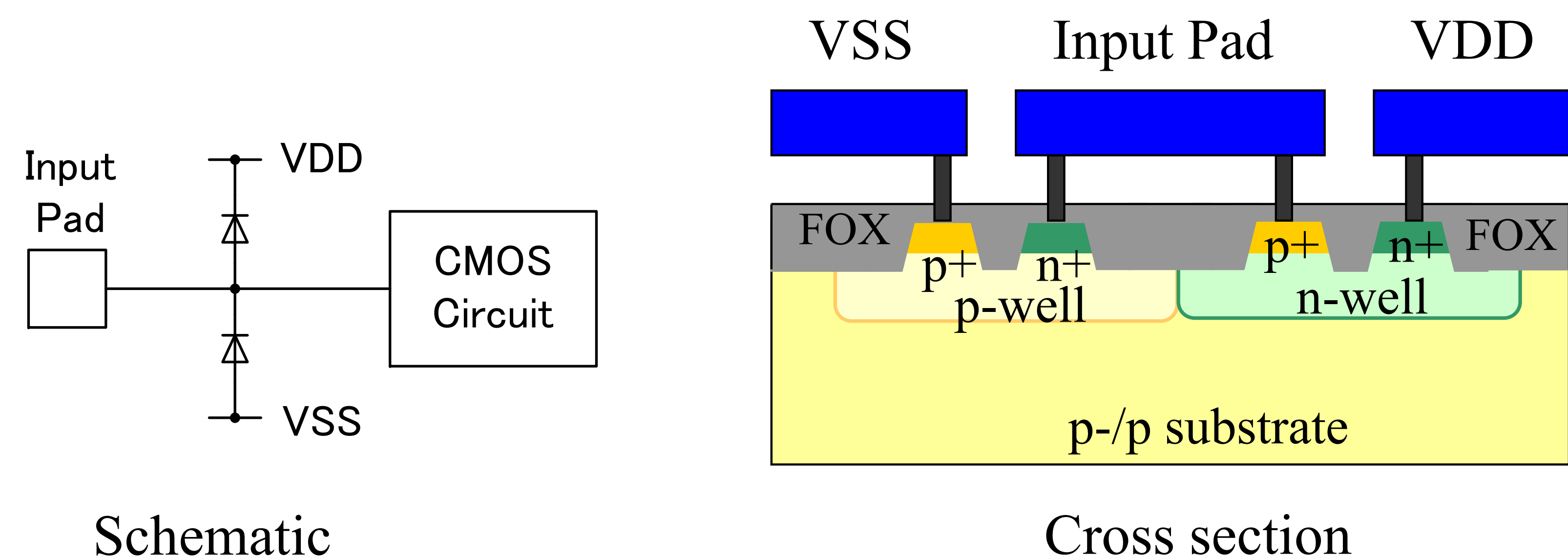
The noise in the VDD, VSS line is bypassed through the bypass capacitors.

Small MOS capacitors under the power line.

6.5 ESD (Electrostatic Discharge) Protection

Input Pad with ESD protection

The ESD protection is required to prevent the damage of the GOX of a MOSFET from the static charge buildup.



Schematic

Cross section

NOTE: If the inductive load is used the output, the amplitude of the output signal is larger than power supply voltage. In this case, the ESD protection diode must be connected tandemly.

Layout sample of pad ESD protection

Layer

- n-well
- n-active (n+)
- p-active (p+)
- poly-1
- contact
- metal-1
- via-1
- metal-2