9. Voltage references

A voltage and current reference are used for the reference of bias circuit, DAC and ADC.

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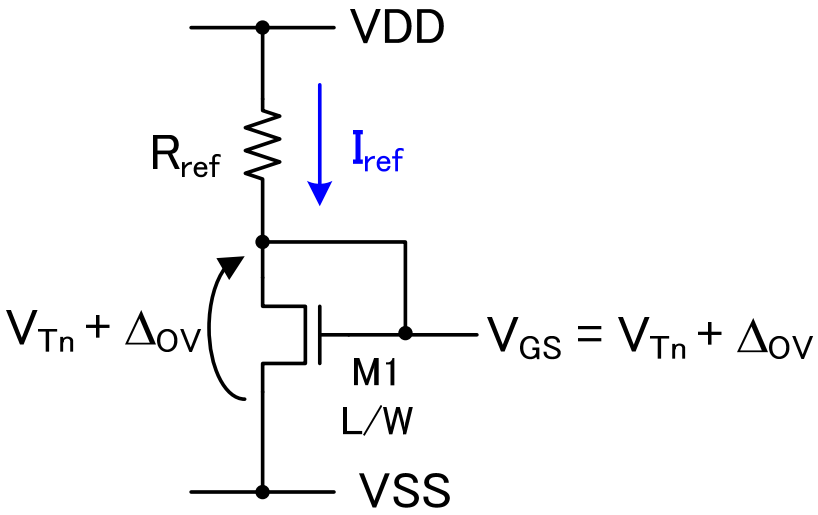
9.1 Simple reference circuits

R-MOSFET voltage reference

$$I_{ref} = \frac{1}{R_{ref}}(VDD - V_{Tn} - \Delta_{OV})$$

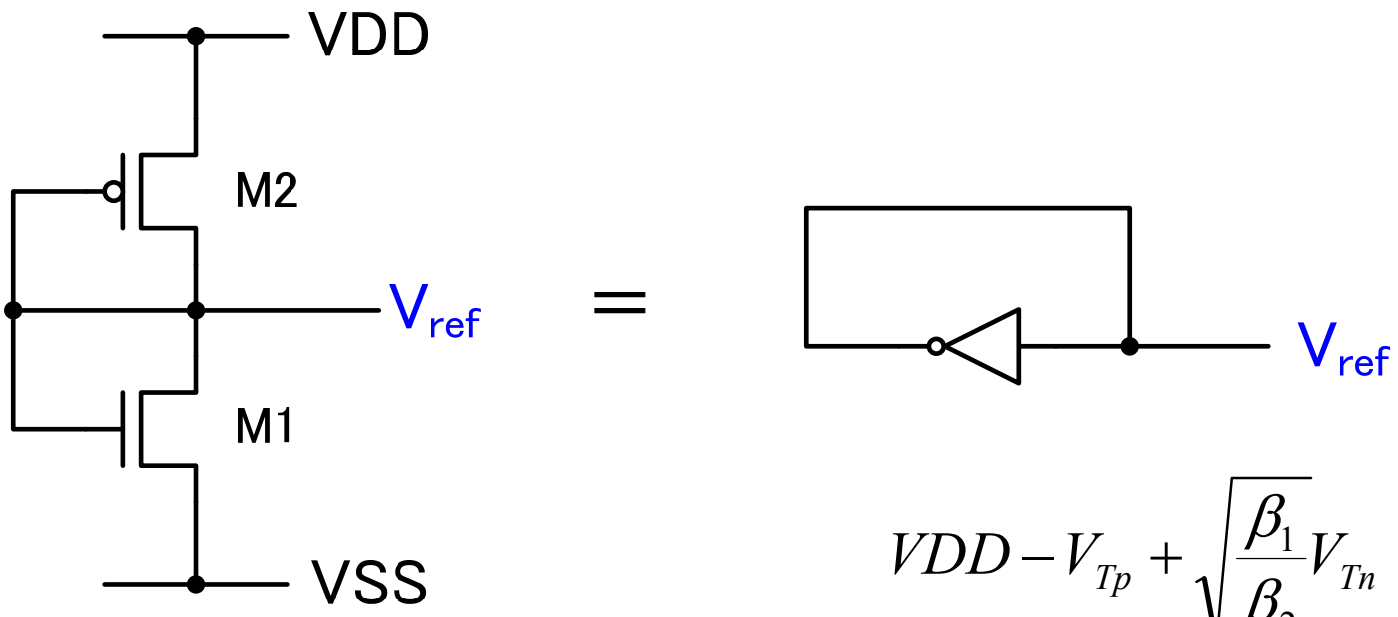
$$= \frac{1}{R_{ref}}(VDD - V_{Tn} - \sqrt{\frac{2I_{ref}}{\beta_n}})$$

$$\approx \frac{1}{R_{ref}}(VDD - V_{Tn}) \quad \text{if } I_{ref} \text{ is small enough.}$$



- Bad stability against the temperature variation, because the temperature coefficient of I_{ref} depends on the temperature coefficient of R_{ref} and $V_{Tn}+\Delta_{OV}$.
- No stability against VDD, because I_{ref} and V_{GS} depend on VDD.

MOSFET Driver

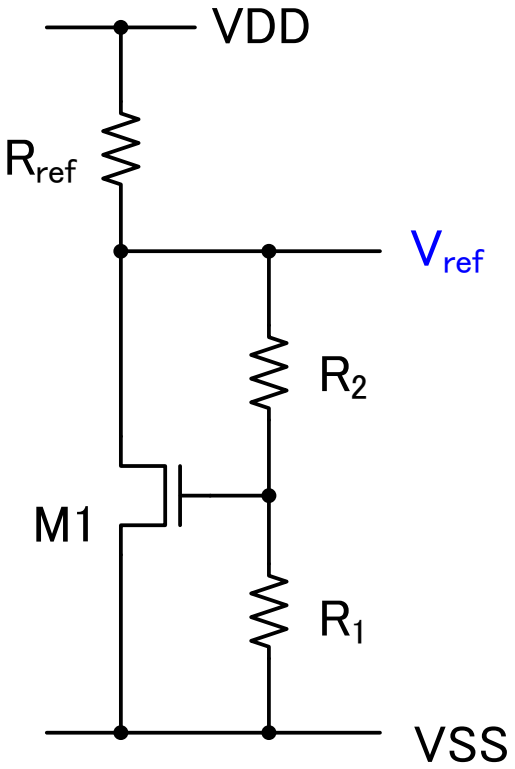


$$V_{ref} = \frac{VDD - V_{Tp} + \sqrt{\frac{\beta_1}{\beta_2}} V_{Tn}}{1 + \sqrt{\frac{\beta_1}{\beta_2}}}$$

- No stability against VDD, because V_{ref} depends on VDD.
- The temperature coefficient of V_{Tn}, V_{Tp} can be canceled by a temperature coefficient of β_1/β_2.

Threshold-Voltage Multiplier

This circuit has a NFB loop in which the decrease of I_{ref} causes the increase of V_{GS}.



$$V_{GS1} = \frac{R_1}{R_1 + R_2} V_{ref}$$

$$V_{ref} = V_{GS1} \cdot (\frac{R_2}{R_1} + 1)$$

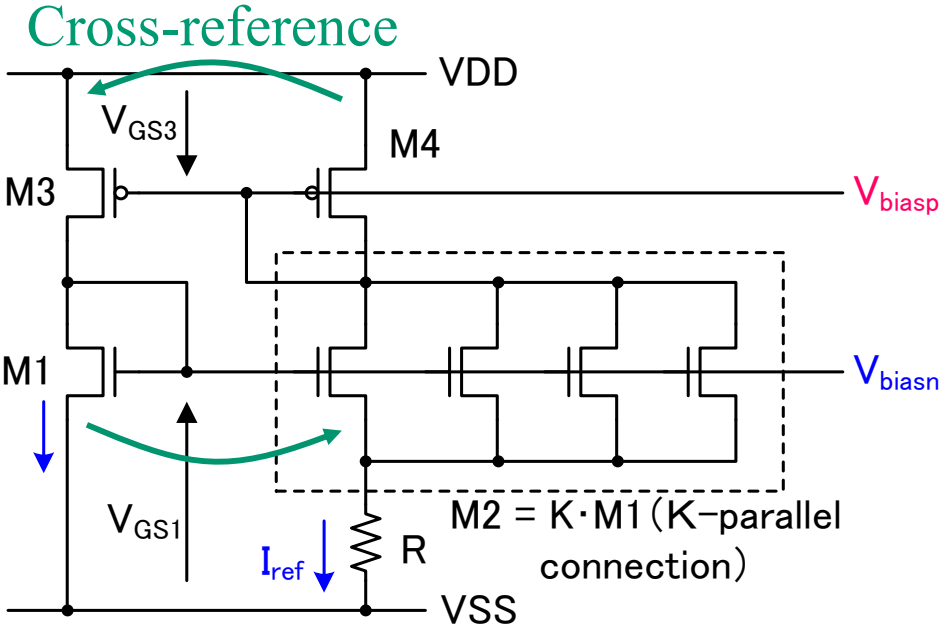
If I_{ref} is small enough,

$$V_{ref} \cong V_{Tn} \cdot (\frac{R_2}{R_1} + 1)$$

V_{ref} does not depends on VDD.

9.2 Beta-Multiplier Reference (BMR)

Principle of BMR circuit



$$\begin{cases} I_{DS4} = I_{DS3} \\ I_{DS1} = I_{DS2} \equiv I_{ref} \\ V_{GS1} = V_{GS2} + I_{ref} R \end{cases}$$

i.e.

$$\beta_2 = \beta_1 \rightarrow I_{ref} R = 0 \, (V_{GS1} = V_{GS2})$$

$$\beta_2 = K\beta_1 \rightarrow I_{ref} R \neq 0 \, (V_{GS1} = V_{GS2} + I_{ref} R)$$

(BMR: Beta-Multiplier Reference)

$$I_{DS1} = \frac{\beta_1}{2}(V_{GS1} - V_{Tn})^2$$

$$I_{DS2} = \frac{\beta_2}{2}(V_{GS2} - V_{Tn})^2 = K\frac{\beta_1}{2}(V_{GS2} - V_{Tn})^2$$

$$I_{DS1} = I_{DS2} = I_{ref}$$

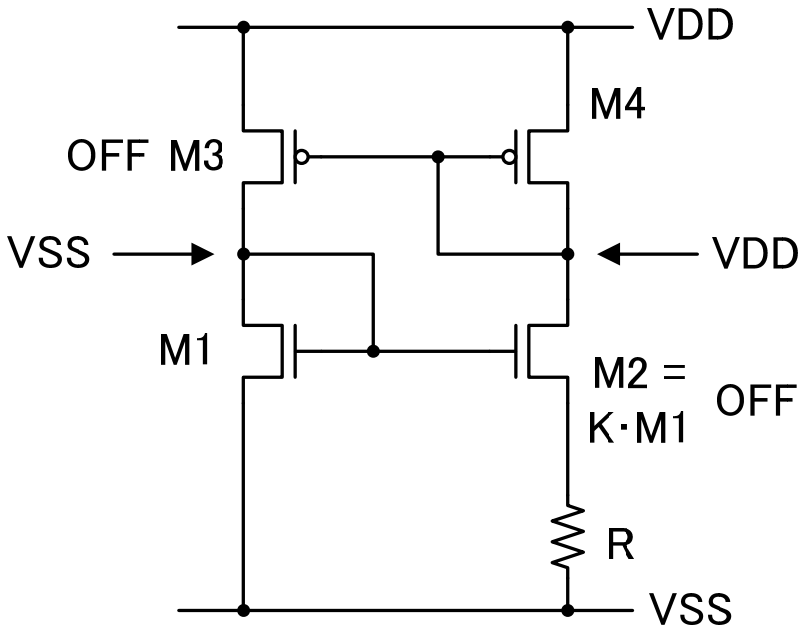
$$I_{ref} = \frac{1}{R}(V_{GS1} - V_{GS2}) = \frac{1}{R^2}\frac{2}{\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

$\Leftarrow$ I_{ref} is independent on VDD.
The temperature coefficient of I_{ref} depends on the temperature coefficients of R and β_1.

Start-up circuit (1)

BMR has two operating state because of a positive feedback.

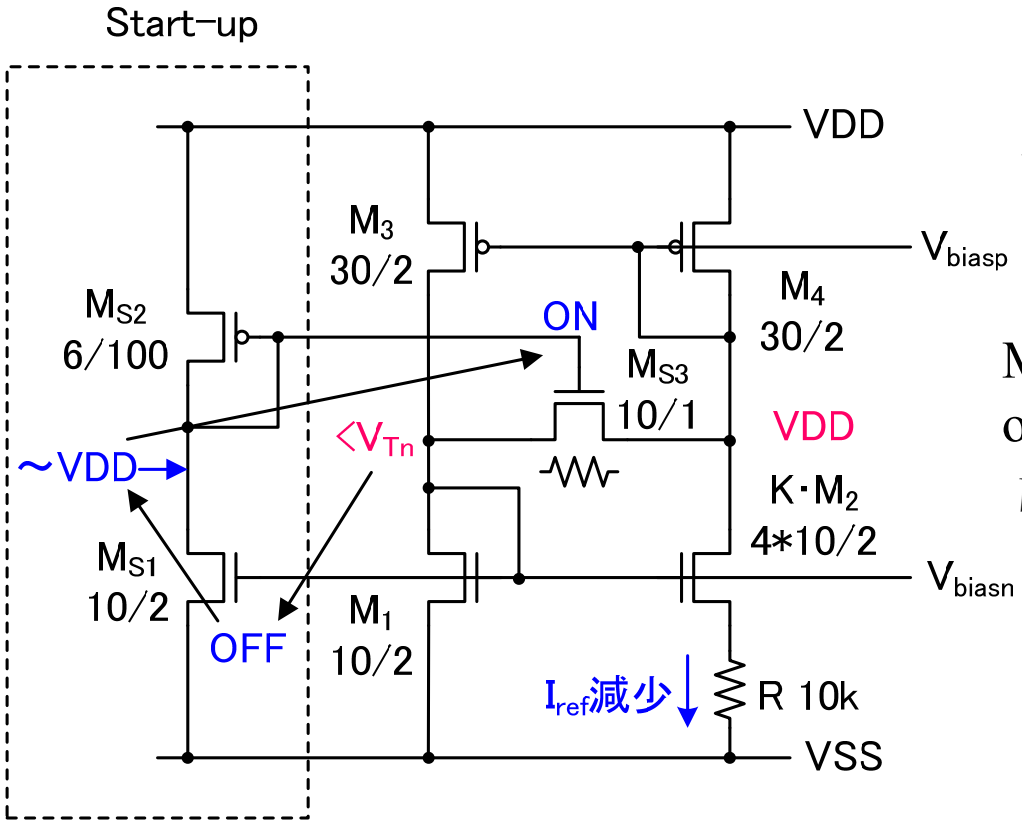
⇨ The initial state should be determined by the start-up circuit.



"$I_{ref} = 0$" is a solution of the circuit equation too.

Start-up circuit (2)

The drain potential of M1-M4 is equalized by MS3.



$$I_{DS\_MS1} = I_{DS\_MS2} = I_{ref}$$ (Normal operation)

$$V_{GS\_MS2} = \sqrt{\frac{2I_{ref}}{\beta_{MS2}}} + V_{Tp}$$

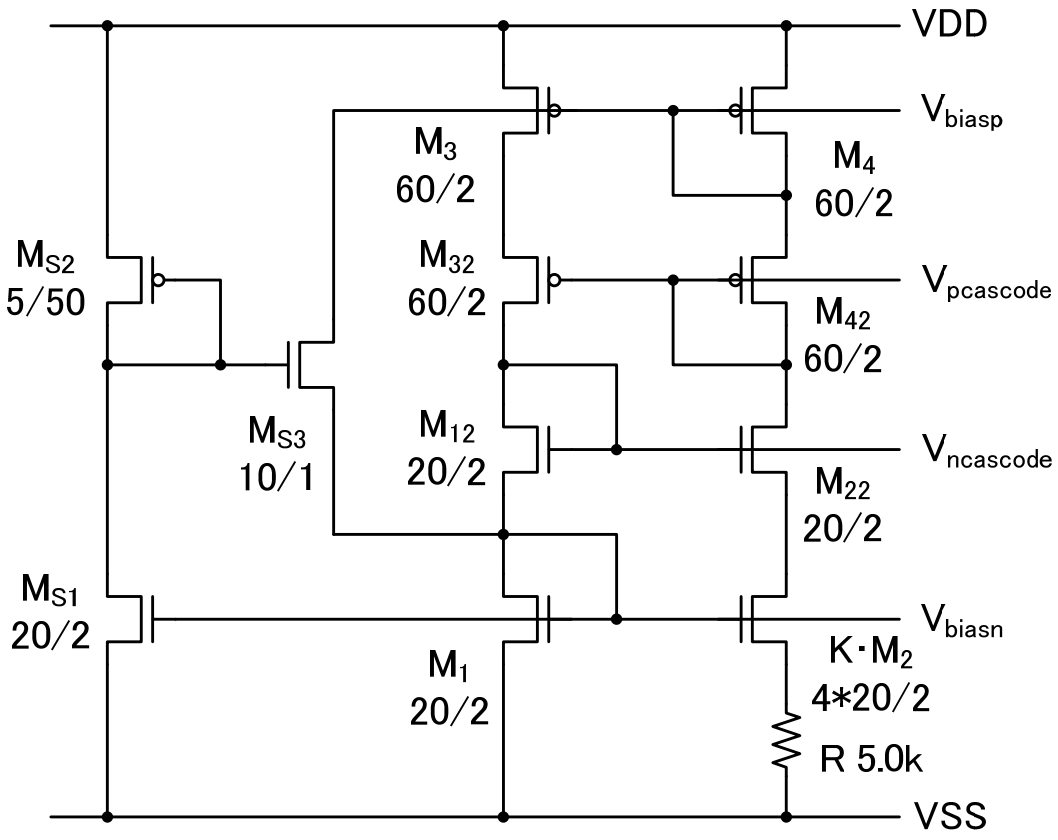
MS3 should be turned off in the normal operation.

$$V_{GB\_MS3} = VDD - V_{GS\_MS2} - VSS$$

$$= (VDD - VSS) - |V_{Tp}| - \sqrt{\frac{2I_{ref}}{\beta_{MS2}}} < V_{Tn}$$

NOTE: The gate length L of MS2 is often very long, if I_{ref} is small value.

Design example of cascode BMR



For $I_{ref} = 20uA$,

$$\Delta_{OV} = \sqrt{\frac{2I_{ref}}{\beta_1}} = \sqrt{\frac{2 \cdot 20u}{98u \cdot 10}} = 0.20V$$

$$R = \sqrt{\frac{2}{I_{ref}\beta_1}}\left(1 - \frac{1}{\sqrt{K}}\right)$$

$$= \sqrt{\frac{2}{20u \cdot 98u \cdot 10}}(1 - \frac{1}{2}) = 5.0k\Omega$$

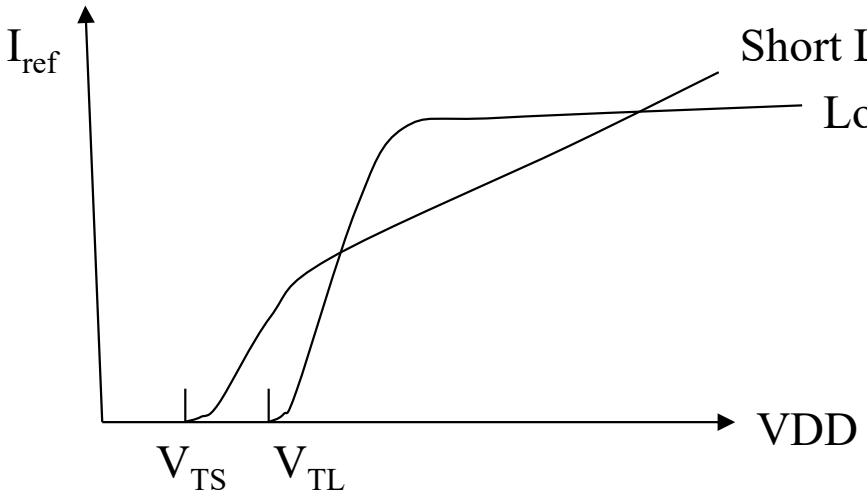
$$\beta_{MS2} < \frac{2I_{ref}}{(VDD - VSS - |V_{Tp}| - V_{Tn})^2}$$

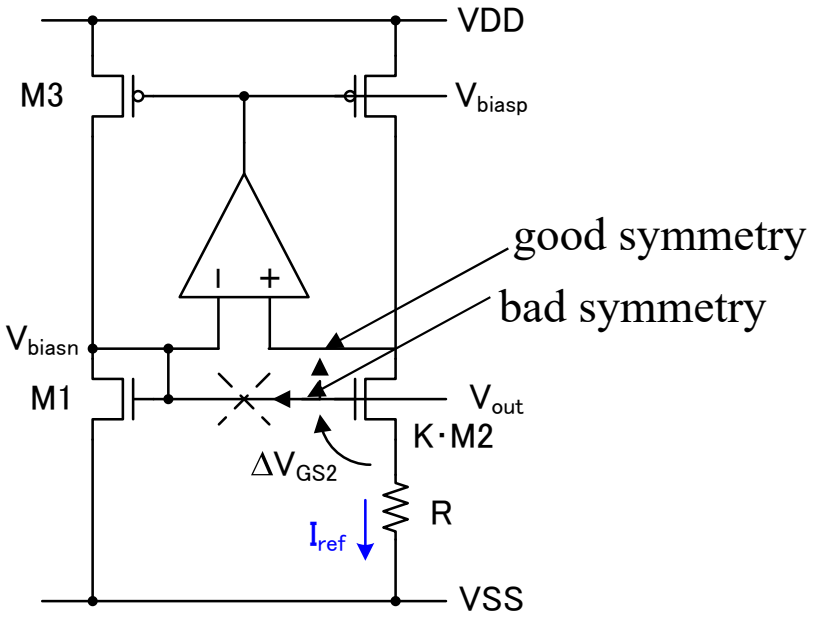
$$= \frac{2 \cdot 20u}{(5.0 - 1.6)^2} = 3.46u$$

$$\frac{W_{MS2}}{L_{MS2}} < \frac{3.46u}{33u} = 0.105$$

Voltage regulation

Short channel MOSFET vs.
Long channel MOSFET





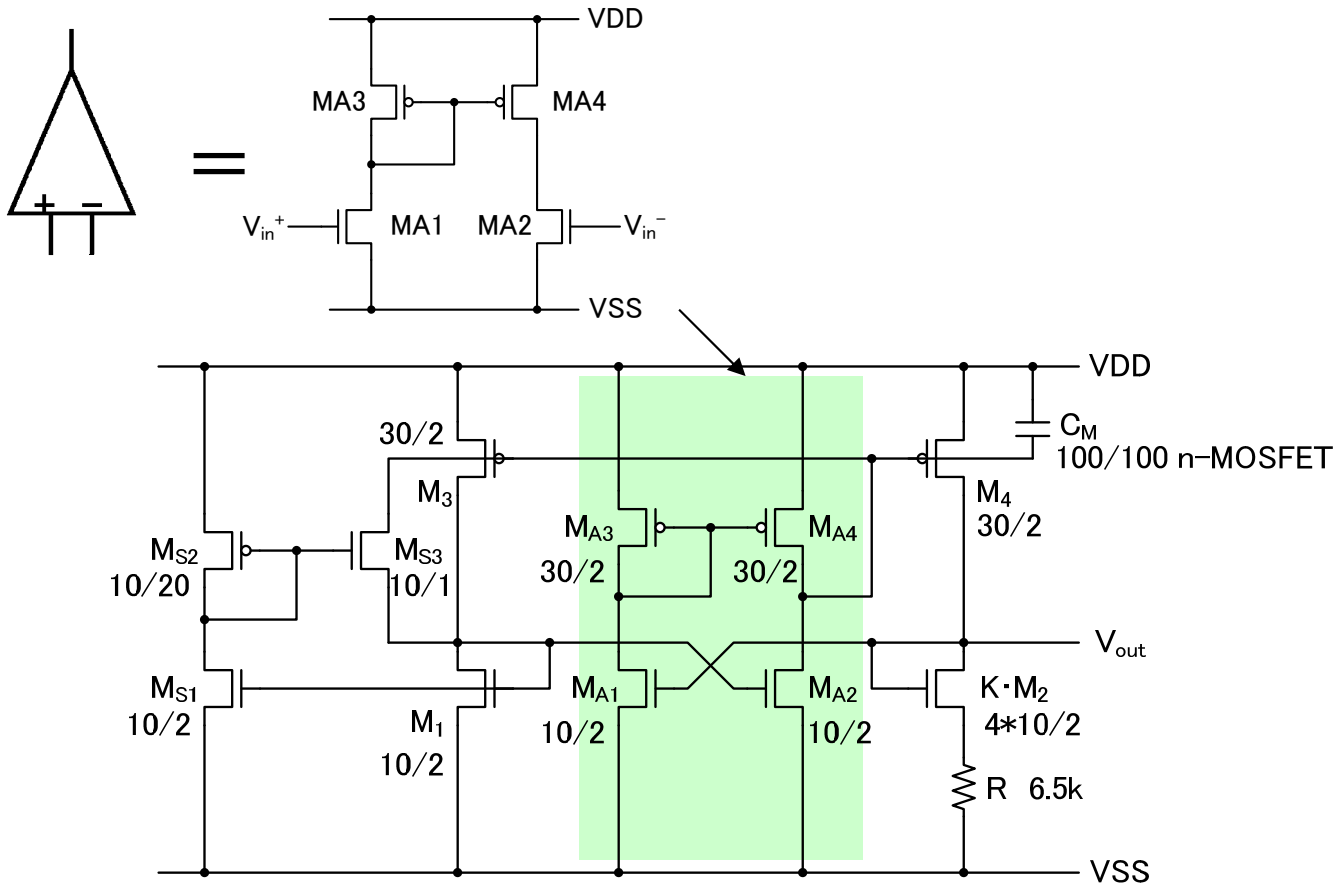
$$V_{biasp} = A_d(V_{out} - V_{biasn}) \xrightarrow{A_d \to \infty} V_{out} = V_{biasn}$$

I_{ref} depends on the drain voltage, because the saturation of I_{DS}-V_{DS} characteristics of the short channel MOSFET is not distinguished clearly.

Negative feedback control to maintain $V_{biasn} = V_{out}$

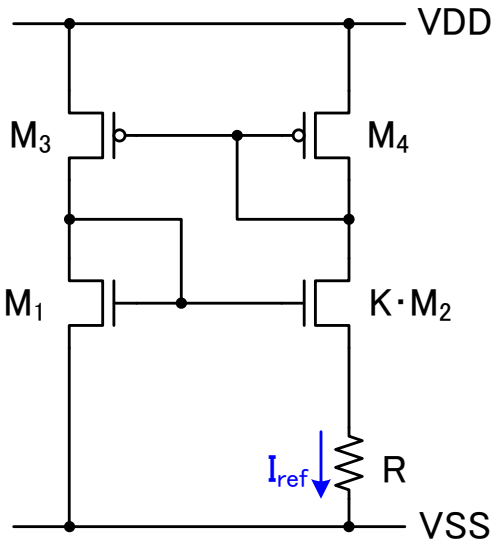
Low-voltage BMR with the voltage regulation

BMR circuit for the short channel MOSFET



Sub-threshold BMR for low-power circuits

Very low power consumption BMR



The circuit topology is same as the normal BMR.

I_{DS}-V_{GS} characteristic in the sub-threshold region.

$$I_{DS} = \frac{W}{L} I_0 \exp\{\frac{q(V_{GS} - V_T)}{mkT}\}, \quad m = 1 + \frac{C_D}{C_{OX}}$$

$$\begin{cases} V_{GS1} = m\frac{kT}{q}\ln(\frac{I_{ref}}{I_0}\frac{L}{W}) + V_{Tn} \\ V_{GS2} = m\frac{kT}{q}\ln(\frac{I_{ref}}{I_0}\frac{L}{K \cdot W}) + V_{Tn} \end{cases}$$

$$I_{ref} = \frac{1}{R}(V_{GS1} - V_{GS2})$$

$$= \frac{m}{R}\frac{kT}{q}\ln K$$

NOTE: The very large resistance R is required.

9.3 Band-gap reference (BGR)

It is not easy to cancel the temperature dependence of $R^2\beta$ in BMR shown in slide 7, because R and MOSFET are fabricated in the different stages of the CMOS process. The temperature coefficient of the reference voltage can be compensated with a pair of pn junctions.

Temperature dependence of pn junction diode

The temperature coefficient is canceled with pn diode.

DC characteristic of pn junction ----

NOTE: Only a diffusion current is modeled in this equation. Therefore, the appropriate bias voltage have to be applied to the pn junction.

$$I = I_S(e^{\frac{qV_D}{kT}} - 1) \cong I_S e^{\frac{qV_D}{kT}}$$

$$V_D = \frac{kT}{q}\ln(\frac{I}{I_S})$$

$$I_S = AT^3 e^{-\frac{E_G}{kT}}$$

Is : Reverse saturation current
k : Boltzmann constant (8.62E-5 eV/K)
T : Absolute temperature (K)
q : electron charge (1.60E-19 coulomb)
E_G : Band-gap energy of Si (1.1eV)
A : Constant depending on the effective density of state and impurity concentrations

CTAT (Complementary to absolute temperature)

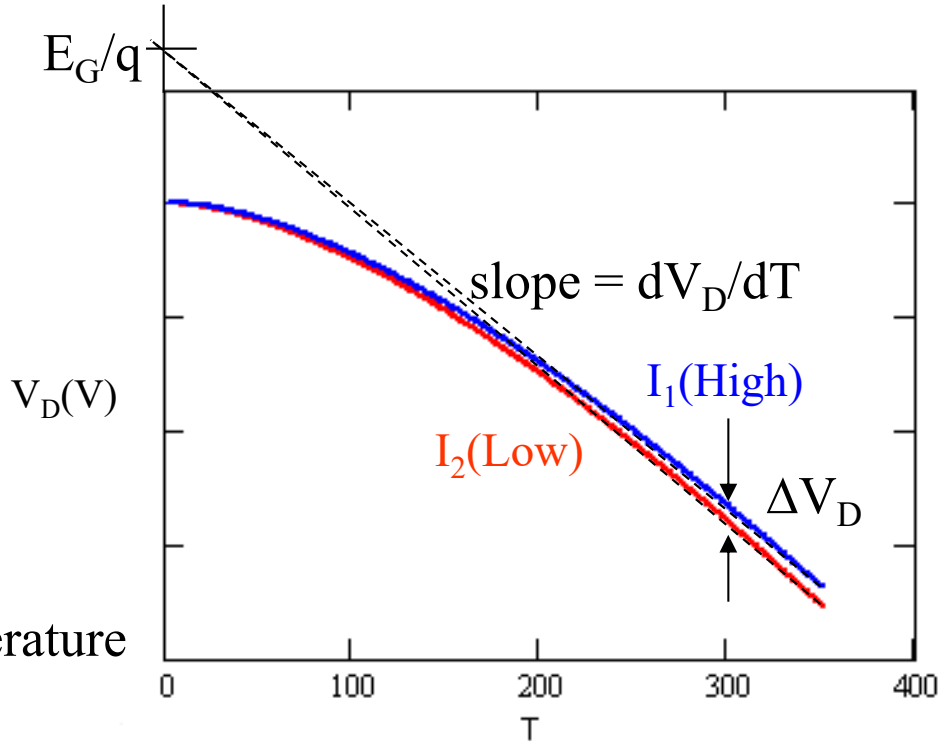
$$V_D = \frac{kT}{q}\ln(\frac{I}{I_S})$$

$$= \frac{kT}{q}\ln(\frac{I}{AT^3}e^{\frac{E_G}{kT}})$$

$$= \frac{1}{q}(kT\ln\frac{I}{T^3} - kT\ln A + E_G)$$

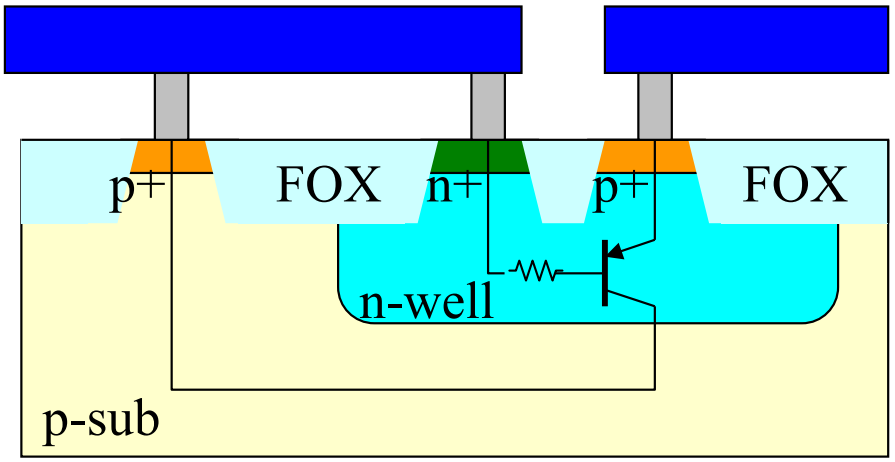
$$\frac{dV_D}{dT} \approx -\frac{k}{q}\ln A$$

CTAT at room temperature

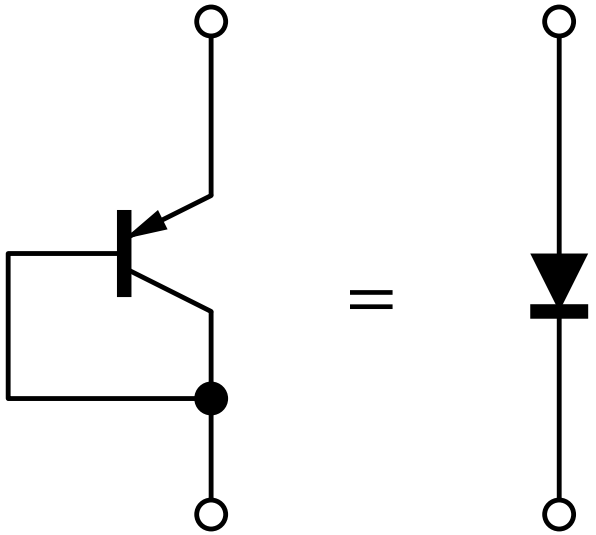


- V_D has a negative temperature coefficient at room temperature.
- ΔV_D has a positive temperature coefficient at room temperature.

Structure of the pn junction diode



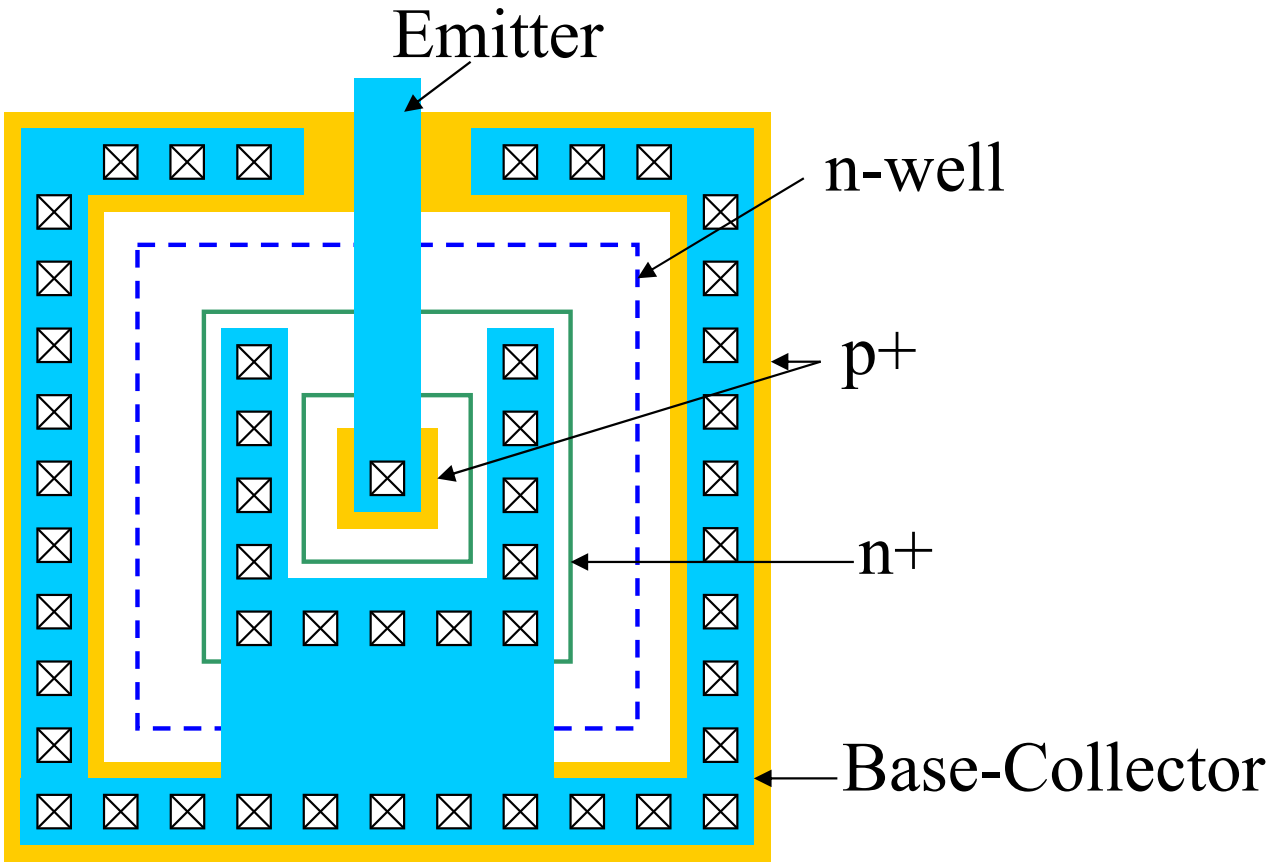
Vertical CMOS well bipolar junction transistor



Equivalent schematic

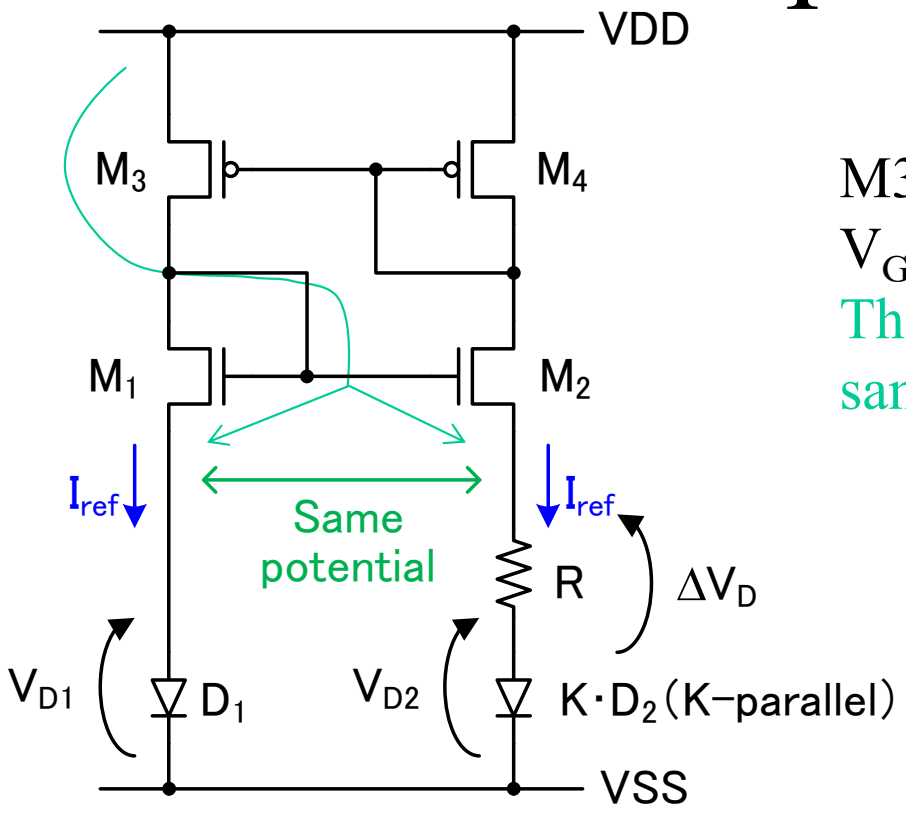
The current I_B should be limited less than 0.1mA to reduce the voltage drop in the base resistance of pnp transistor.

Layout sample of the pn junction diode



Check the production tolerance of pn junction.
The standard deviation of the I-V characteristics of pn junction is rather smaller than V_T of MOSFET, but it may not be controlled by the foundry.

PTAT (Proportional to absolute temperature)



(Start-up circuit is required.)

ΔV_D has a positive temperature coefficient

M3, M4: Current mirror.

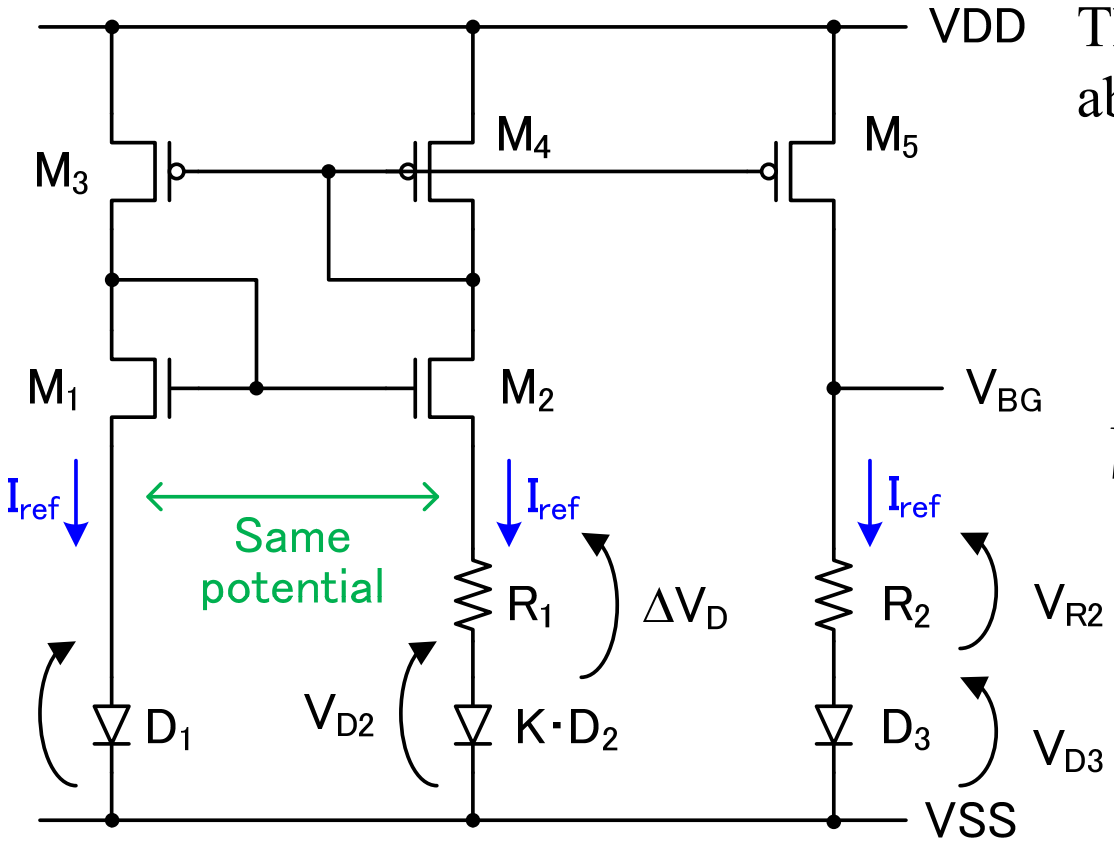
$V_{GS1} = V_{GS2}$ (because the $I_{DS1} = I_{DS2}$)

The source potential of M1 and M2 is same, then $V_{D1} = V_{D2} + \Delta V_D$

$$\begin{cases} I_{D1} = \dfrac{1}{K} I_{D2} \\ V_{D1} = \dfrac{kT}{q} \ln\left(\dfrac{I_{ref}}{I_S}\right) \\ V_{D2} = \dfrac{kT}{q} \ln\left(\dfrac{I_{ref}}{KI_S}\right) \end{cases}$$

$$\Delta V_D = \frac{kT}{q}\left(\ln\frac{I_{ref}}{I_S} - \ln\frac{I_{ref}}{KI_S}\right) = \frac{kT}{q}\ln K$$

BGR voltage reference



The current I_{ref} is proportional to absolute temperature (PTAT).

$$I_{ref} = \frac{\Delta V_D}{R_1} = \frac{kT}{qR_1} \ln K \quad (1)$$

$$V_{BG} = V_{D3} + R_2 \cdot I_{ref}$$

$$= V_{D3} + \frac{R_2}{R_1} \Delta V_D$$

Negative temperature coefficient

Positive temperature coefficient

Cancelation of temperature coefficient

$$V_{BG} = V_{D3} + \frac{R_2}{R_1}\Delta V_D$$

$$= \frac{kT}{q}\ln\frac{I_{ref}}{AT^3} + \frac{E_G}{q} + \frac{R_2}{R_1}\frac{kT}{q}\ln K$$

$$= \frac{kT}{q}\left(\frac{R_2}{R_1}\ln K - \ln\frac{AT^3}{I_{ref}}\right) + \frac{E_G}{q}$$

$$\downarrow$$

$$0$$

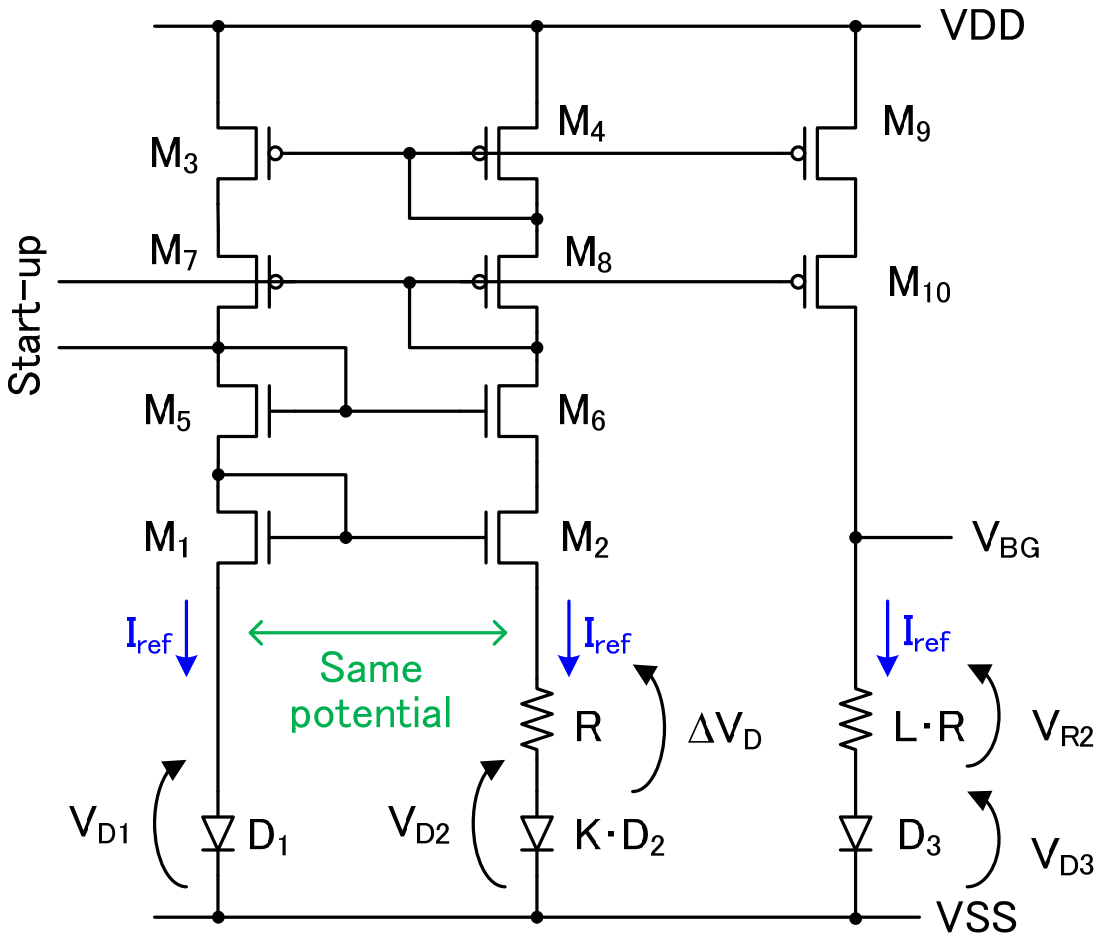
$$\frac{R_2}{R_1} = \frac{\ln\frac{AT^3}{I_{ref}}}{\ln K} \quad (2) \Rightarrow$$

Band-gap Reference

$$V_{BG} = \frac{E_G(J)}{q(coulomb)}$$

Note: The equation (1) is satisfied at the given temperature . You need to measure AT^3 at the operating temperature of the circuit.

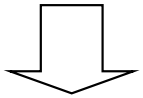
Cascode BGR



M4, M3: Current mirror

$V_{GS1} = V_{GS2}$ because $I_{DS1} = I_{DS2}$.

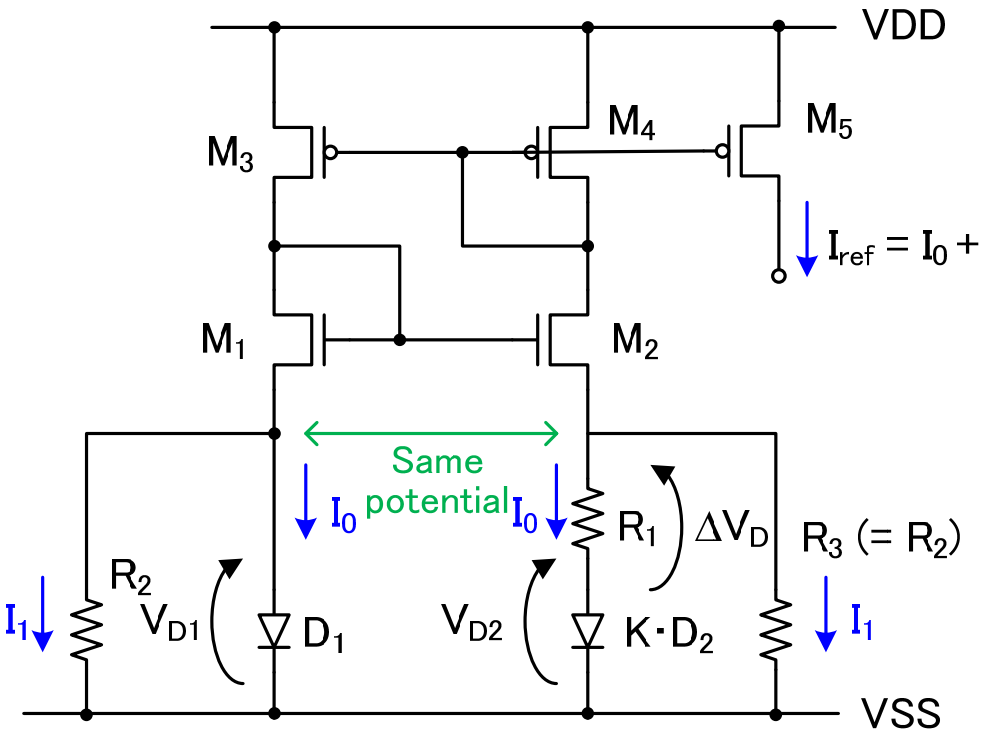
The source potential of M1 and M2 is same, then $V_{D1} = V_{D2} + \Delta V_D$



The cascode current mirror can reduce the current error by the residual temperature dependence of $V_{D3} + V_{R2}$, but it requires the large supply voltage.

BGR current reference

Temperature-independent current reference circuit with BGR

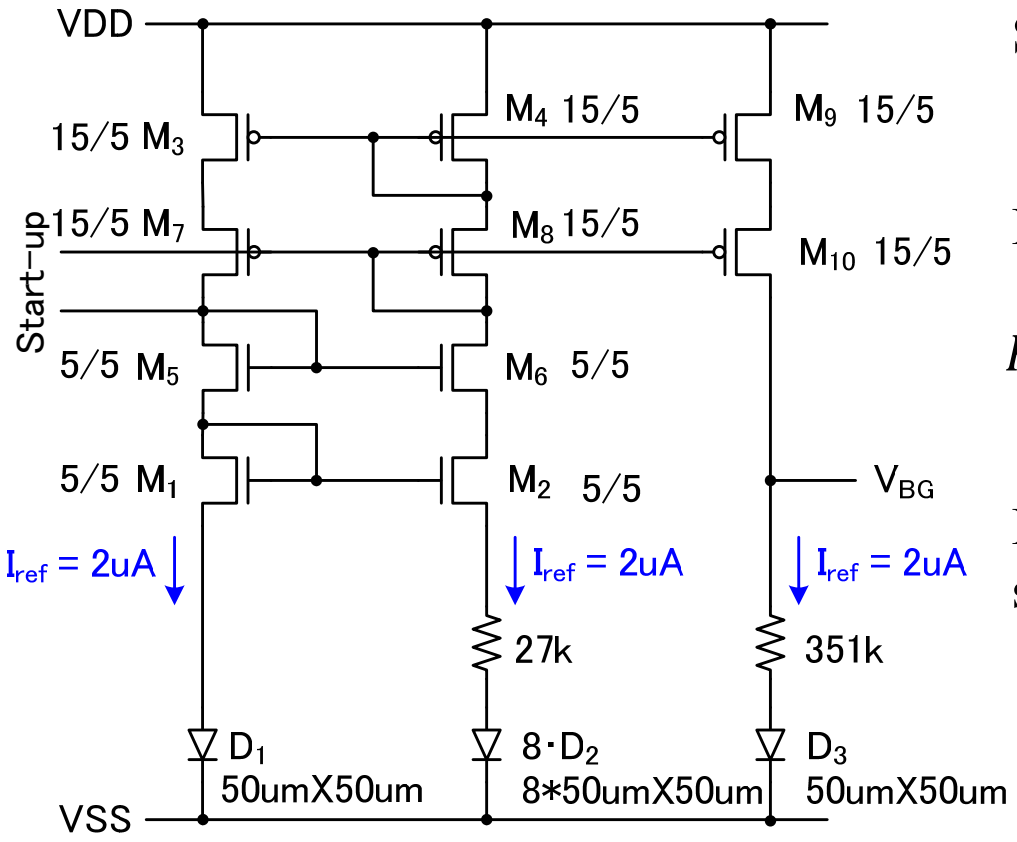


$$\begin{cases} I_0 = \dfrac{\Delta V_D}{R_1} = \dfrac{kT}{qR_1}\ln K \cdot \cdot \cdot PTAT \\ I_1 = \dfrac{V_{D1}}{R_2} = \dfrac{1}{qR_2}\left(-kT\ln\dfrac{AT^3}{I} + E_G\right) \end{cases}$$

$$I_0 + I_1 = \frac{kT}{q}\underbrace{\left(\frac{1}{R_1}\ln K - \frac{1}{R_2}\ln\frac{AT^3}{I}\right)}_{0} + \frac{E_G}{qR_2}$$

$$\frac{R_2}{R_1} = \frac{\ln\dfrac{AT^3}{I}}{\ln K}$$

Design example of cascode BGR



Say I_{ref} = 2uA, K = 8, W_1/L_1 = 1

$$\Delta_{OV} = \sqrt{2I_{ref}/\beta_1} = \sqrt{2 \cdot 2\text{u}/(98\text{u} \cdot 1)} = 0.20\text{V}$$

From Eq.(1) shown in the slide 20,

$$R = \frac{1}{I_{ref}}\frac{kT}{q}\ln(K) = \frac{1.380 \cdot 10^{-23}300}{2\text{u} \cdot 1.602 \cdot 10^{-19}}\ln 8 = 27\text{k}\Omega$$

From the simulation result for 50um-square diode.

$$I_s = 3.45 \cdot 10^{-13}$$

$$A = \frac{I_s}{T^3}e^{\frac{E_G}{kT}} = \frac{3.45 \cdot 10^{-13}}{300^3}e^{\frac{1.1\text{eV}}{8.62 \cdot 10^{-5}300}} = 0.038$$

From Eq.(2) shown in the slide 21, $L = \frac{\ln(\frac{AT^3}{I_{ref}})}{\ln(K)} = \frac{\ln(\frac{0.038 \cdot 300^3}{2\text{u}})}{\ln(8)} = 13$