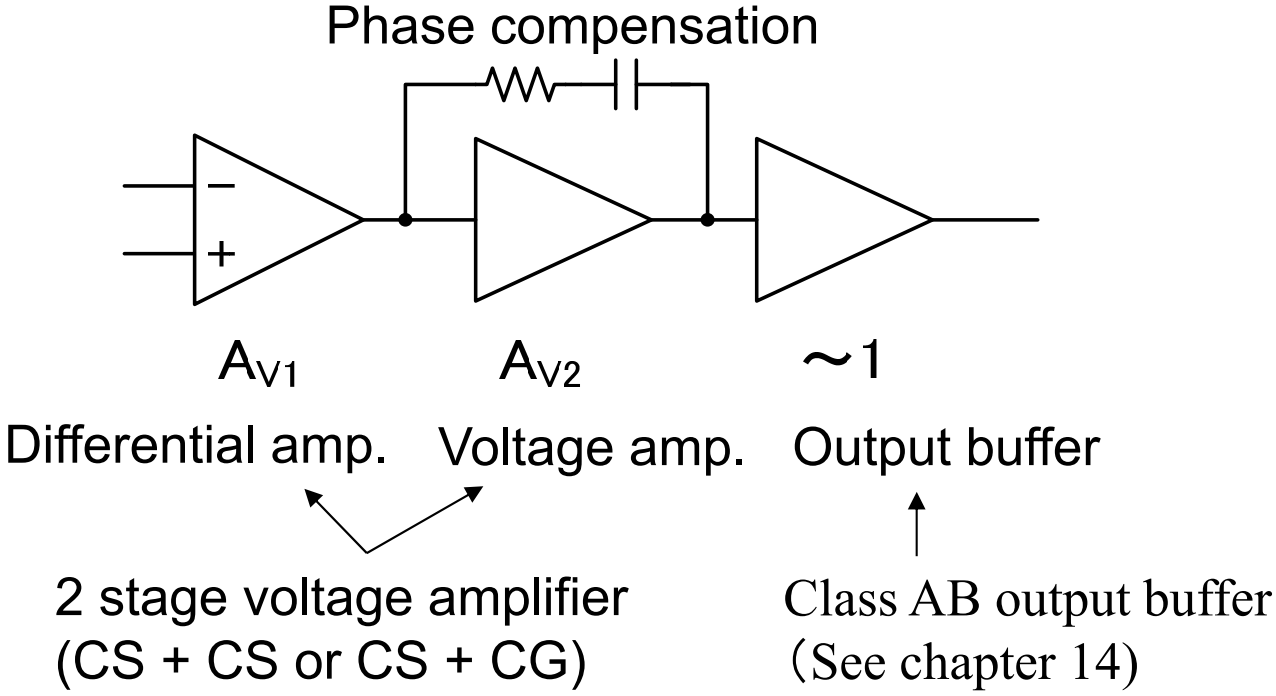
Summary of Chapter 12-13

Mixed signal LSI, Akio Kitagawa, Kanazawa University

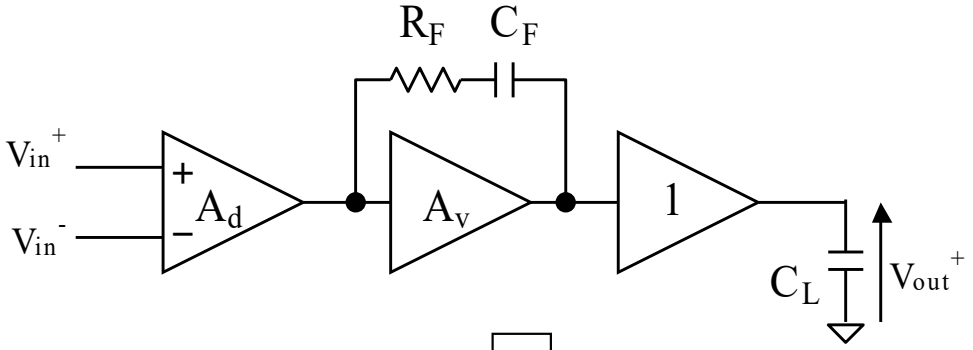
1. Structure of OPA

Circuit configuration of OPA

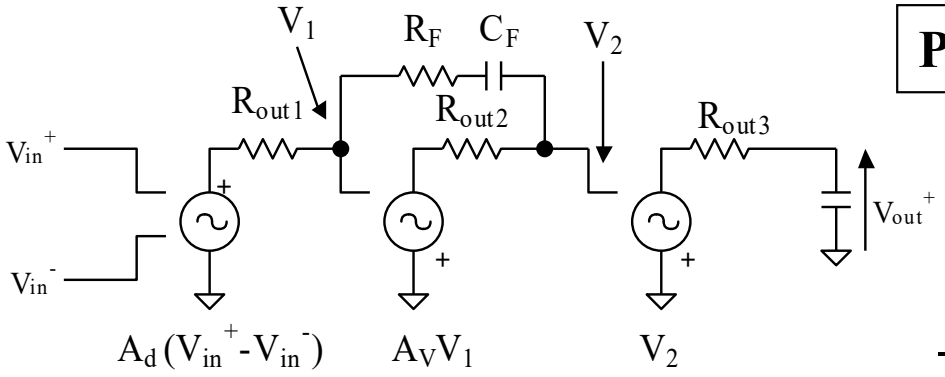


The output buffer may be omitted to reduce the power consumption, if the OPA drive only the capacitive load or operate with high loop gain.

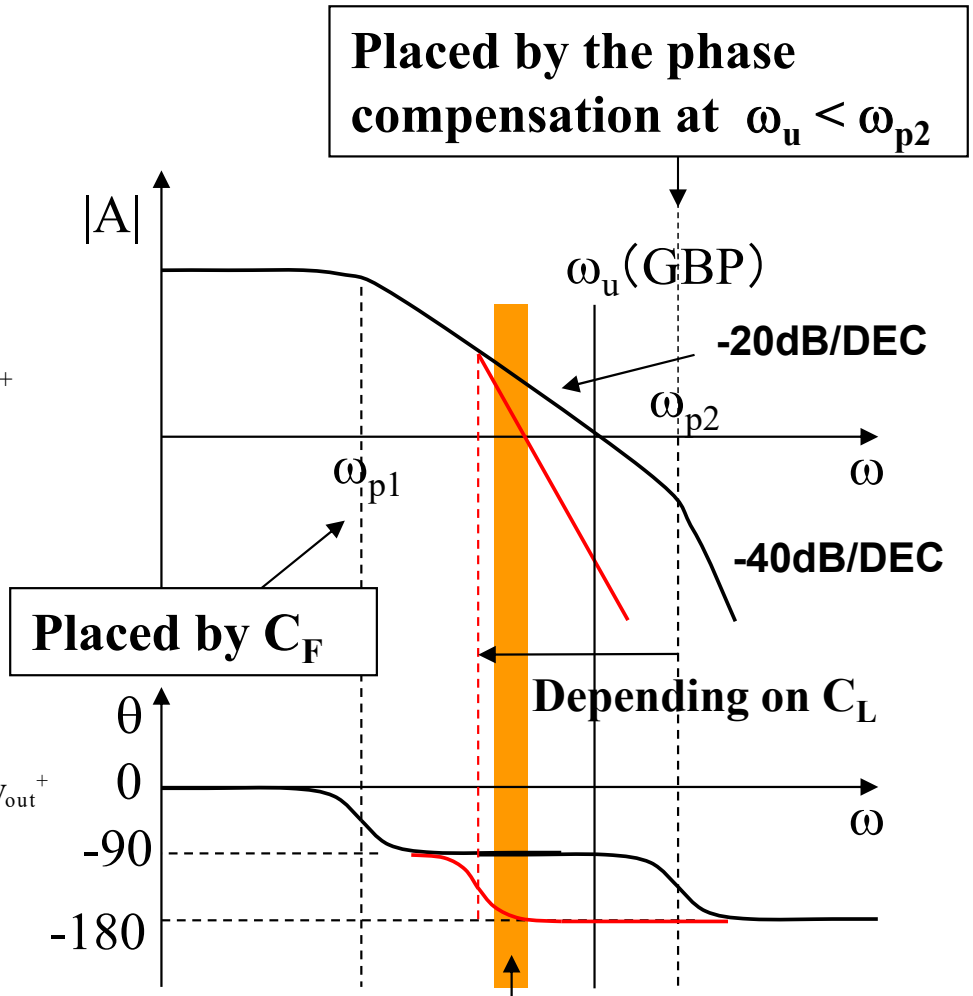
AC characteristic of OPA



Small-signal



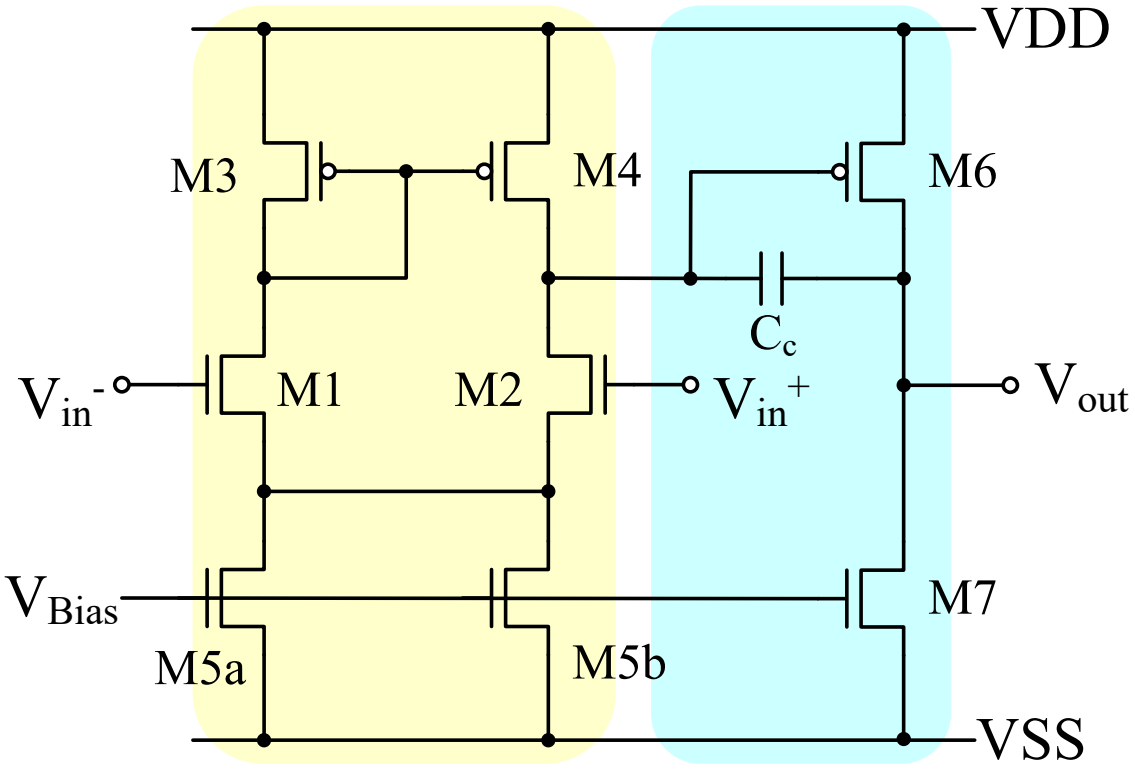
$$V_{out}^{+} = \frac{1}{1 + j\omega \cdot R_{out3} C_L} V_2 = \frac{1}{1 + j\omega / \omega_{p2}} V_2$$



The phase margin is decreased for the very large C_L.

2. Analysis of 2-stage single-end OPA

Structure of 2-stage OPA



The power consumption of impedance buffers often large. If the high load impedance is estimated, consider the unbuffered structure.

Differential amplifier CS amplifier (without the output buffer)

$$A_d = g_{m1} \cdot (r_{ds2} // r_{ds4}) \cdot g_{m6} \cdot (r_{ds6} // r_{ds7})$$

Bias current dependence of the differential gain

Differential amplifier stage

$$A_{V1} = -g_{m1} \cdot (r_{ds2} \,//\, r_{ds4})$$

$$g_{m1} = \sqrt{2\beta_1 I_{DS1}}$$

$$r_{ds2} = \frac{1}{\lambda_2 I_{DS2}} = \frac{1}{\lambda_2 I_{DS1}}$$

$$r_{ds4} = \frac{1}{\lambda_4 I_{DS4}} = \frac{1}{\lambda_4 I_{DS1}}$$

CS amplifier stage

$$A_{V2} = -g_{m6} \cdot (r_{ds6} \,//\, r_{ds7})$$

$$g_{m6} = \sqrt{2\beta_6 I_{DS6}}$$

$$r_{ds6} = \frac{1}{\lambda_6 I_{DS6}} = \frac{1}{\lambda_6 I_{DS6}}$$

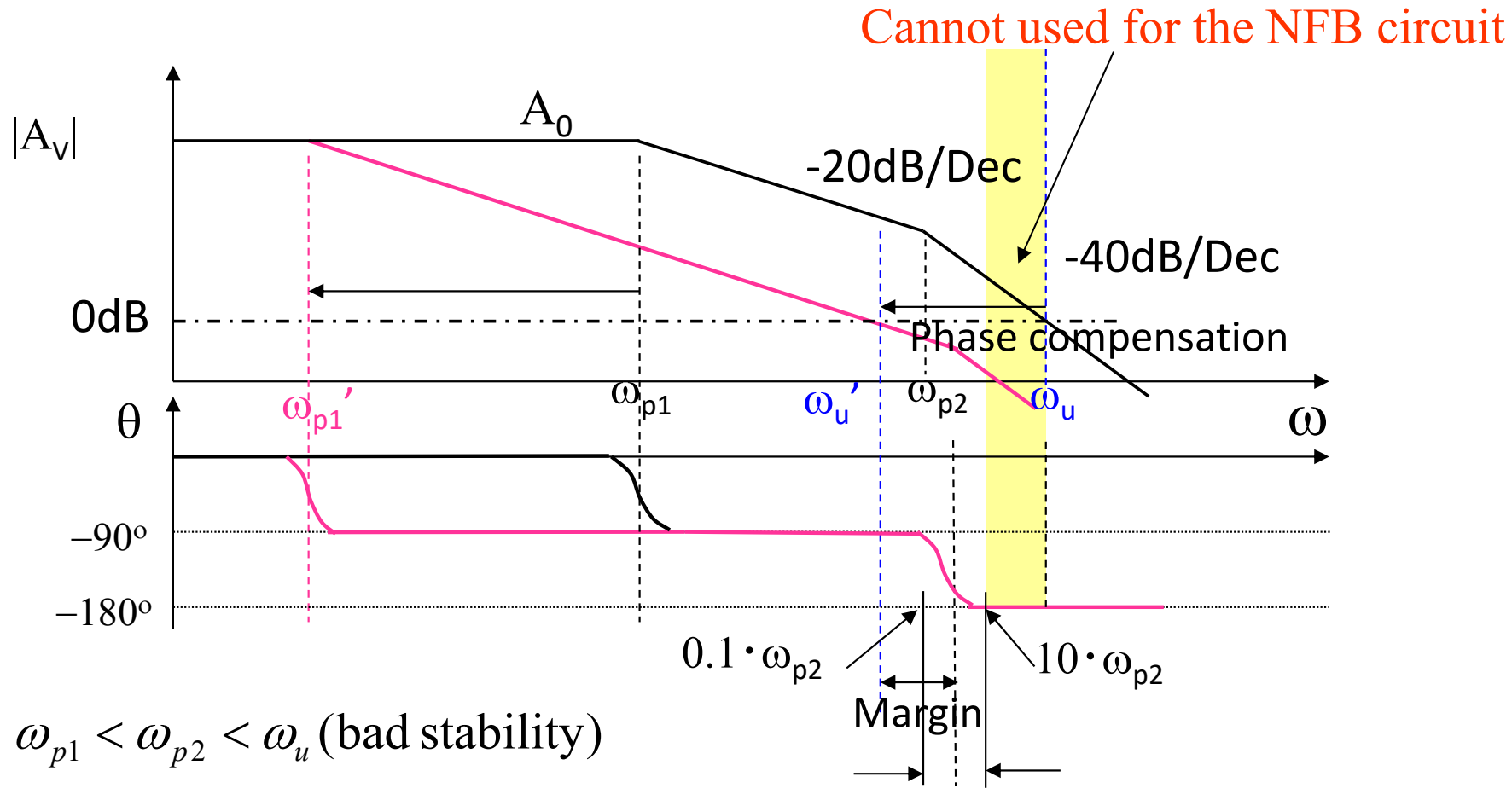
$$r_{ds7} = \frac{1}{\lambda_7 I_{DS7}} = \frac{1}{\lambda_7 I_{DS6}}$$

Total gain

$$A_d = A_{V1} A_{V2} = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})} = \frac{2\sqrt{\beta_1 \beta_6}}{(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)} \frac{1}{\sqrt{I_{DS1} I_{DS6}}}$$

Phase compensation (1)

Constraint for ω_{p2} and ω_u



$\omega_{p1} < \omega_{p2} < \omega_u$ (bad stability)

$\omega_{p1} < \omega_u < \omega_{p2}$ (good stability)

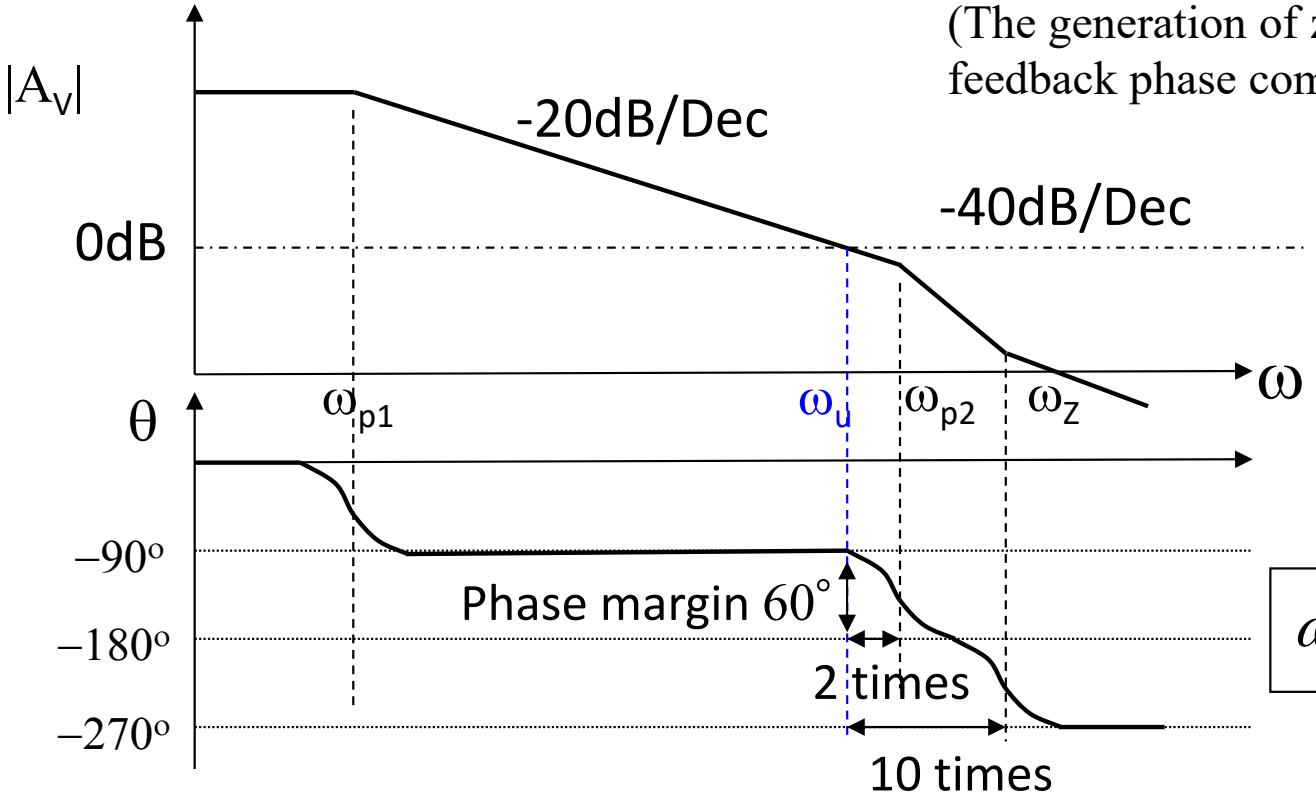
Phase compensation (2)

Constraint for ω_z and ω_u

Constraint for ω_{p2} and ω_z

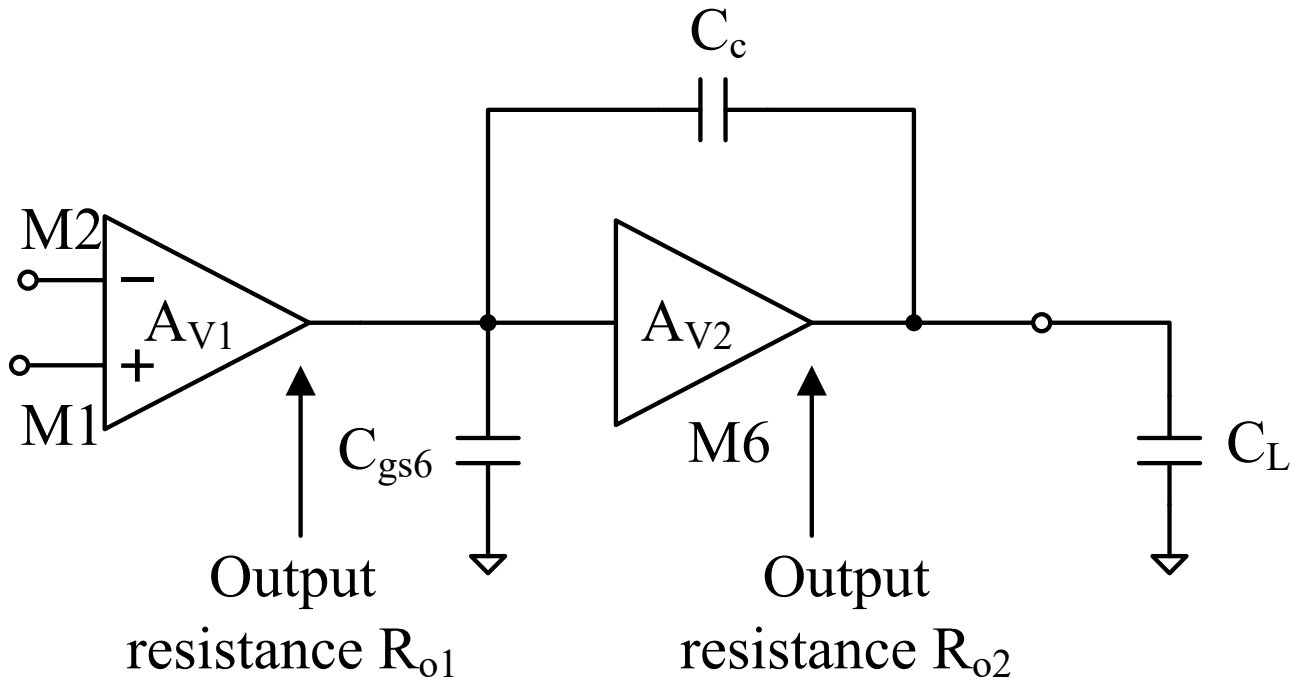
$$\begin{cases} \omega_{p2} \geq 2 \cdot \omega_u \\ \omega_z \geq 10 \cdot \omega_u \end{cases}$$

(The generation of zero is inevitable in the feedback phase compensation circuit.)



$$\omega_{p1} < \omega_u < \omega_{p2} < \omega_z$$

Miller capacitance phase compensation technique



The input parasitic capacitance of M6 is C_{gs6}, but the input capacitance of the 2nd amplifier is controlled by the Miller capacitance C_M.

$$C_M = A_{V2} \cdot C_C + C_{gs6} \approx A_{V2} \cdot C_C$$

Design of the frequency response

Pole and Zero frequency and the circuit parameters

$$\omega_{p1} \cong \frac{1}{(A_{V2}C_C)\cdot R_{o1}}$$ (Miller effect)

$$\omega_u \cong A_{V1}\cdot A_{V2}\cdot\omega_{p1} = \frac{A_{V1}}{C_C\cdot R_{o1}} = \frac{g_{m1}}{C_C}$$ (Miller effect)

$$\omega_Z \cong \frac{g_{m6}}{C_C}$$ (Feed forward through C_c)

$$\omega_{p2} \cong \frac{1}{C_L\cdot R_{o2}} \cong \frac{g_{m6}}{C_L}$$ (The output capacitance of 2nd amplifier)

In the frequency range more than ω_u, the input signal and output signal level is comparable, approximately, $A_{V2}=G_{m2}\cdot R_{o2}= -g_{m6}\cdot R_{o2} \fallingdotseq -1$.

Constraint of the phase compensation

60° Phase margin

$$\omega_{p2} > 2\omega_u$$

$$\frac{g_{m6}}{C_L} > 2\frac{g_{m1}}{C_C}$$

Separation between ω_z and ω_u

$$\omega_Z > 10\omega_u$$

$$\frac{g_{m6}}{C_C} > 10\frac{g_{m1}}{C_C}$$

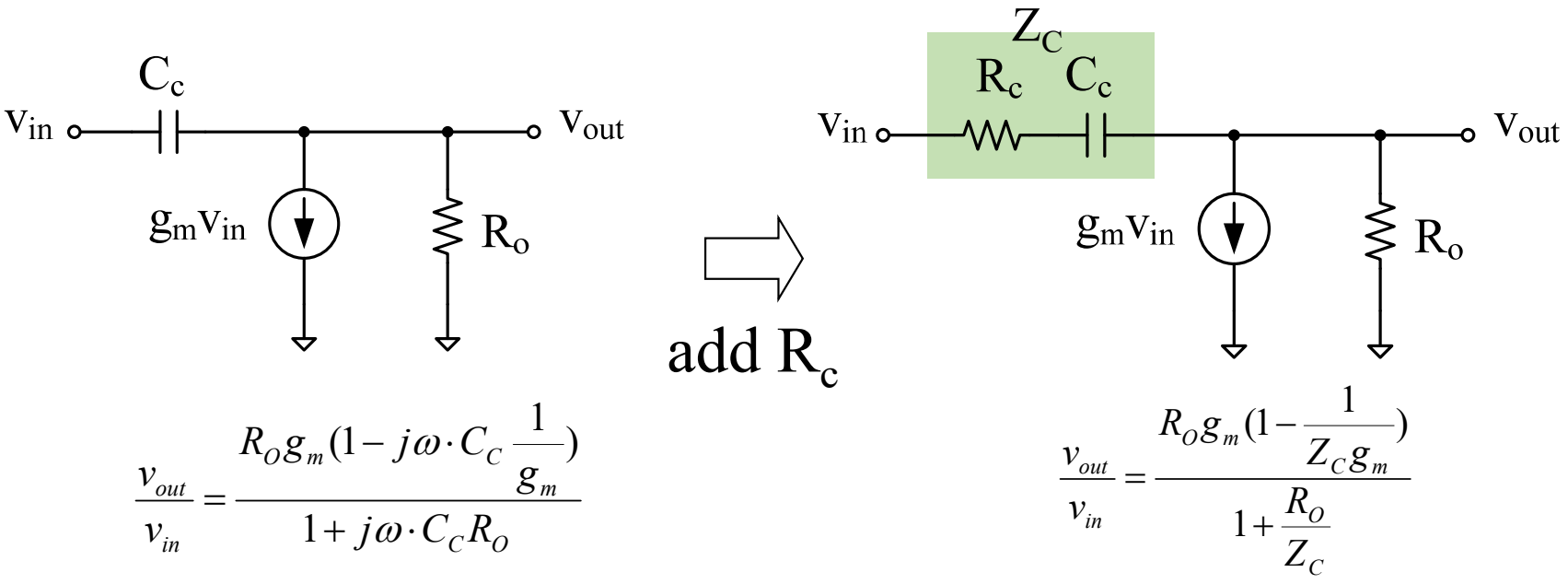
Phase compensation Constraint

$$g_{m6} \geq 10 g_{m1}$$

$$C_C \geq 0.2 C_L$$

Location of the zero (1)

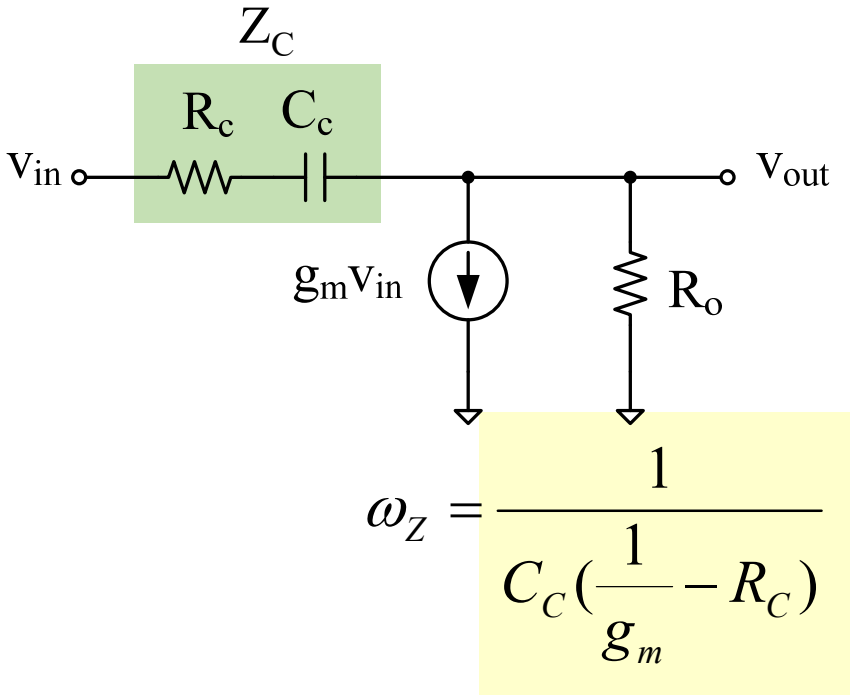
The phase compensation using C_C requires the constraint $g_{m6} > 10g_{m1}$ to remove the influence of ω_Z. this method requires the very large g_{m6}. RC phase compensation can be used to evade this problem.



$$\frac{v_{out}}{v_{in}} = \frac{R_O g_m (1 - j\omega \cdot C_C \frac{1}{g_m})}{1 + j\omega \cdot C_C R_O}$$

$$\frac{v_{out}}{v_{in}} = \frac{R_O g_m (1 - \frac{1}{Z_C g_m})}{1 + \frac{R_O}{Z_C}}$$

Location of the zero (2)



$$\omega_Z = \frac{1}{C_C\left(\frac{1}{g_m} - R_C\right)}$$

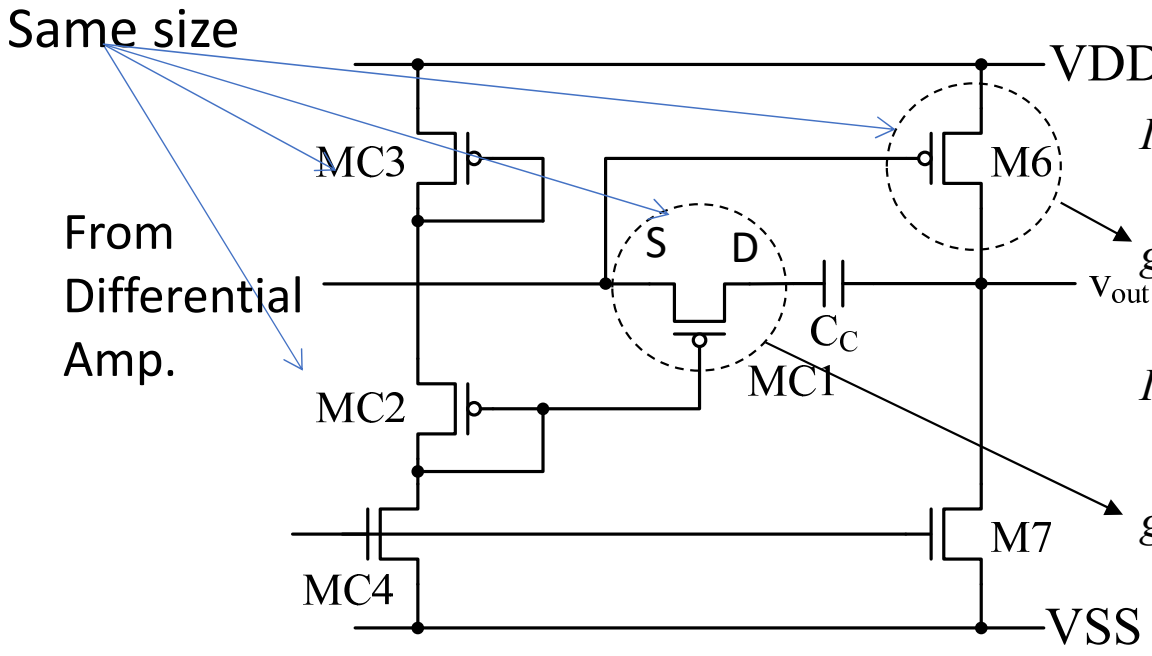
$$\frac{v_{out}}{v_{in}} = \frac{-R_O g_m\left(1 - \frac{1}{Z_C g_m}\right)}{1 + \frac{R_O}{Z_C}}$$

$$= \frac{-R_O g_m\left\{1 - j\omega \cdot C_C\left(\frac{1}{g_m} - R_C\right)\right\}}{1 + j\omega \cdot C_C(R_O + R_C)}$$

$$= \frac{-R_O g_m\{1 - j\omega/\omega_Z\}}{1 + j\omega/\omega_{p3}}$$

Method (1) : If $R_C = 1/g_m$, $\omega_Z \rightarrow \infty$ (Nulling the zero)
Method (2) : If $R_C > 1/g_m$, ω_Z is located in the left half plane (the phase turns counterclockwise.)

Practical R_c implementation by MOSFET output conductance



$$I_{DS6} = \frac{\beta_p}{2}(V_{GS6} - V_{Tp})^2$$

$$g_{m6} = \frac{\partial I_{DS6}}{\partial V_{GS6}} = \beta_p (V_{GS6} - V_{Tp})$$

$$I_{DS\_MC1} = \beta_p \{(V_{GS\_MC1} - V_{Tp}) V_{DS\_MC1} - \frac{1}{2} V_{DS\_MC1}^2\}$$

$$g_{ds\_MC1} = \left.\frac{\partial I_{DS\_MC1}}{\partial V_{DS\_MC1}}\right|_{V_{DS\_MC1}=0} = \beta_p (V_{GS\_MC1} - V_{Tp})$$

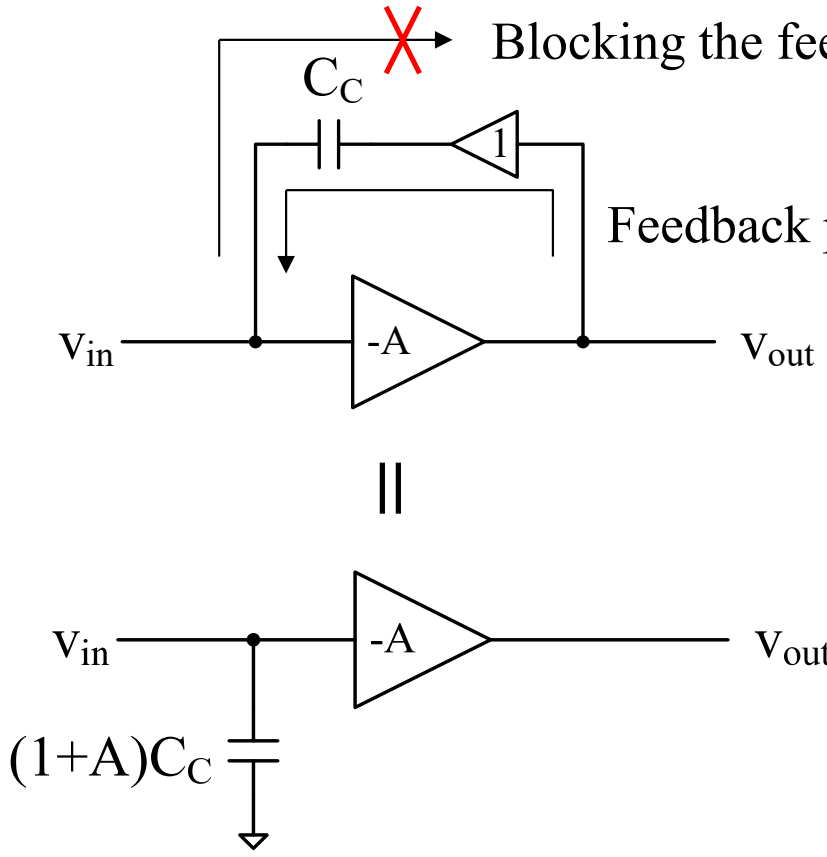
M7 and MC4 are the same size.
M6, MC1, MC2, and MC3 are the same size.

$\Rightarrow$

$$V_{GS\_MC3} + V_{GS\_MC2} = V_{GS6} + V_{GS\_MC1}$$
$$V_{GS\_MC1} = V_{GS\_MC3} + V_{GS\_MC2} - V_{GS6} = V_{GS6} + V_{GS6} - V_{GS6} = V_{GS6}$$

$g_{m6} = g_{ds\_MC1}$, $\omega_z \rightarrow \infty$ (see slide 14)

Indirect phase compensation (1)



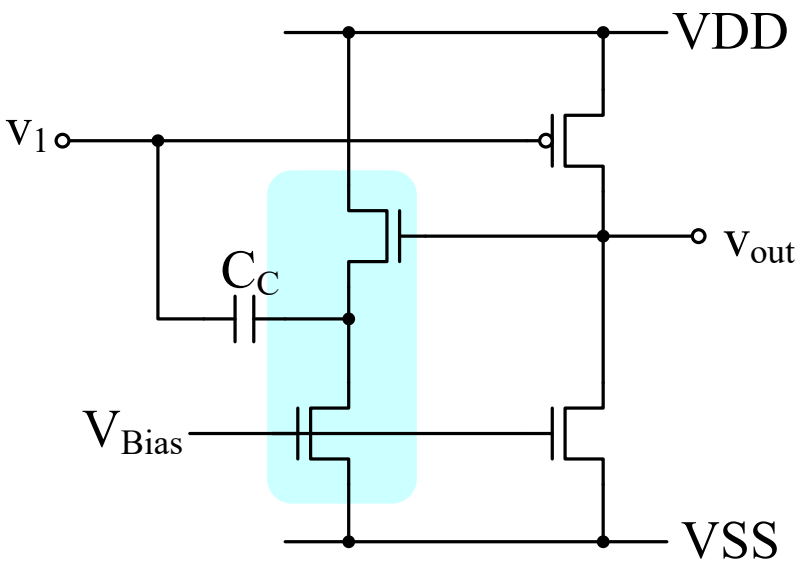
$$i_{in} = j\omega \cdot C(v_{in} - v_{out})$$

$$v_{out} = -A \cdot v_{in}$$

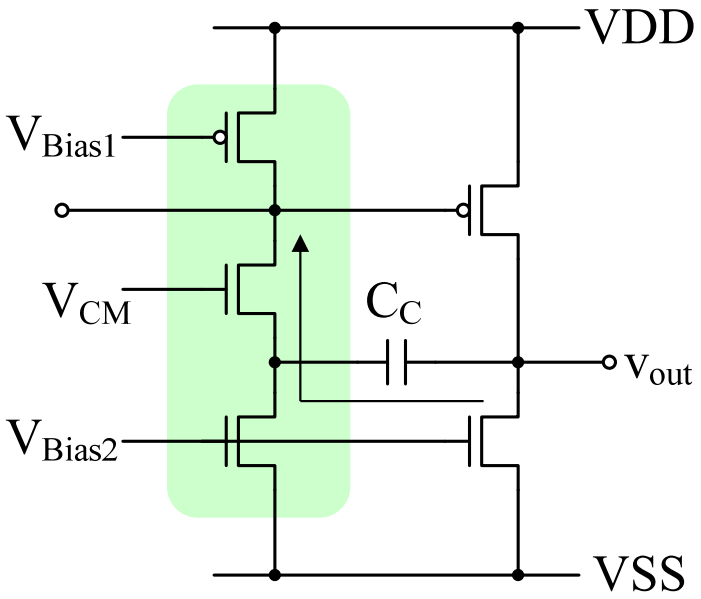
$$\frac{i_{in}}{v_{out}} = j\omega \cdot C(1 + A)$$

Indirect phase compensation (2)

Source follower feedback buffer



Common-gate feedback buffer



Advantages:

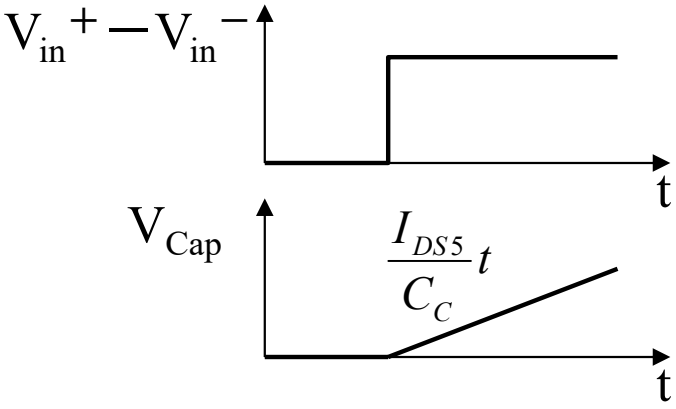
- High SR, High ω_{p2}, High ω_u, small C_c

Disadvantage:

- Additional power consumption

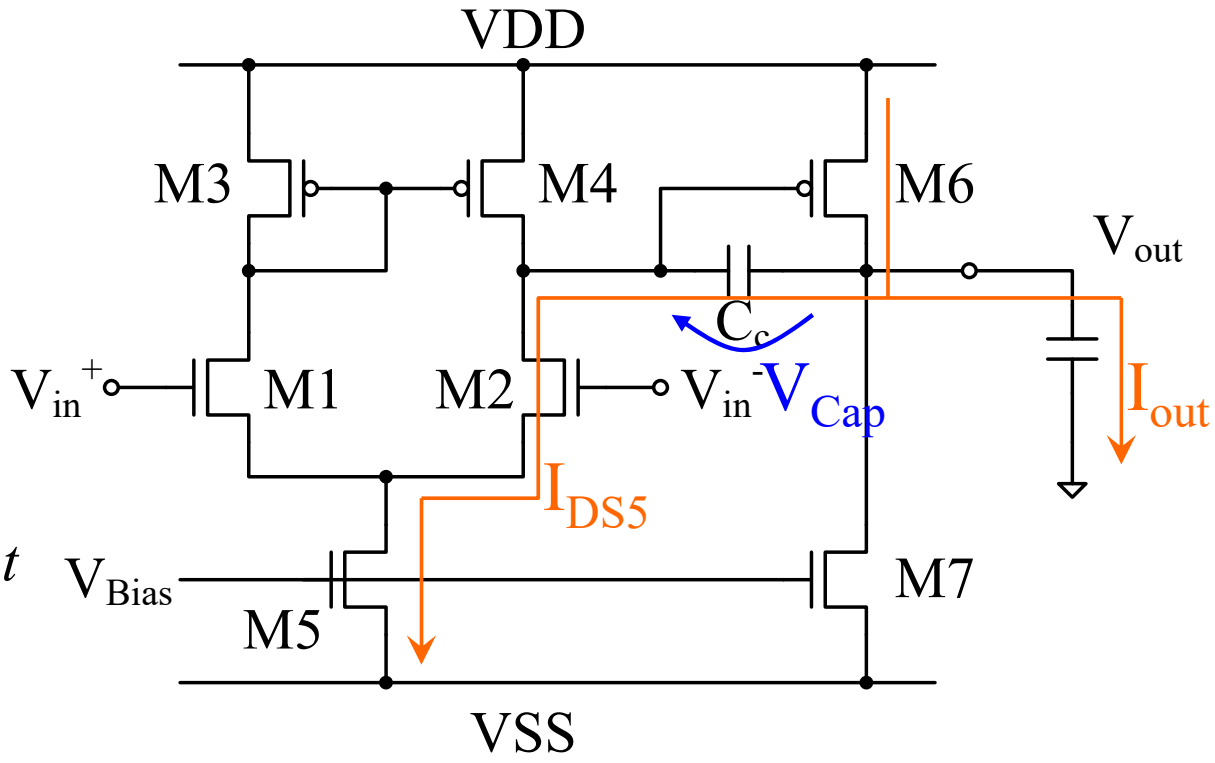
3. Design of 2-stage single-end OPA

I_{SS} and SR



$$V_{Cap} = \frac{1}{C_C}\int I_{DS5}dt = \frac{I_{DS5}}{C_C}\cdot t$$

$$SR = \frac{I_{DS5}}{C_C}$$



SR is limited by the current I_{SS} (I_{DS5}) and I_{out}.

Saturation of M4 (1)

$$V_{DS3} \geq V_{GS3} - V_{Tp} = \Delta_{OV3}$$

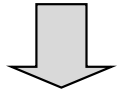
M3 always operates in the saturation region.

$$V_{DS4} = V_{GS6}$$

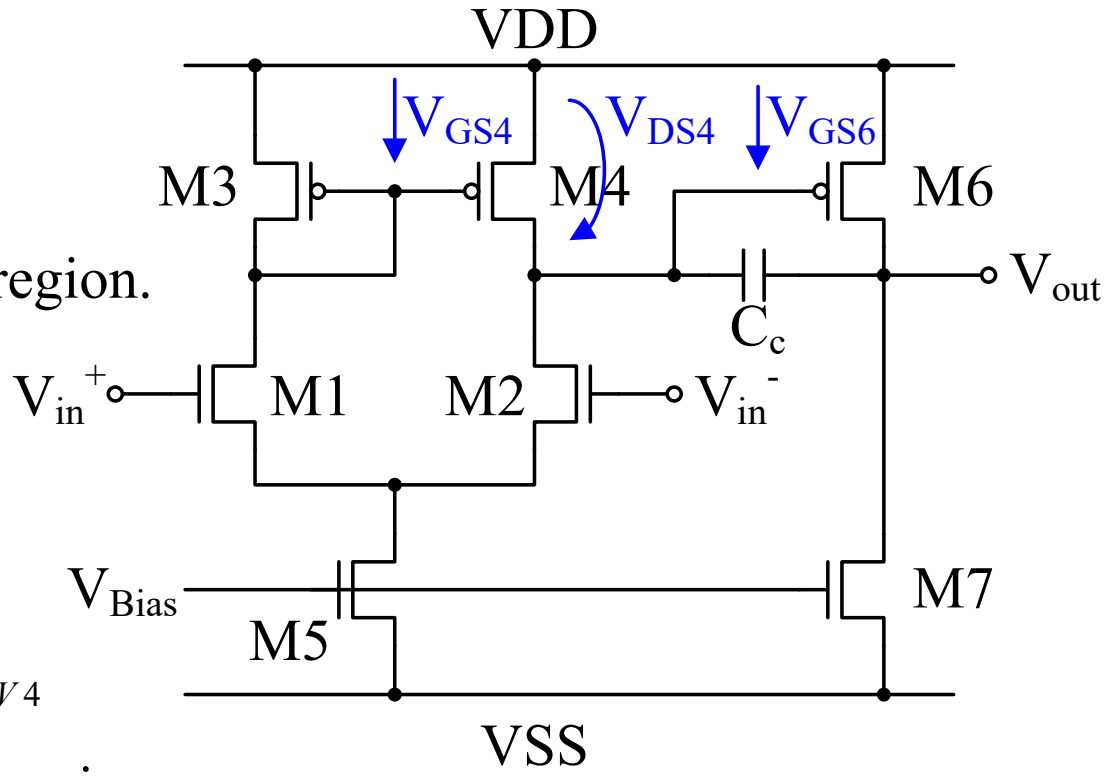
If $V_{GS4} = V_{GS6}$,

$$V_{DS4} = V_{GS6} = V_{GS4} \geq V_{GS4} - V_{Tp} = \Delta_{OV4}$$

M4 always operates in the saturation region.



MOSFET size should be optimized for $V_{GS4} = V_{GS6}$.



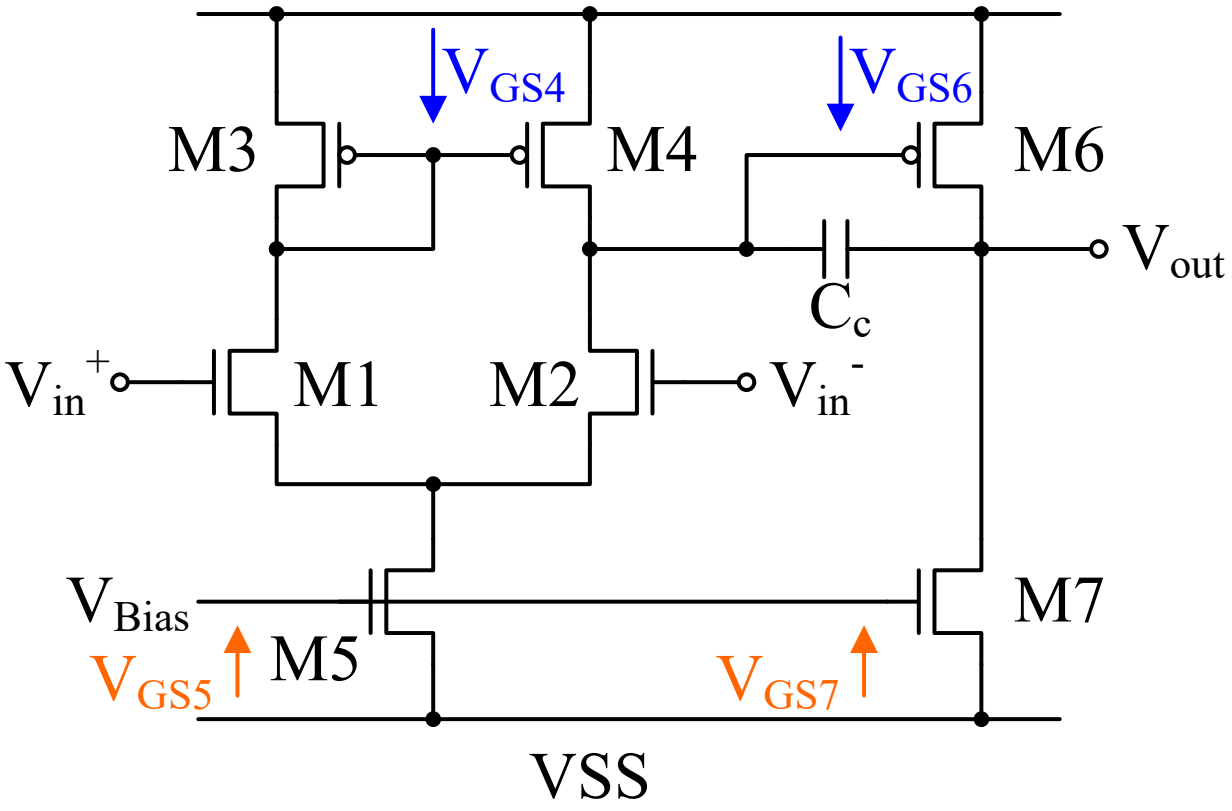
Saturation of M4 (2)

If $V_{GS4} = V_{GS6}$,

$$\frac{I_{DS6}}{I_{DS4}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}$$

$$V_{GS5} = V_{GS7}$$

$$\frac{I_{DS7}}{I_{DS5}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$



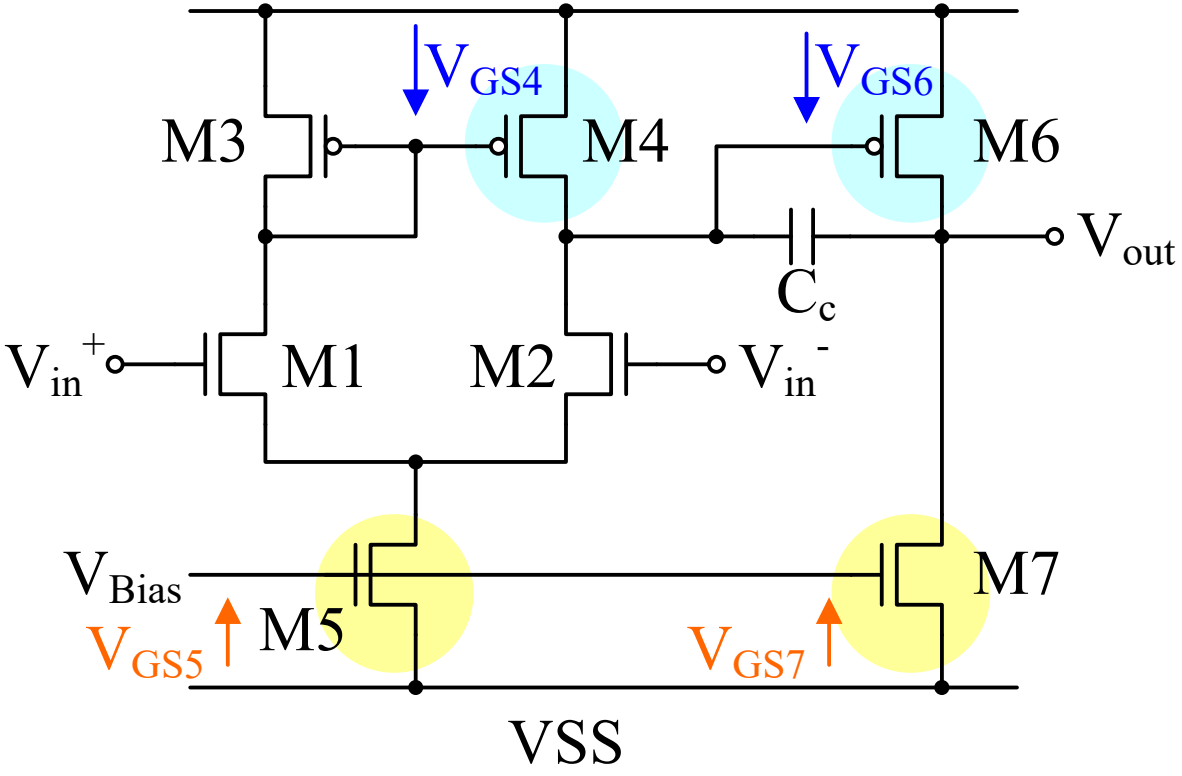
Saturation of M4 (3)

$$\begin{cases} I_{DS6} = I_{DS7} \\ I_{DS5} = 2I_{DS4} \end{cases}$$

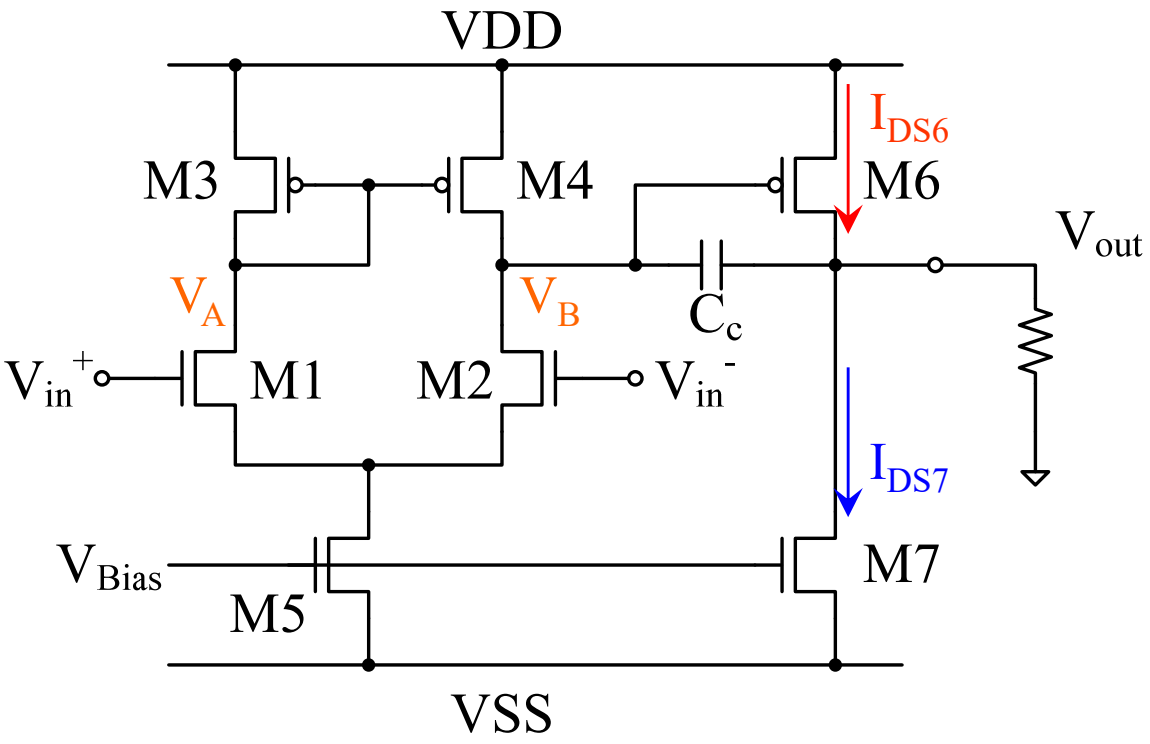
$$\frac{I_{DS6}}{I_{DS4}} = 2\frac{I_{DS7}}{I_{DS5}}$$

Saturation condition of M4

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$



Systematic offset (1)



Systematic offset
- Current balance of M6 and M7

Random offset
- Process variation of V_T

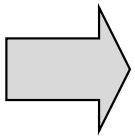
When $V_A = V_B$ (differential input = 0),
the output current = 0 or $I_{DS6} = I_{DS7}$.

Systematic offset (2)

$$\begin{cases} I_{DS3} = \dfrac{\beta_3}{2}(V_A - V_{Tp})^2 \\ I_{DS5} = \dfrac{\beta_5}{2}(V_{Bias} - V_{Tn})^2 \\ I_{DS6} = \dfrac{\beta_6}{2}(V_B - V_{Tp})^2 \\ I_{DS7} = \dfrac{\beta_7}{2}(V_{Bias} - V_{Tn})^2 \end{cases}$$

When $V_A = V_B$,

$$\begin{cases} I_{DS6} = I_{DS7} \leftarrow \text{slide 23} \\ I_{DS3} = \dfrac{I_{DS5}}{2} \end{cases}$$



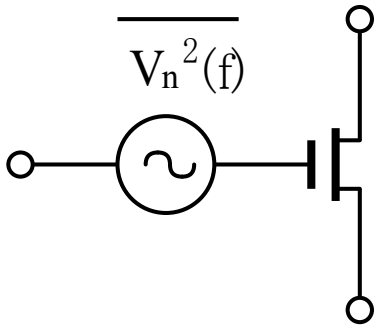
$$\frac{\beta_6}{\beta_3} = 2\frac{\beta_7}{\beta_5}$$

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$

This constraint is same as the saturation constraint of M4.

Input-referred noise (1)

Channel noise model of MOSFET



Thermal noise Flicker noise

$$\overline{V_n^2(f)} = 4kT\gamma \frac{g_{ds}}{g_m^2} + \frac{K_{p/n}}{WLC_{OX}^{\ 2}} \frac{1}{f} \qquad (V^2/Hz)$$

$$\begin{cases} \gamma = 2/3 & \text{(Long Channel)} \\ 1 & \text{(Short Channel)} \end{cases}$$

$$\begin{cases} K_p \cong 10^{-24} & (V^2/F) \\ K_n \cong 10^{-23} & (V^2/F) \end{cases}$$

The channel noise is observed in the output terminal, but the noise PSD is normally described as an input-referred noise PSD.

NOTE: Large L is better for the low noise amplifier, because of large L*W.

Input-referred noise (2)

Intrinsic noise density of the differential amplifier

Thermal noise $\overline{V_n^2(f)} = 4kT\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right)$ (Total noise from M1 and M3)

Flicker noise $\overline{V_n^2(f)} = \frac{K_n}{W_1 L_1 C_{OX}^{\ 2}}\left(1 + \frac{K_p}{K_n}\frac{W_1 L_1}{W_3 L_3}\right)\frac{1}{f}$

NOTE: Assuming that the differential pair consists n-ch MOFET and current mirror load consists p-ch MOSFETs.

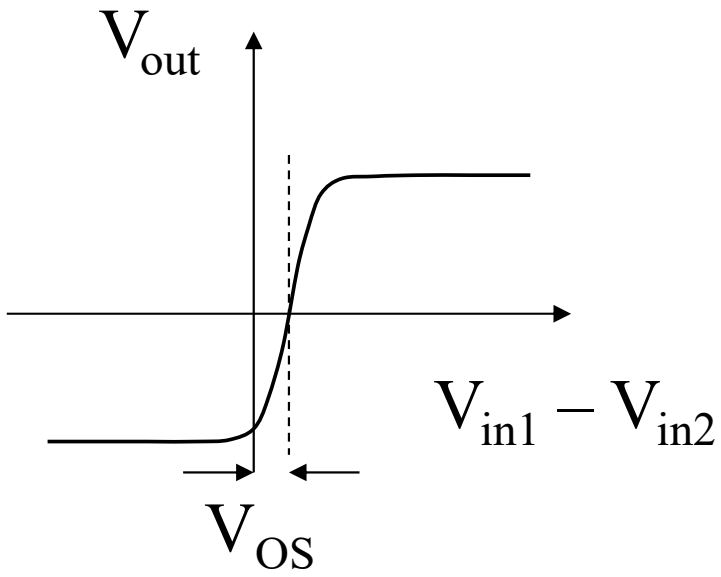
Mismatch of MOSFETs by the process variation

$$V_{OS\_1-2} = V_{GS1} - V_{GS2}$$

$$= V_{Tn1} + \sqrt{\frac{I_{DS5}}{\beta_1}} - V_{Tn2} - \sqrt{\frac{I_{DS5}}{\beta_2}}$$

$$= (V_{Tn1} - V_{Tn2}) + \sqrt{\frac{I_{DS5}}{\beta_1}}[1 - \sqrt{\frac{\beta_1}{\beta_2}}]$$

$$\cong (V_{Tn1} - V_{Tn2}) - \frac{1}{2}\sqrt{\frac{I_{DS5}}{\beta_1}}[\frac{\beta_1 - \beta_2}{\beta_1}]$$



$$= \Delta V_{Tn1-2} - \frac{V_{GS1} - V_{Tn1}}{2}[\frac{\Delta\beta}{\beta_1}]_{1-2} = \Delta V_{Tn1-2} - \frac{\Delta_{OV1}}{2}[\frac{\Delta\beta}{\beta_1}]_{1-2}$$

$$V_{OS\_3-4} = V_{GS3} - V_{GS4}$$

$$\cong \Delta V_{Tn3-4} - \frac{V_{GS3} - V_{Tp3}}{2}[\frac{\Delta\beta}{\beta_3}]_{3-4} = \Delta V_{Tn3-4} - \frac{\Delta_{OV3}}{2}[\frac{\Delta\beta}{\beta_3}]_{3-4}$$

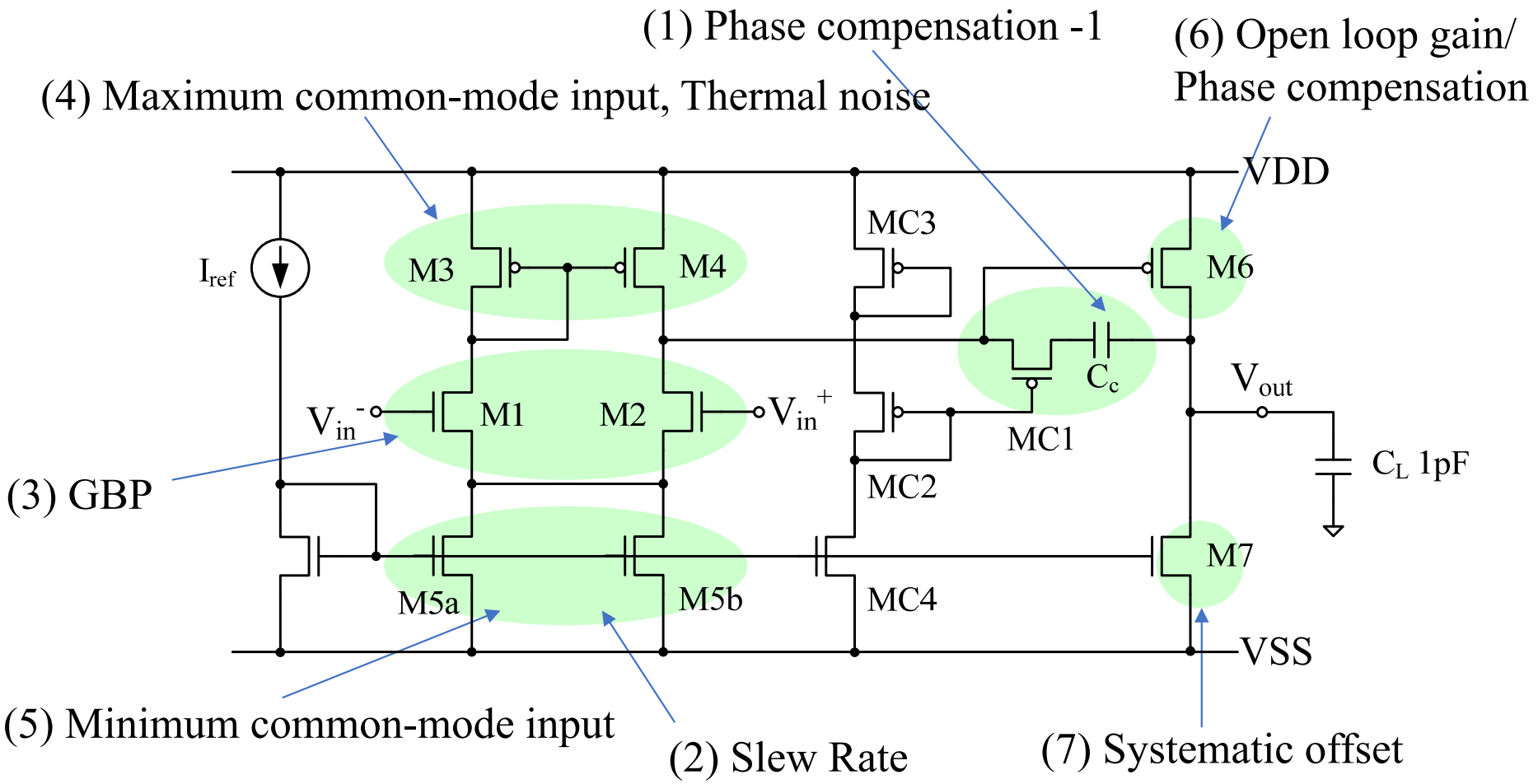
$$V_{OS} = \Delta V_{Tn1-2} - \frac{\Delta_{OV1}}{2}[\frac{\Delta\beta}{\beta_1}]_{1-2} + \frac{g_{m3}}{g_{m1}}[\Delta V_{Tn3-4} - \frac{\Delta_{OV3}}{2}[\frac{\Delta\beta}{\beta_3}]_{3-4}]$$

Optimization for the noise and process variation

- Thermal noise
  - Differential pair MOSFETs: Large W/L
  - Current mirror load MOSFETs: Small W/L
- Flicker noise
  - Differential pair MOSFETs: Large W*L
  - Current mirror load MOSFETs: Large W*L
- Mismatch offset
  - Differential pair MOSFETs: Large W, L
  - Current mirror load MOSFETs: Small W/L (Small g_{m3}/g_{m1})

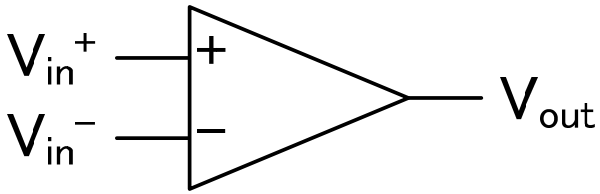
NOTE: Consider that the L and W influences the frequency response too.

Design constraints



4. The function and structure of Full-differential OPA

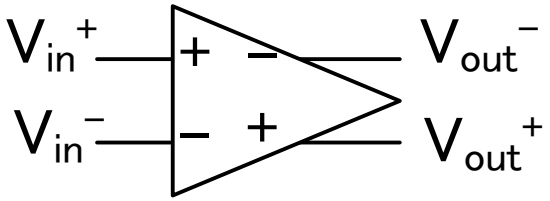
Function of a full-differential OPA



Symbol of Single-end OPA

Function

$$\begin{cases} V_{out} = A_d (V_{in}^+ - V_{in}^-) \\ \text{A}_\text{d} = \text{Differential Gain} \end{cases}$$



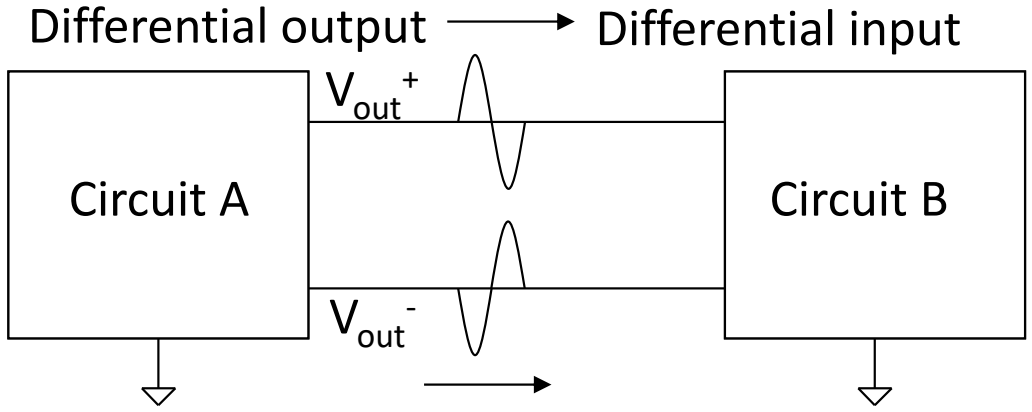
Symbol of Full-differential

$$\begin{cases} V_{out}^+ = \dfrac{A_d}{2}(V_{in}^+ - V_{in}^-) \\ V_{out}^- = -\dfrac{A_d}{2}(V_{in}^+ - V_{in}^-) \\ V_{out} = V_{out}^+ - V_{out}^- \end{cases}$$

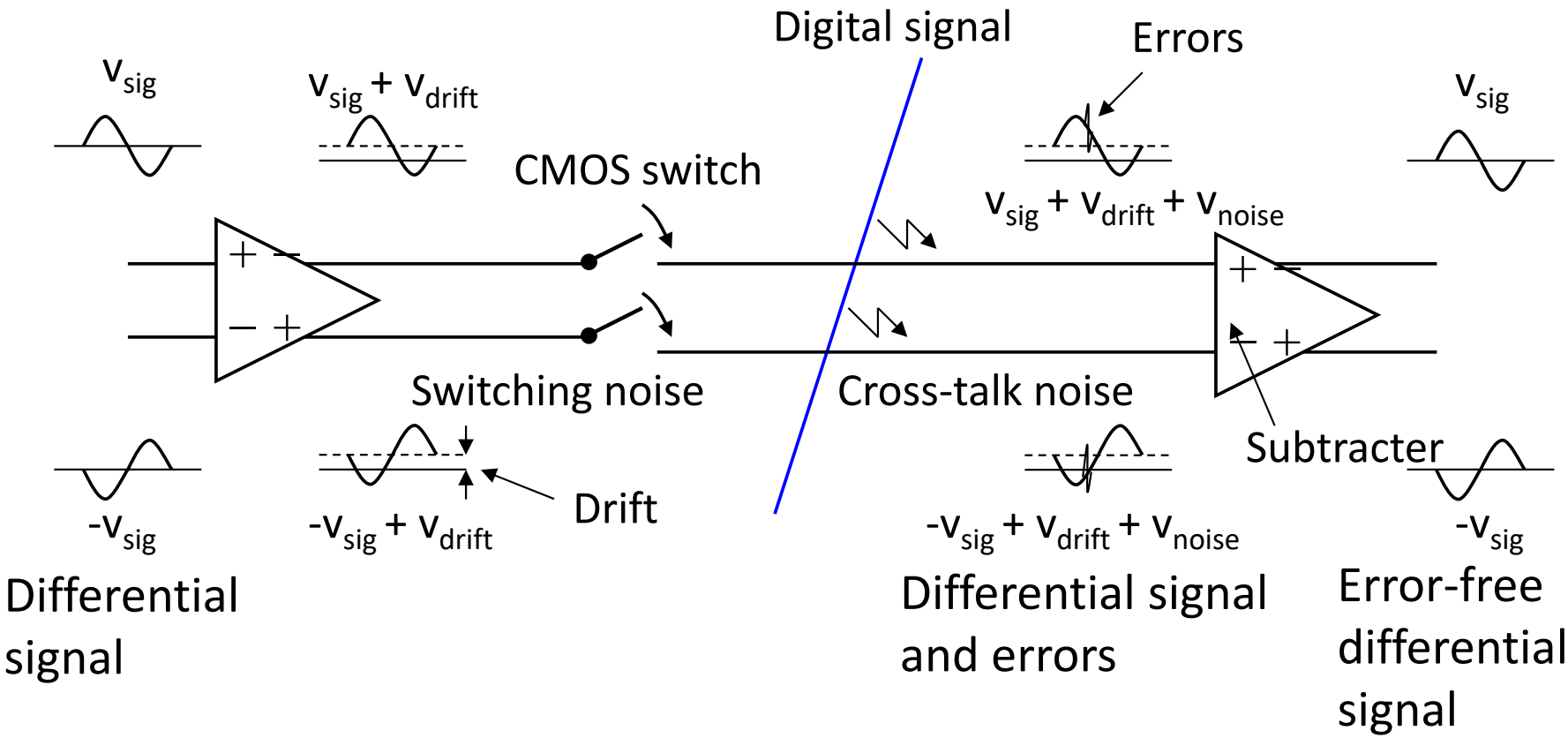
A_d = Differential Gain

Advantages of full-differential OPA

- Feature of full-differential OPAs
  - Cancellation of common-mode noise
  - Cancellation of clock feedthrough and charge injection error (essential for the discrete analog circuit)
  - Cancellation of even-order distortions of MOSFET



Cancellation of common-mode noise

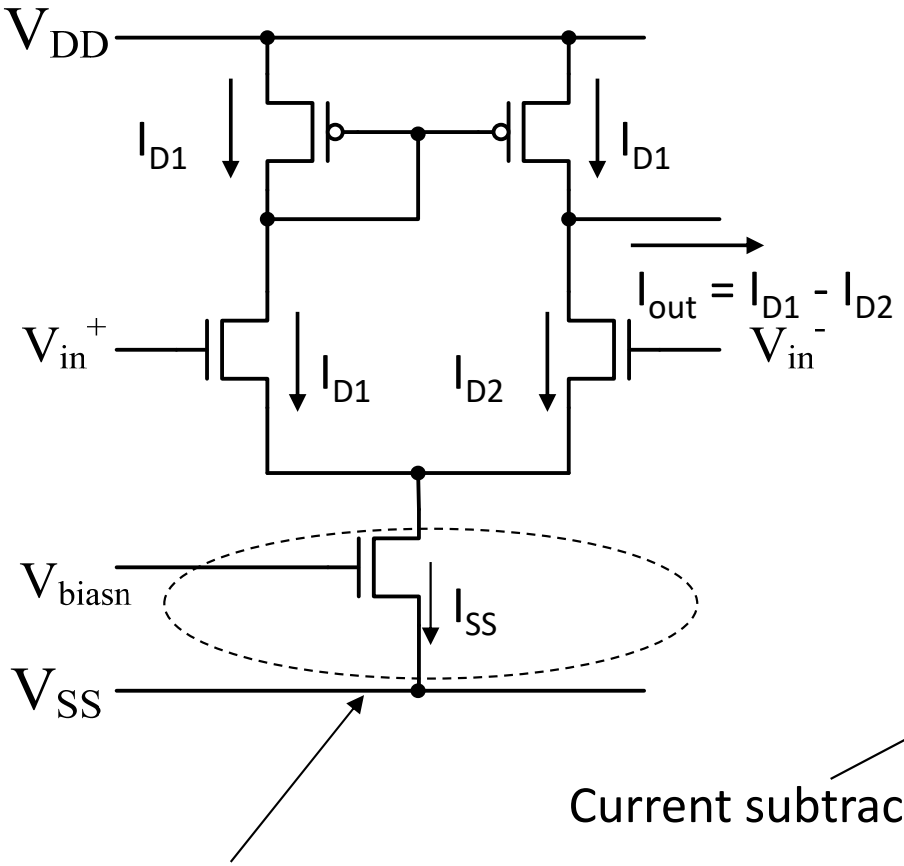


Drift : A slow shift of the common-mode voltage is often observed as a drift. The drift error occurs by a temperature change easily.

Circuit configuration of diff. amp.

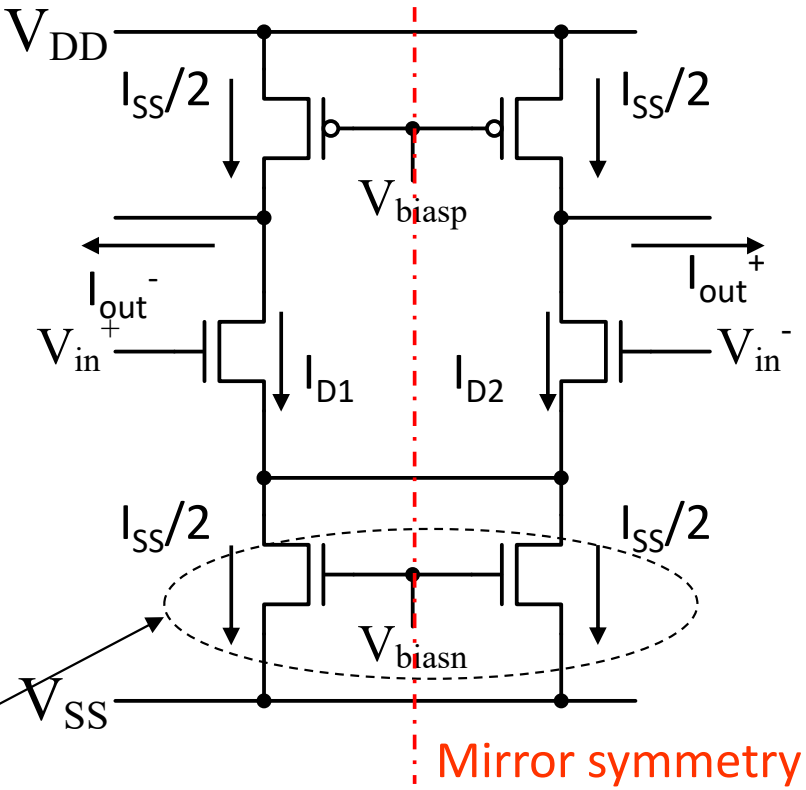
Gain = 1/2 times lower for each output port and mirror symmetry

Current mirror load



common mode rejection

Current source load



Mirror symmetry

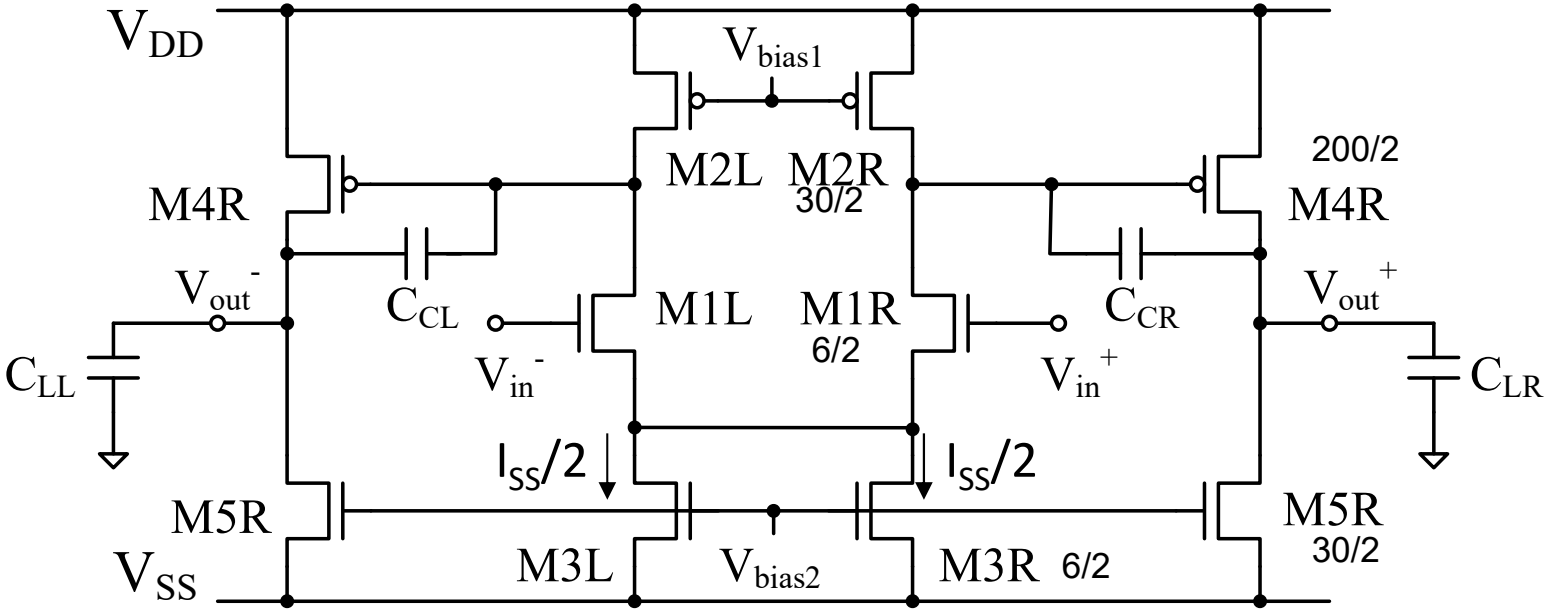
Current subtraction

$I_{SS}/2 = (I_{D1} + I_{D2})/2$

$I_{out}^+ = I_{SS}/2 - I_{D2} = (I_{D1} - I_{D2})/2$

$I_{out}^- = I_{SS}/2 - I_{D1} = (I_{D2} - I_{D1})/2$

2-stage CS full-differential OPA



$$SR = \frac{I_{SS}}{C_C}$$

$$G_0 = g_{m1}(r_{ds1} // r_{ds2}) \cdot g_{m4}(r_{ds4} // r_{ds5})$$

$$\omega_{p1} = \frac{1}{g_{m4}(r_{ds1} // r_{ds2}) \cdot (r_{ds4} // r_{ds5}) \cdot C_C}$$

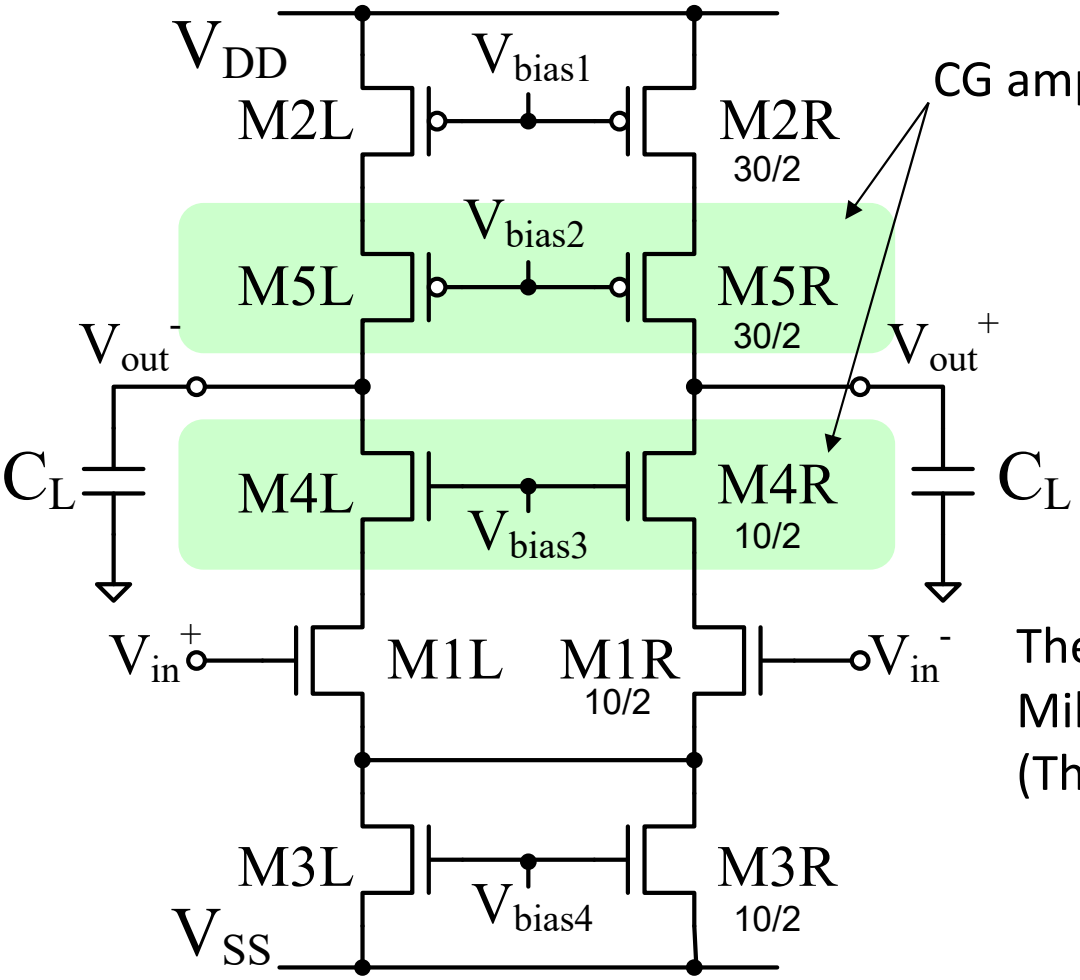
$$\omega_{p2} = \frac{g_{m4}}{C_L}$$

$$\omega_u = \frac{g_{m1}}{C_C}$$

CMRR ○
PSRR △
Gain △
Bandwidth, SR ×
Power △

NOTE: GBP increases with increasing g_{m1}, but power consumption is increased with the g_{m1} ($g_m \propto I_{DS}^{0.5}$).

Characteristic of cascode OPA



The bias current of M1 and M2 is reused for the M4 and M5.

$$SR = \frac{I_{SS}}{C_L}$$

$$G_0 = g_{m1} \cdot (g_{m4} \cdot r_{ds4} \cdot r_{ds1}) // (g_{m5} \cdot r_{ds5} \cdot r_{ds2})$$

$$\omega_{p1} = \frac{1}{(g_{m4} \cdot r_{ds4} \cdot r_{ds1}) // (g_{m5} \cdot r_{ds5} \cdot r_{ds2}) \cdot C_L}$$

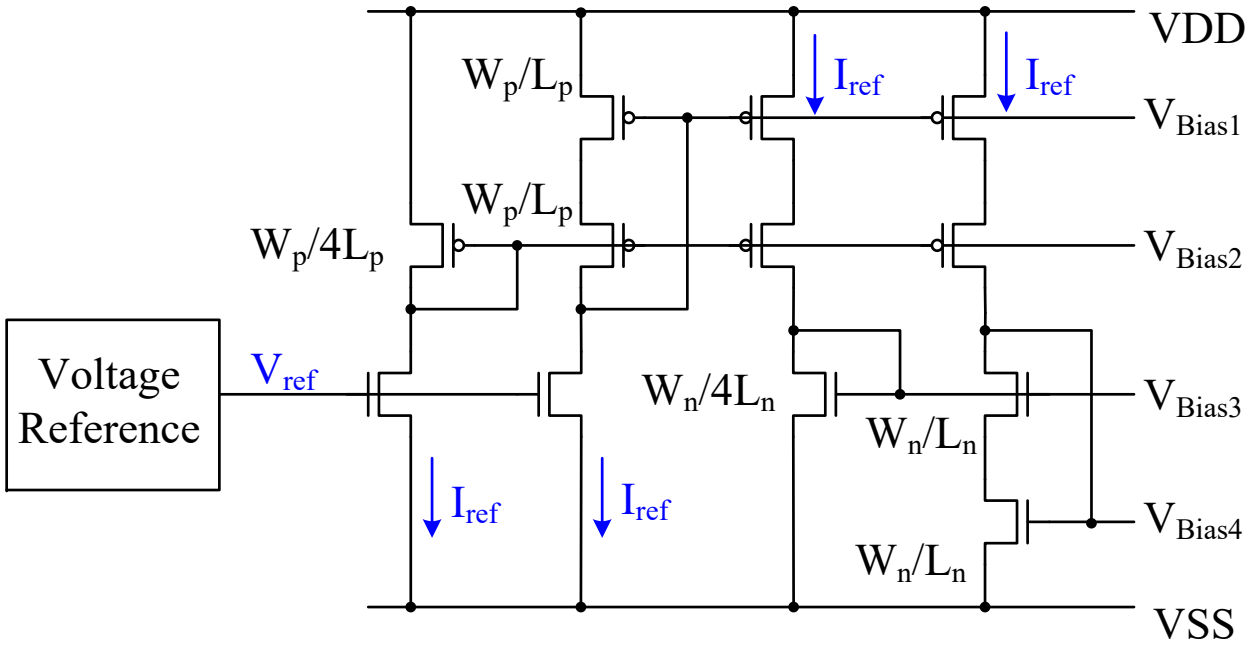
$$\omega_u = \frac{g_{m1}}{C_L}$$

The voltage gain of M1 is about unity and the Miller effect is negligible, thus, $\omega_{p2} \geqq \omega_u$
(The Phase margin depends on the C_L.)

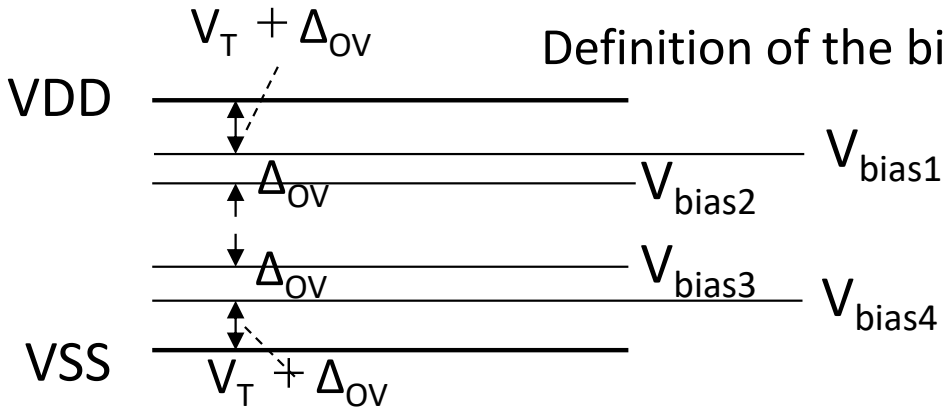
CMRR ◯
PSRR ◯
Gain ◯
Bandwidth, SR ◯ (depends on C_L)
Power ◯

Cascode bias circuit

See Chapter 4, Wide Swing cascode current mirror.



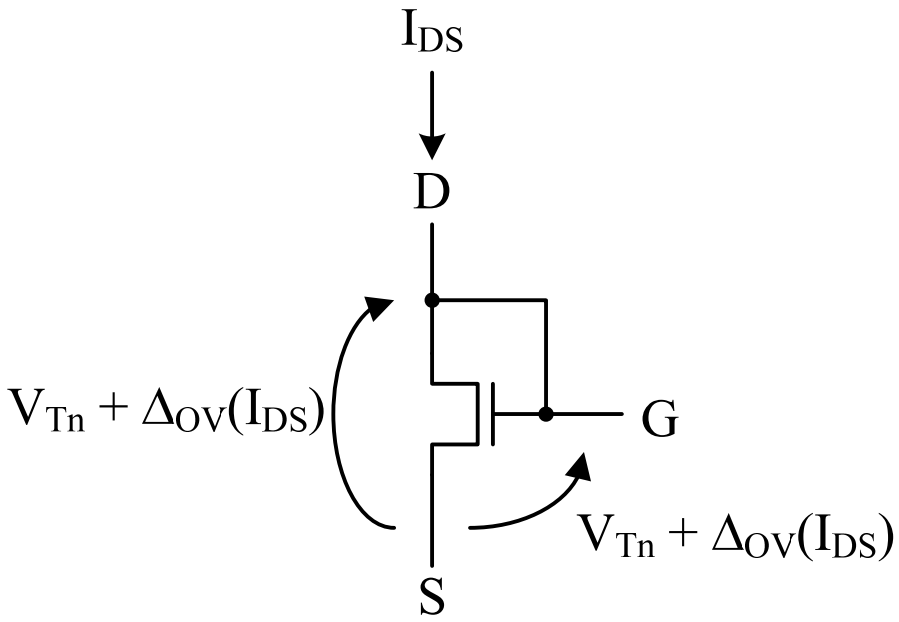
Definition of the bias voltage



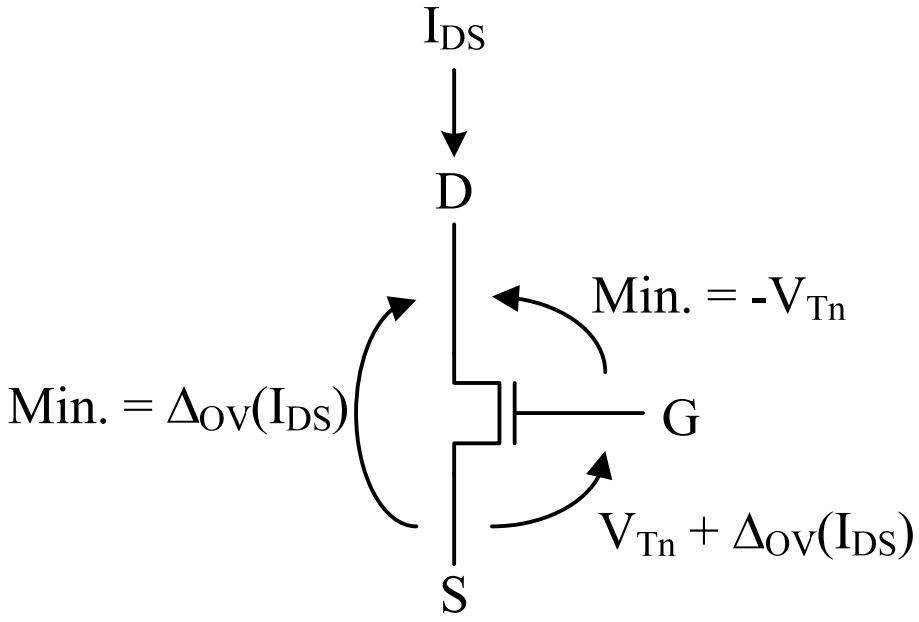
5. Folded cascode OPA

NOTE: The folded cascode OPA consumes larger bias current, but it has some advantages, such as wide input range, good stability, high gain, which these features are suitable for IP.

Calculation method of the common-mode range (remind)

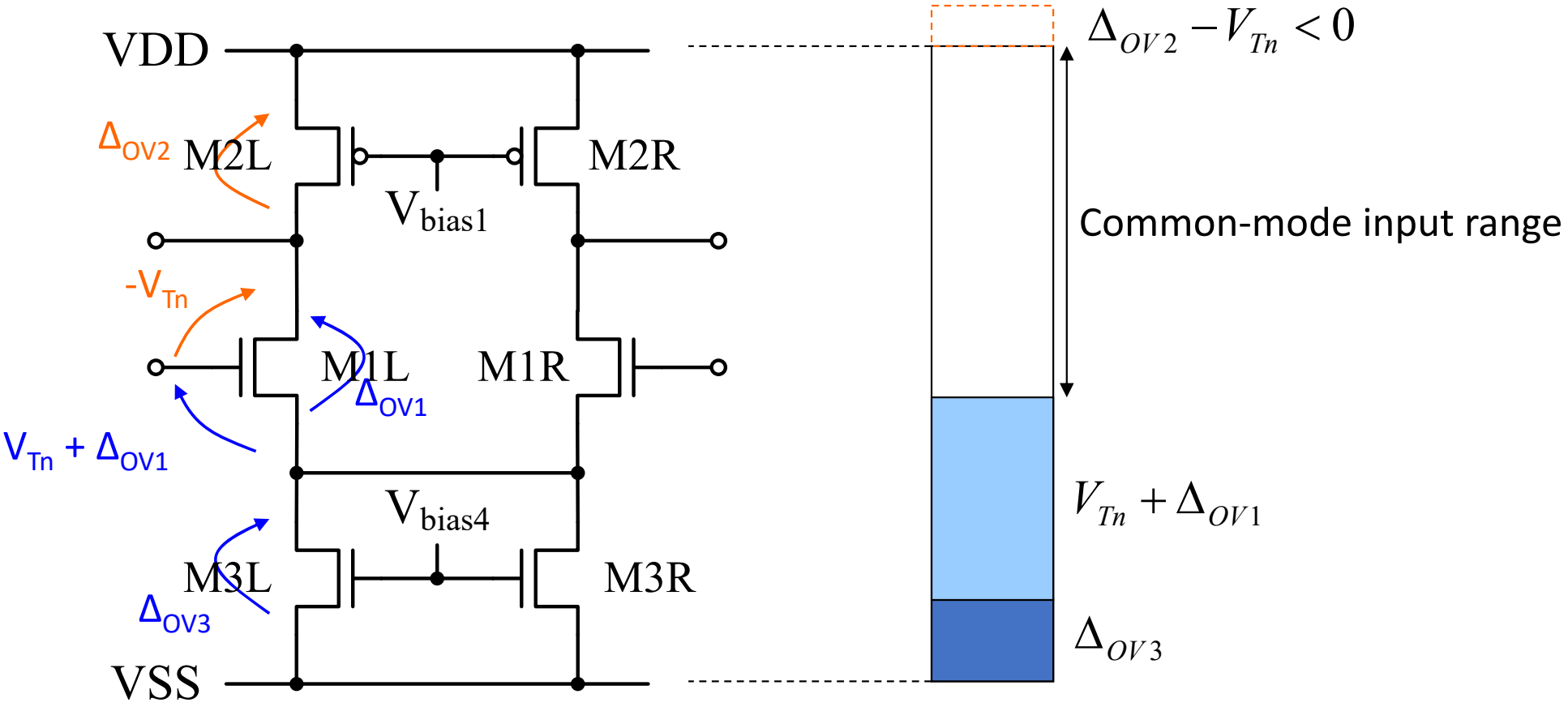


$V_{DS} = V_{GS}$

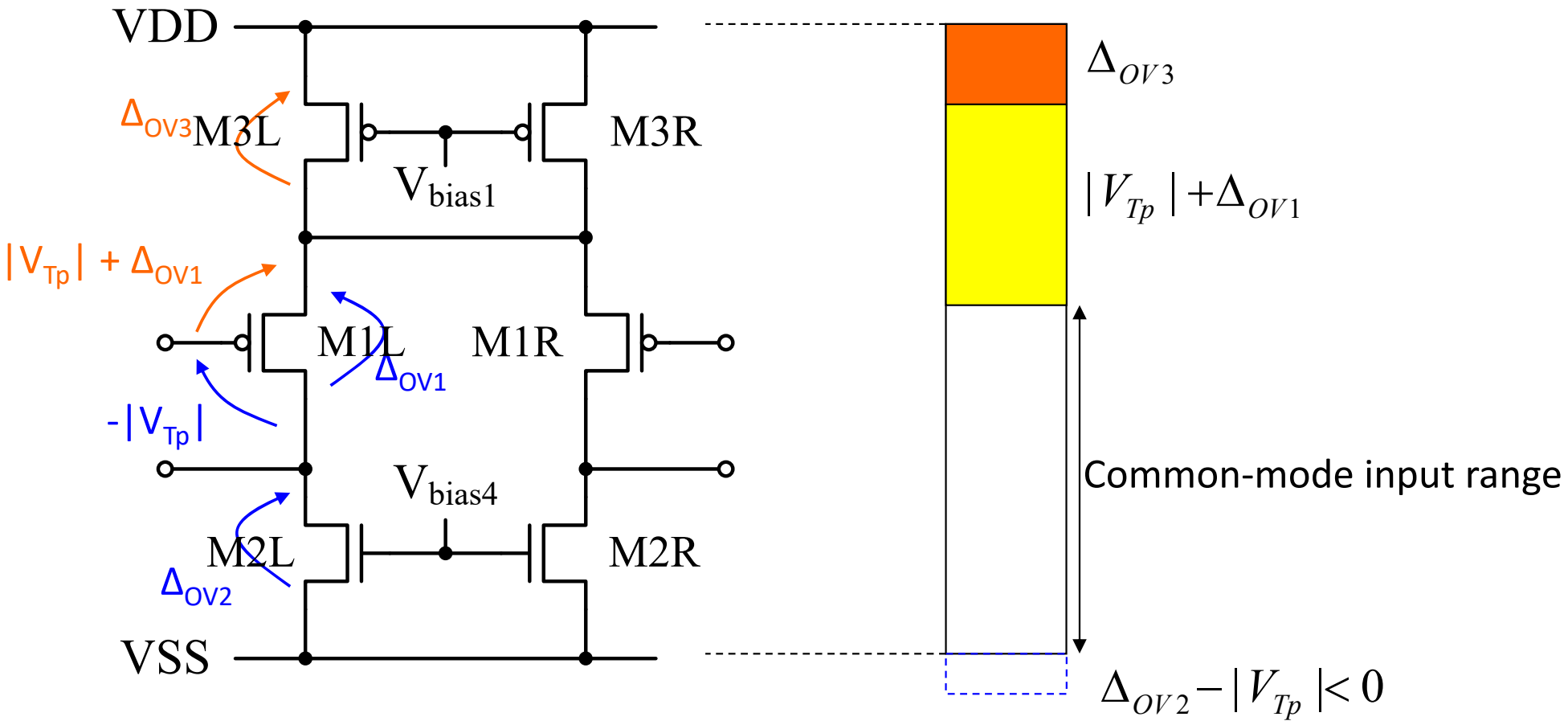


$V_{DS} = V_{GS}$

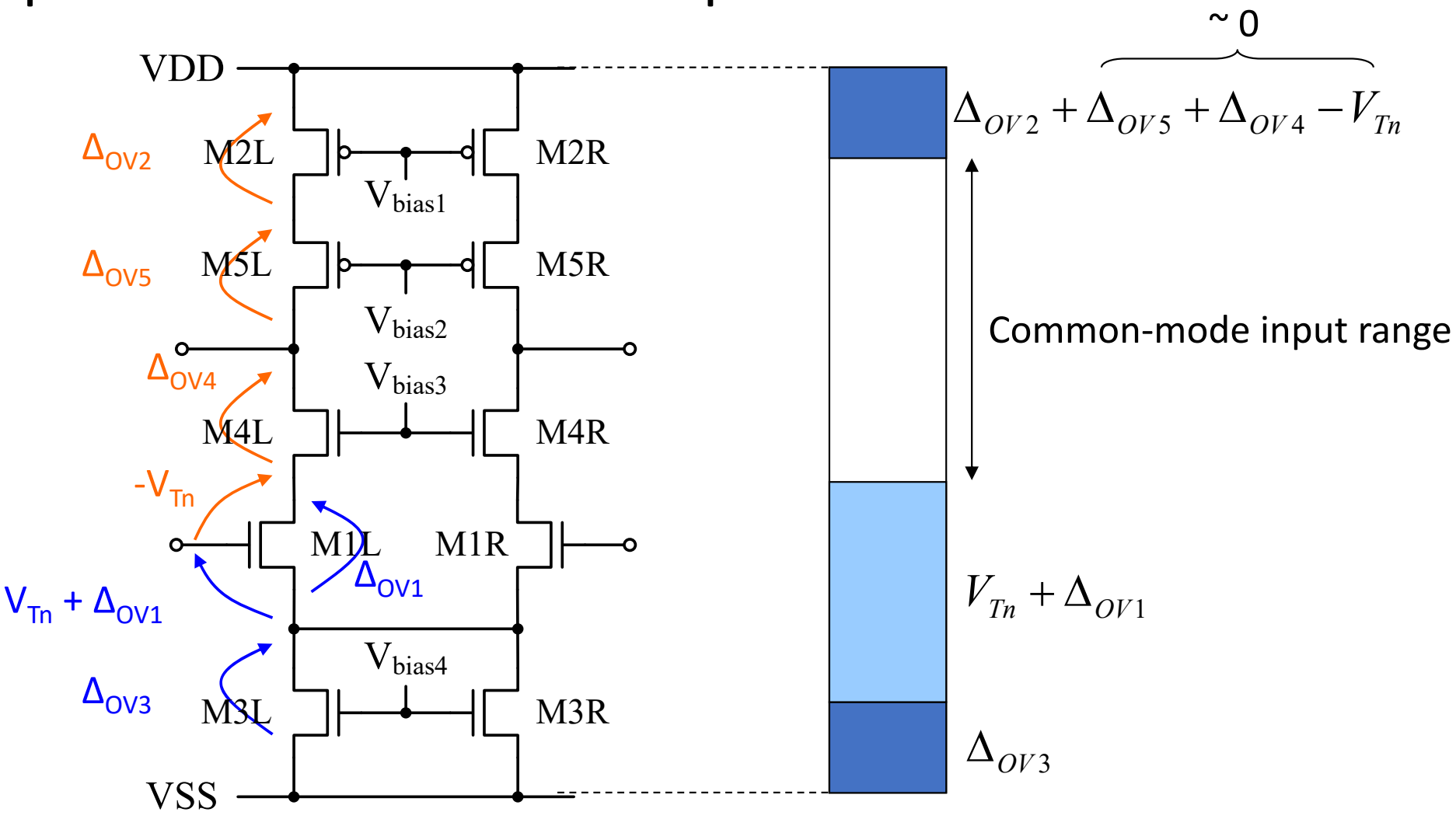
Common-mode input range of n-ch input differential amplifier



Common-mode input range of p-ch input differential amplifier



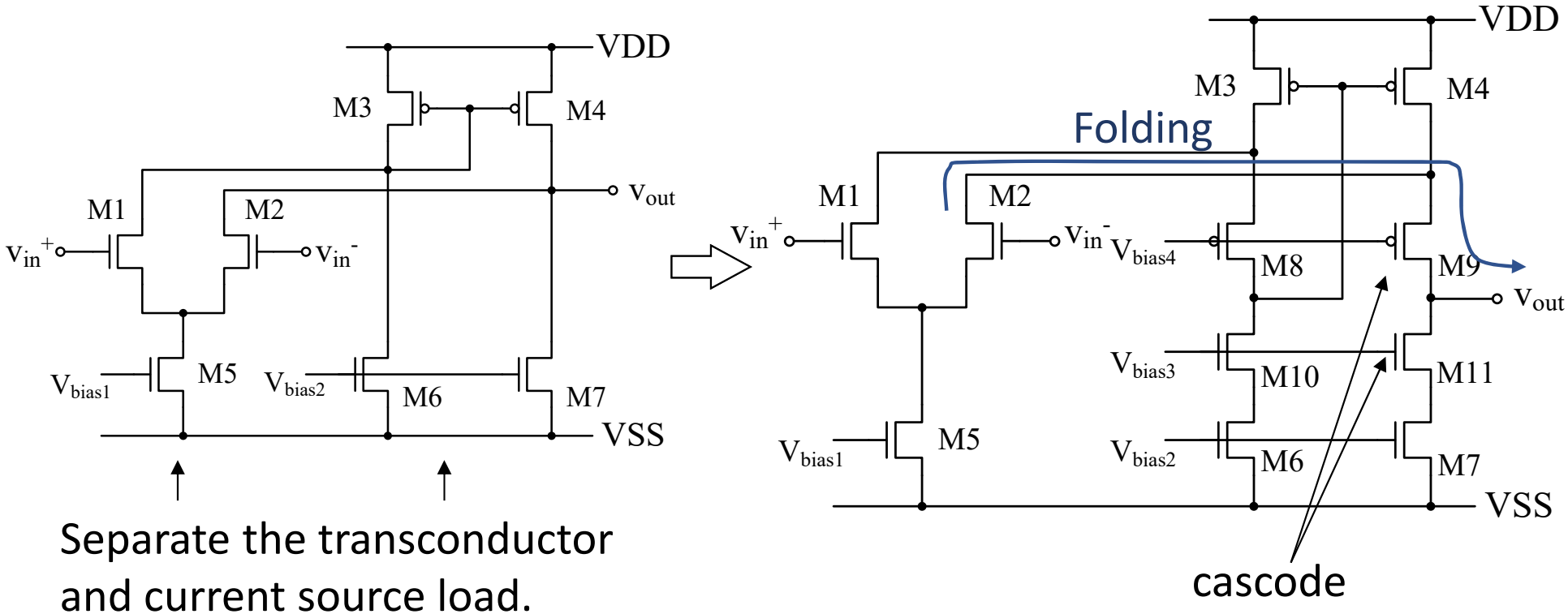
Common-mode input range of n-ch input differential amplifier



High gain, small input range, and small output swing

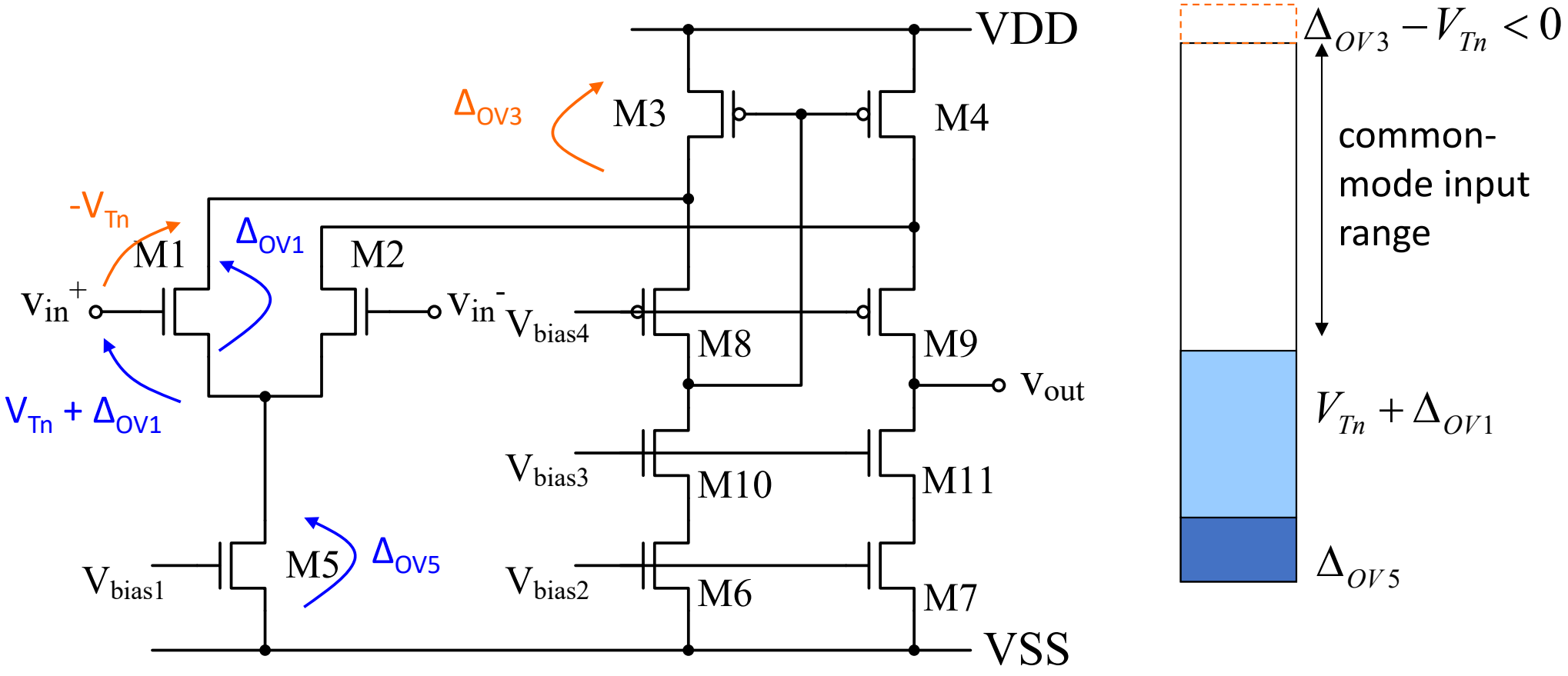
Folding technique of the current source load (single-end)

The differential pair and the current source load can be separated to enhance the signal swing and to reduce the bias voltage tolerances.

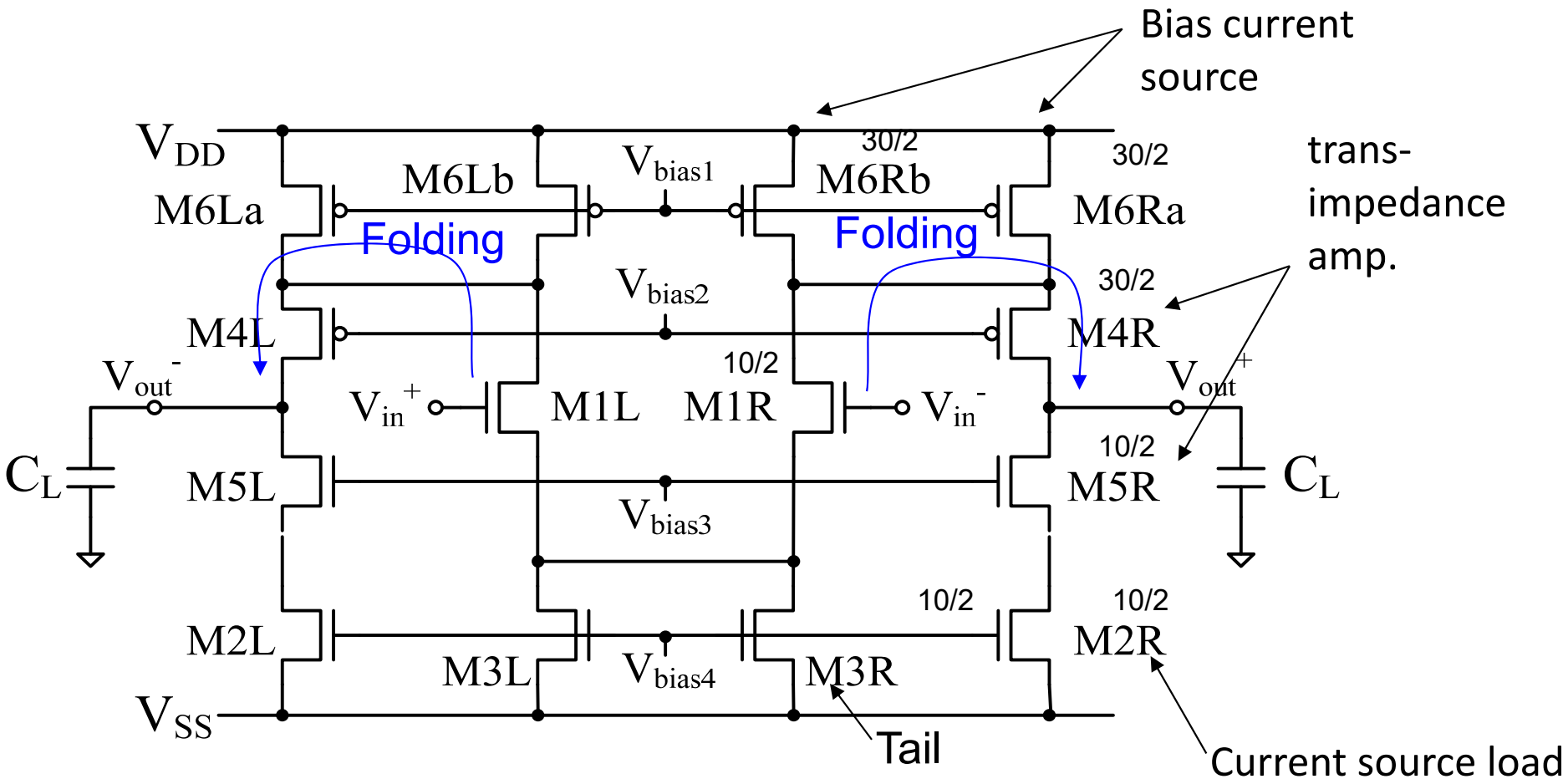


Separate the transconductor and current source load.

Common-mode input range of the folded cascode amplifier

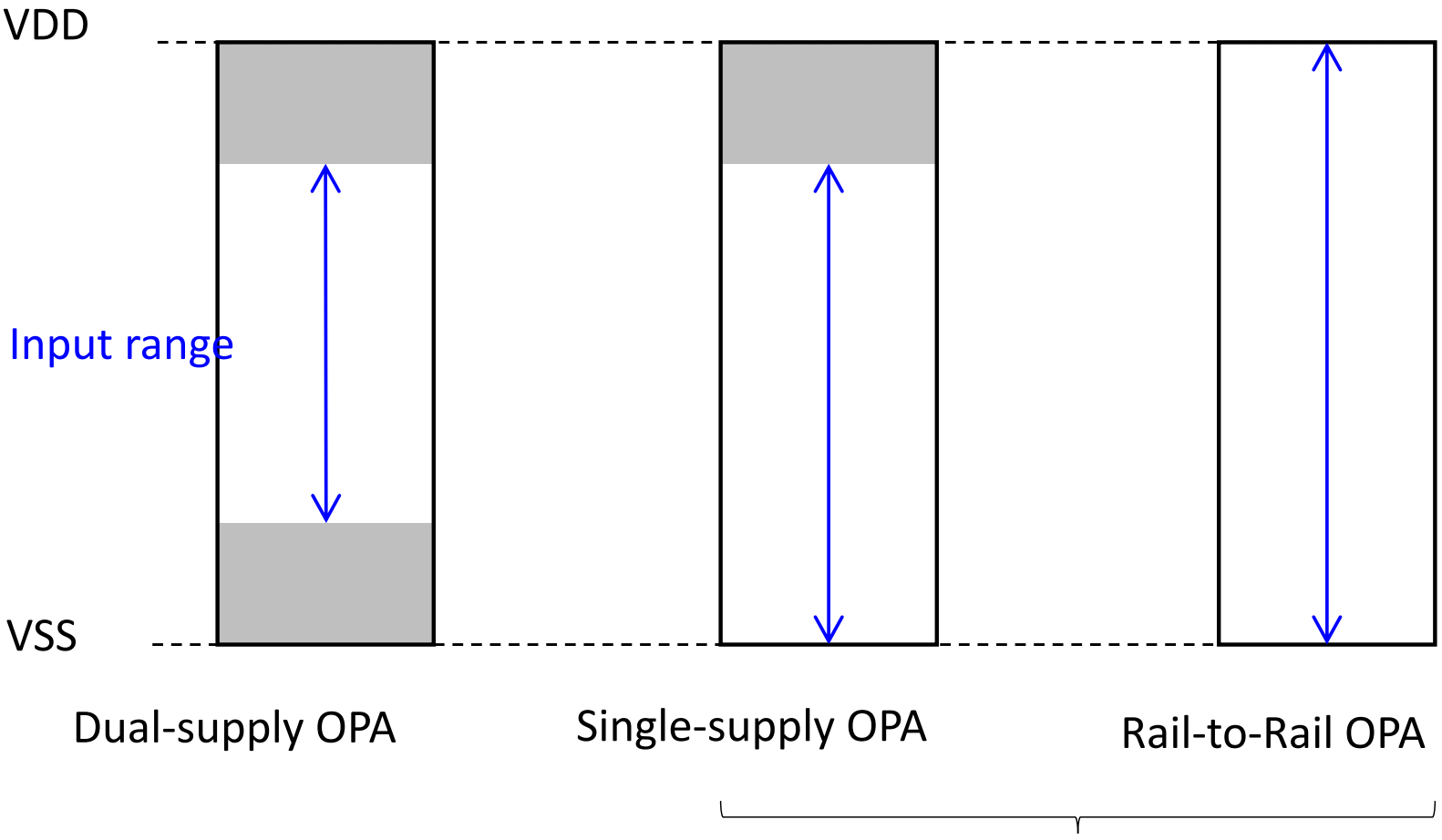


Full-Differential Folded Cascode OPA (or OTA)



(Same as a circuit shown in previous slide)

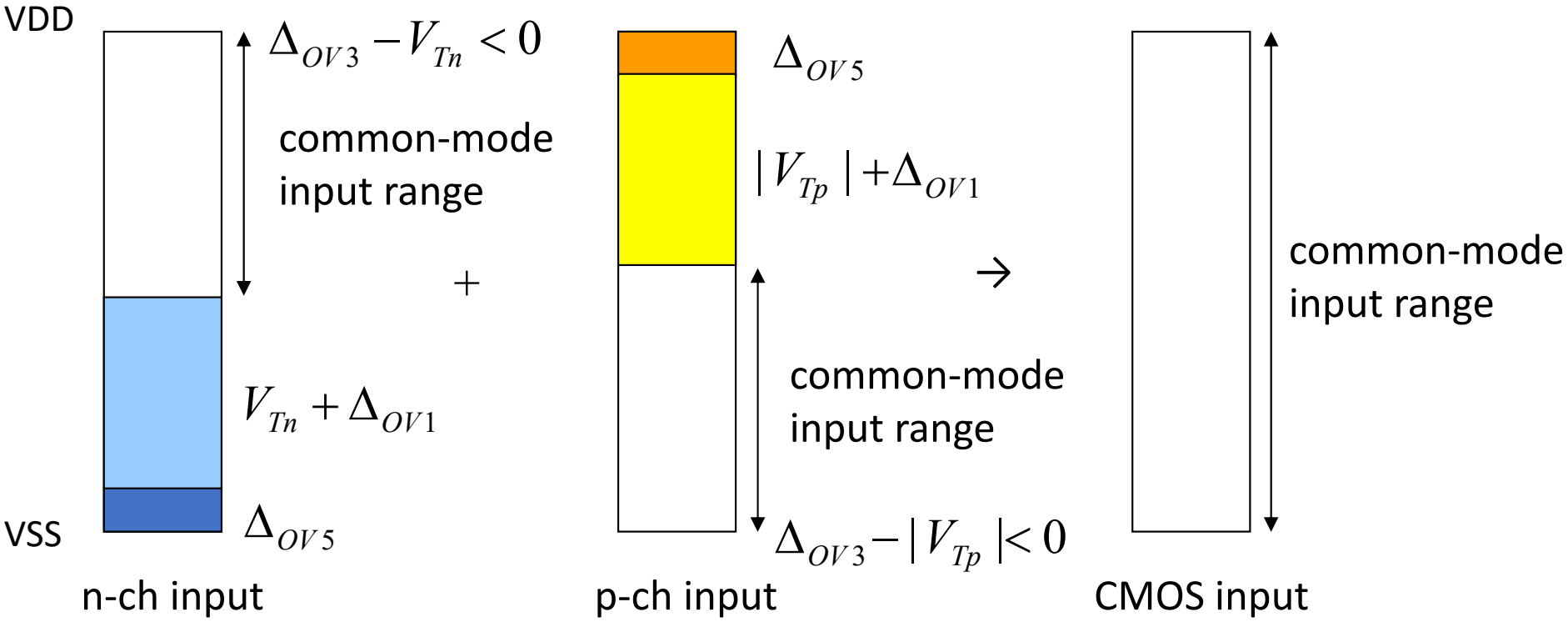
Common mode voltage range of OPA



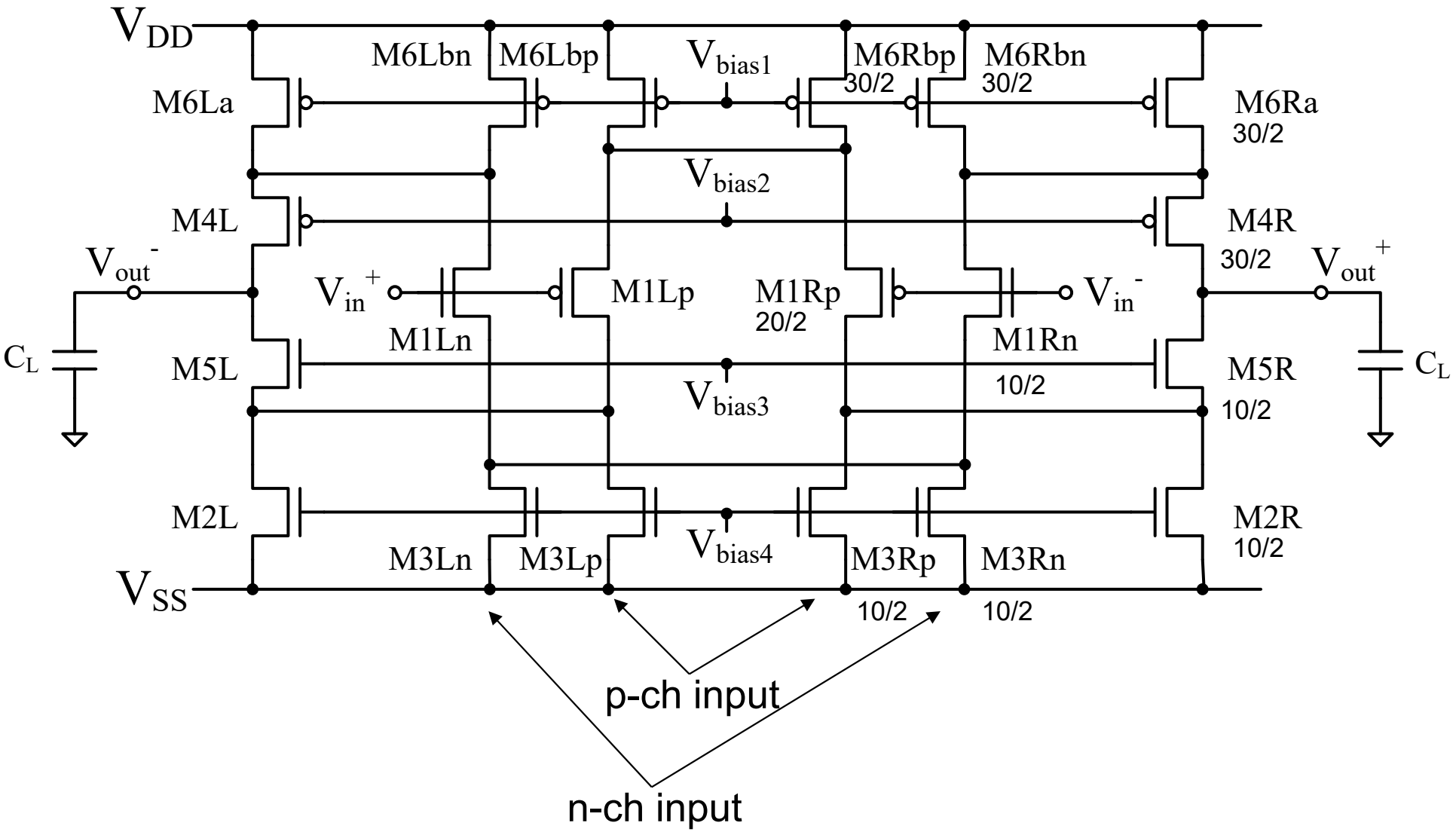
These OPAs operate under the condition that VSS = GND. This feature is useful for many sensor applications.

Rail-to-Rail input stage

Rail-to-Rain input OPA can be composed with p-ch differential pair and n-ch differential pair



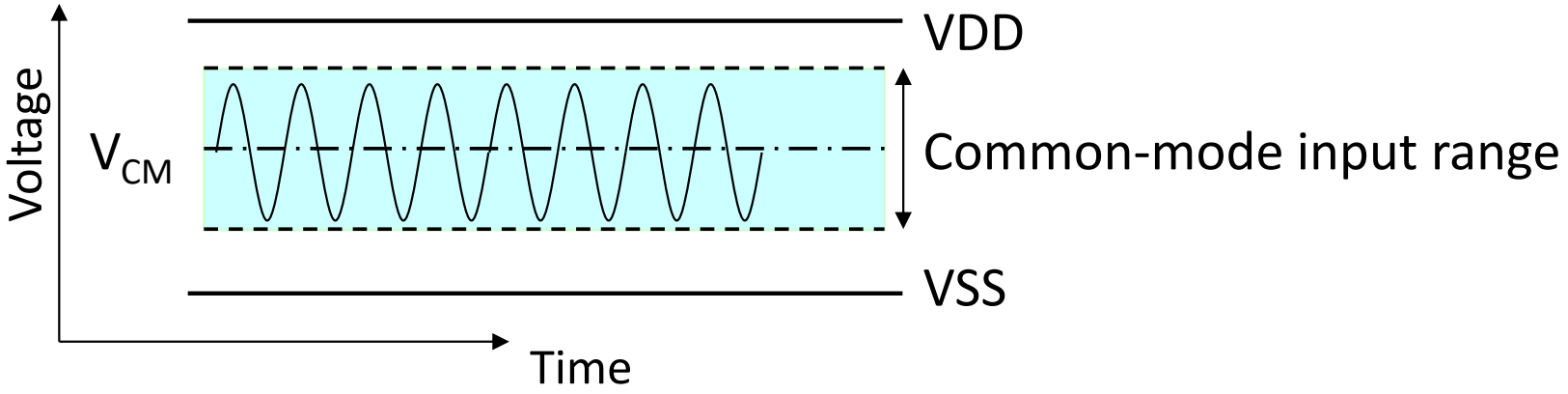
Rail-to-Rail OPA



6. Common mode feedback

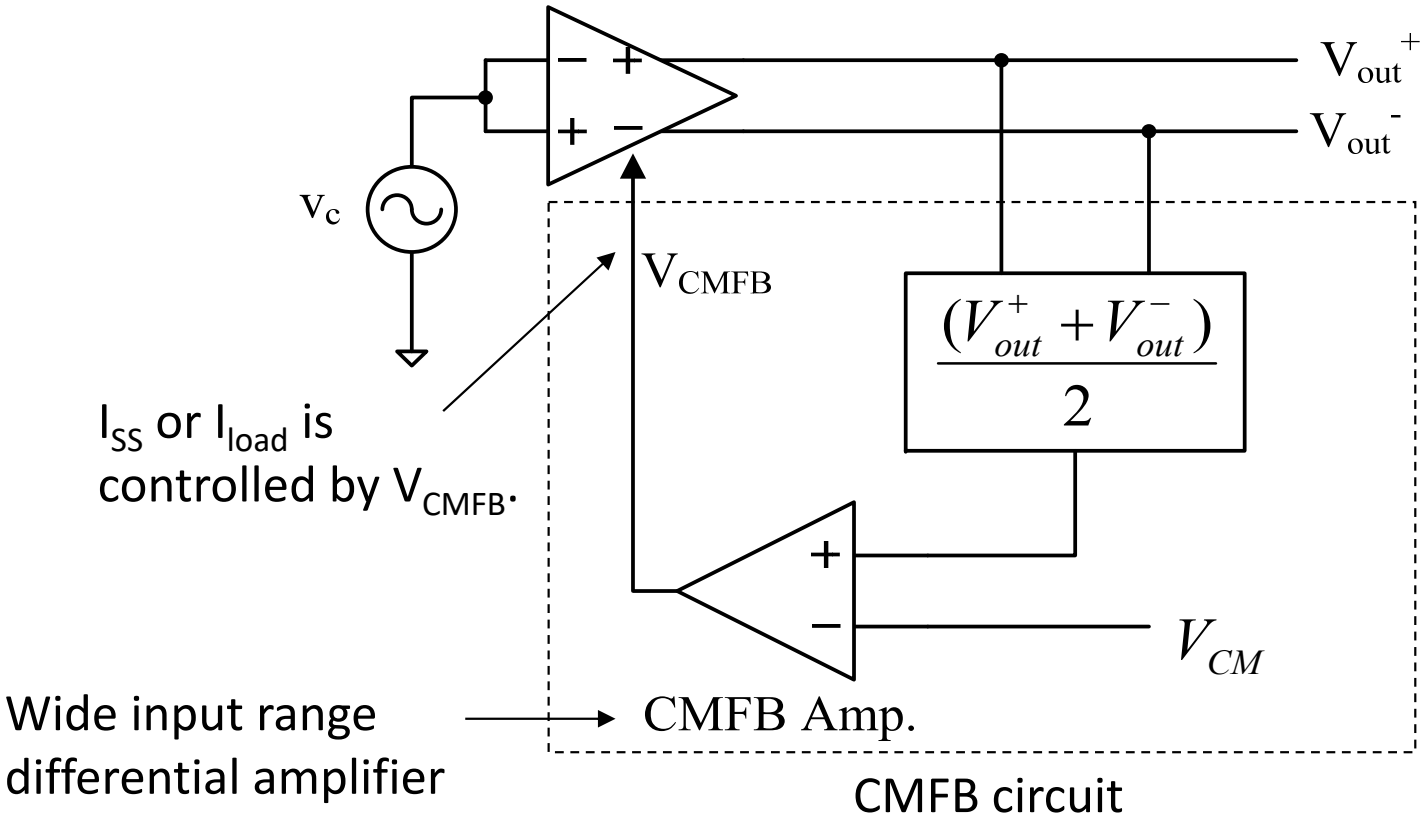
Common Mode Feedback (CMFB)

- Common-mode voltage V_{CM}
  - The common potential of the input and output nodes in the full-differential OPAs cannot be defined in the circuit. Therefore, the full-differential OPAs have to be controlled with the common-mode voltage V_{CM}.
  - The common-mode voltage is applied to the common-mode input.
- I_{SS} or I_{load} should be controlled by the common-mode voltage, because,
  - $I_{load\_L} + I_{load\_R} > I_{SS} \rightarrow \quad V_{out}^{+} = V_{out}^{-} = VDD$
  - $I_{load\_L} + I_{load\_R} < I_{SS} \rightarrow \quad V_{out}^{+} = V_{out}^{-} = VSS$

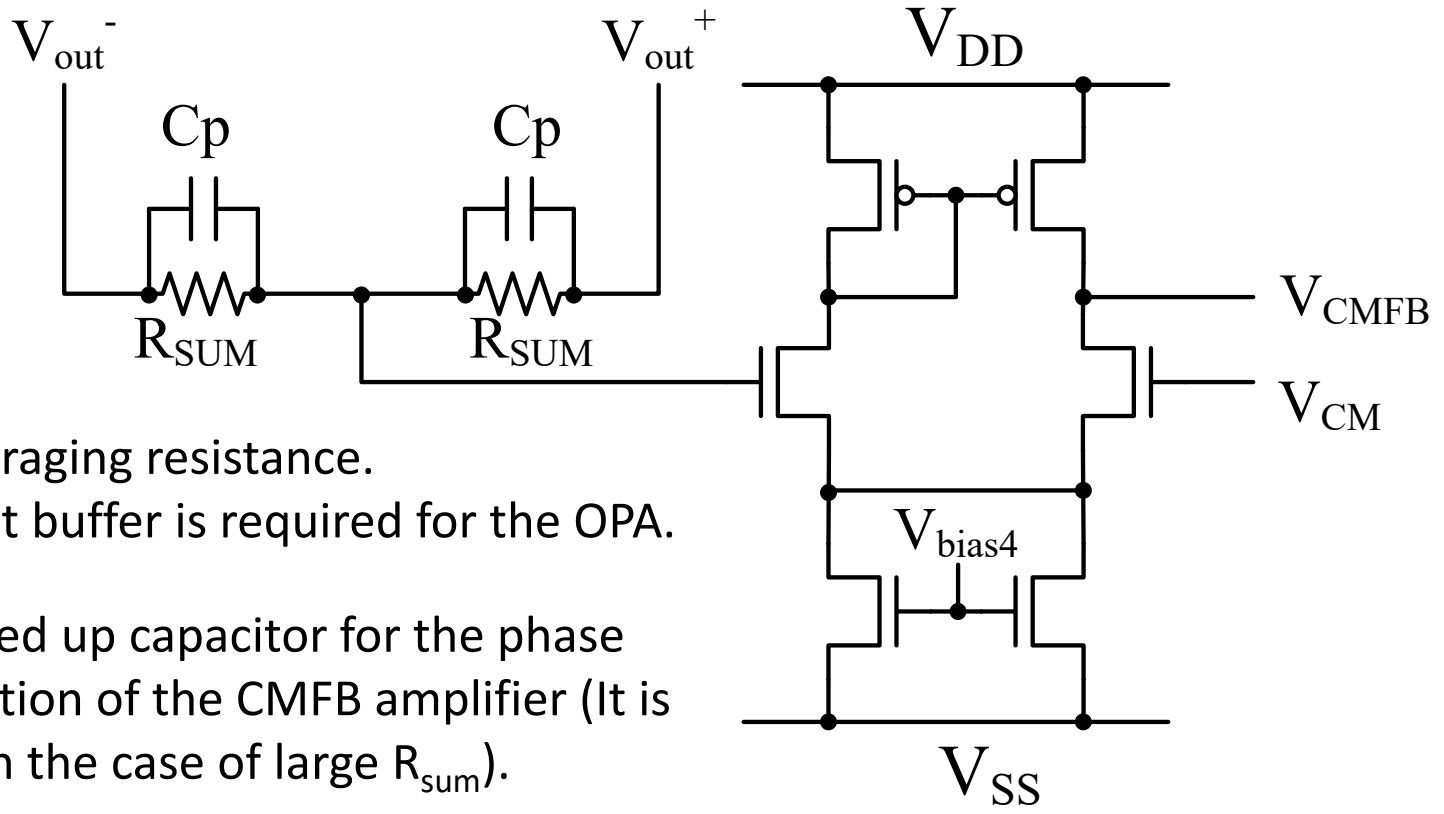


Operation of CMFB

CMFB keeps the bias condition: $I_{D2L} + I_{D2R} = I_{SS}$.



CMFB circuit for continuous-time OPA (1)

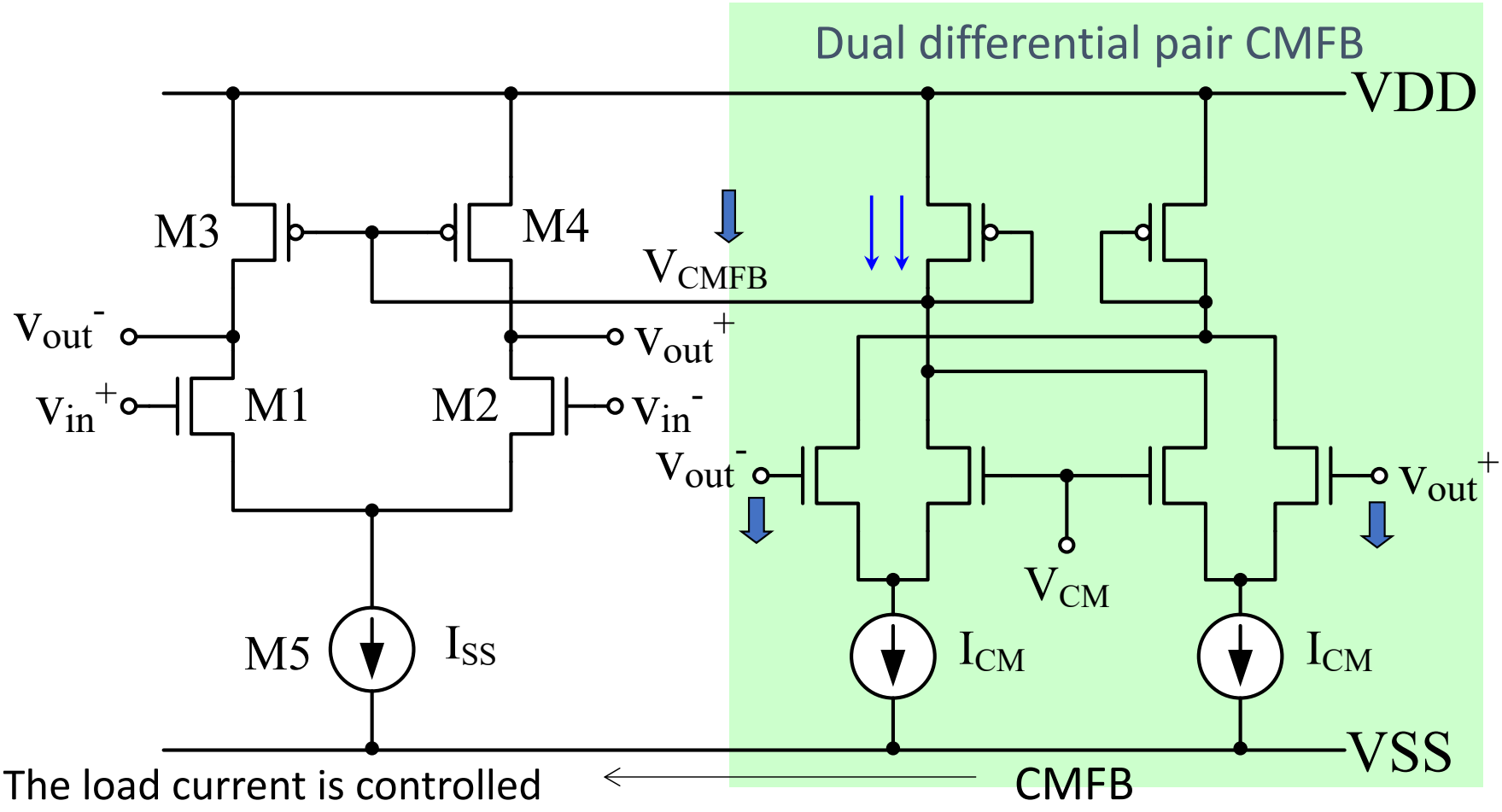


R_{sum} is averaging resistance.
The output buffer is required for the OPA.

C_p is a speed up capacitor for the phase compensation of the CMFB amplifier (It is required in the case of large R_{sum}).

Implementation by the summing amplifier

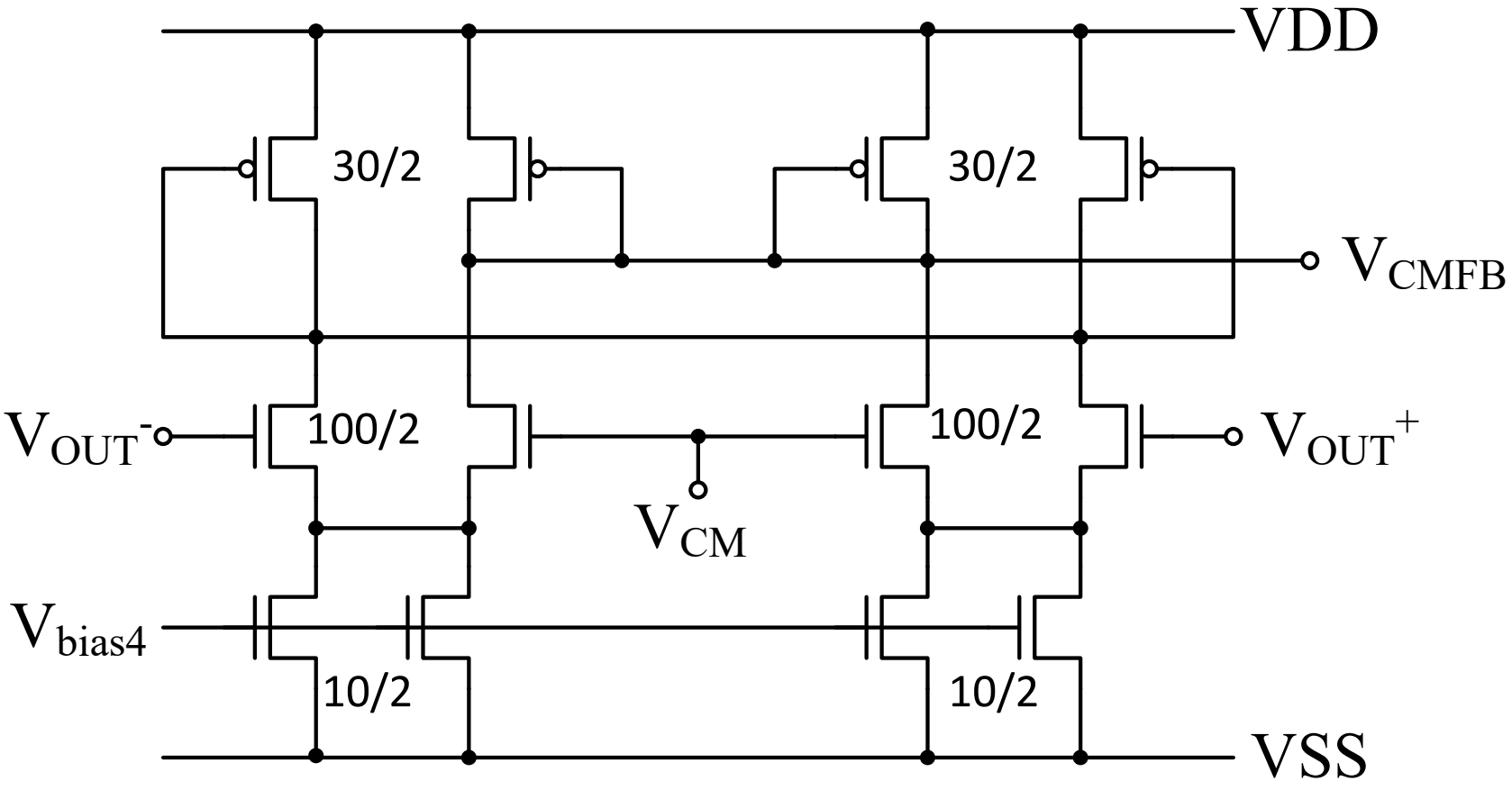
CMFB circuit for continuous-time OPA (2)



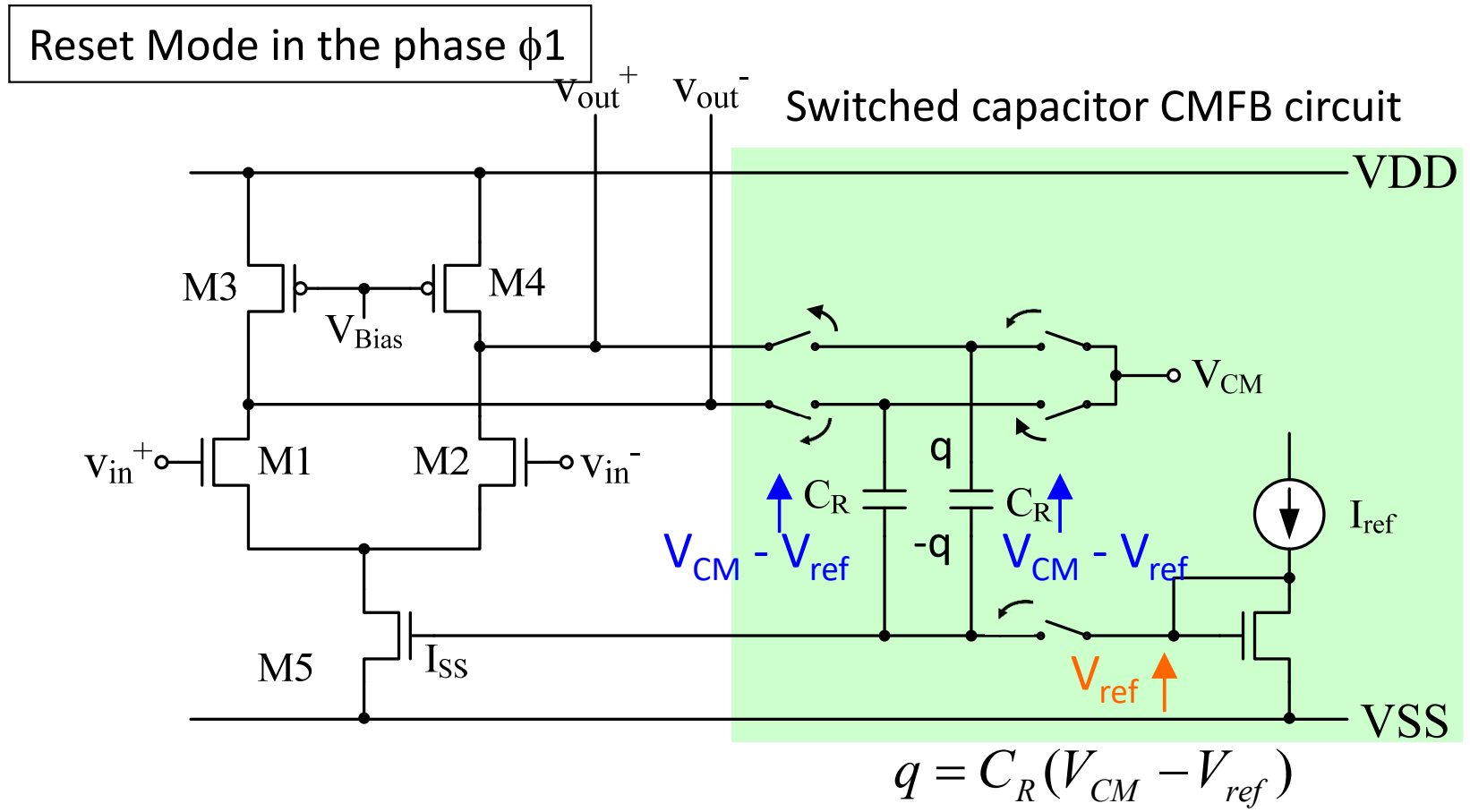
The load current is controlled by the common-mode output referred by V_{CM}.

R.A.Whatley, U.S.Pat. 4, 573, 020, (1986)

Symmetrical implementation of continuous-time CMFB



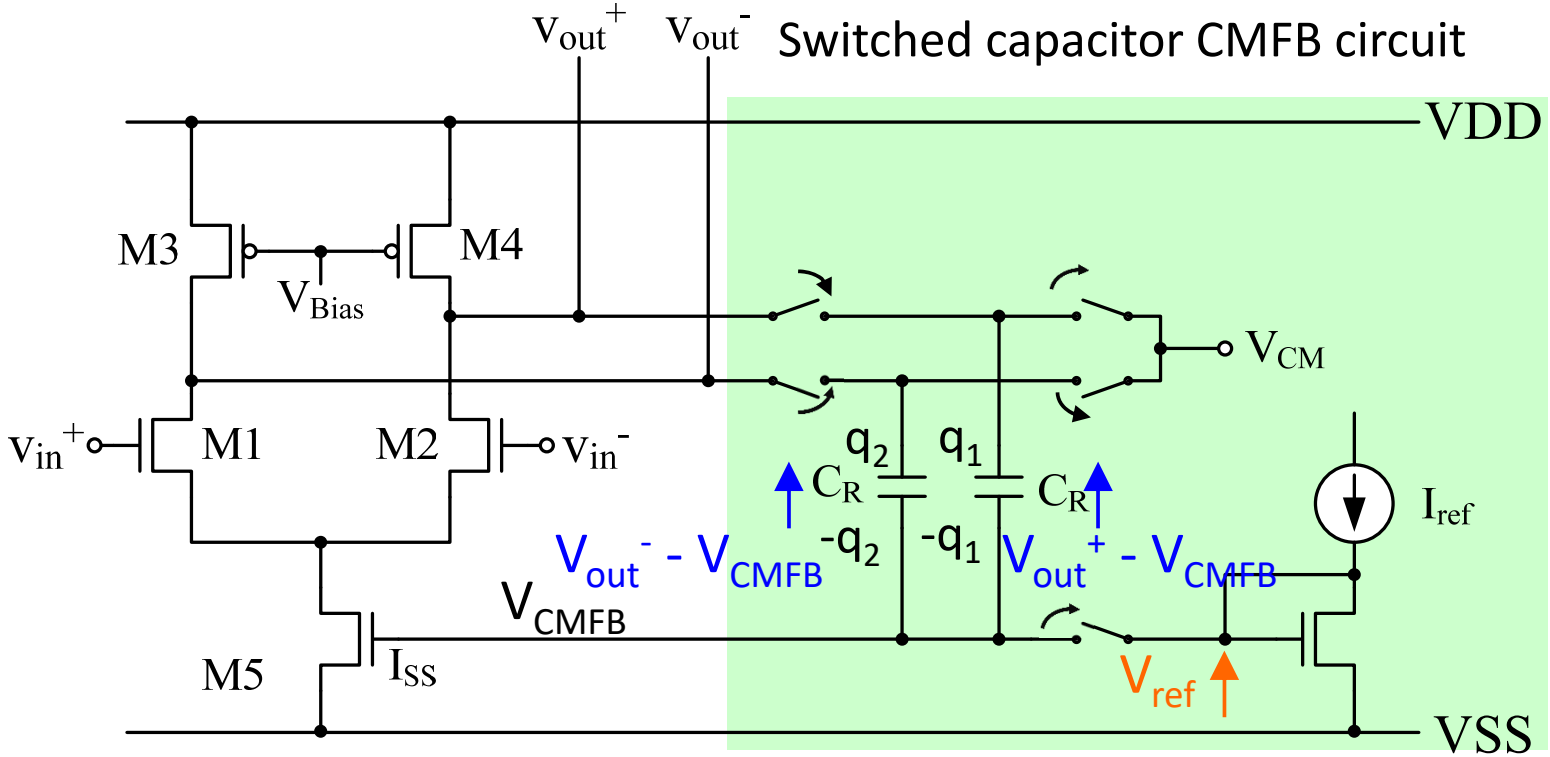
Switched capacitor CMFB for discrete-time OPA (1)



D. Senderowicz et al., IEEE J. Solid-State Circuits, vol.17, p.1014 (1986)

Switched capacitor CMFB for discrete-time OPA (2)

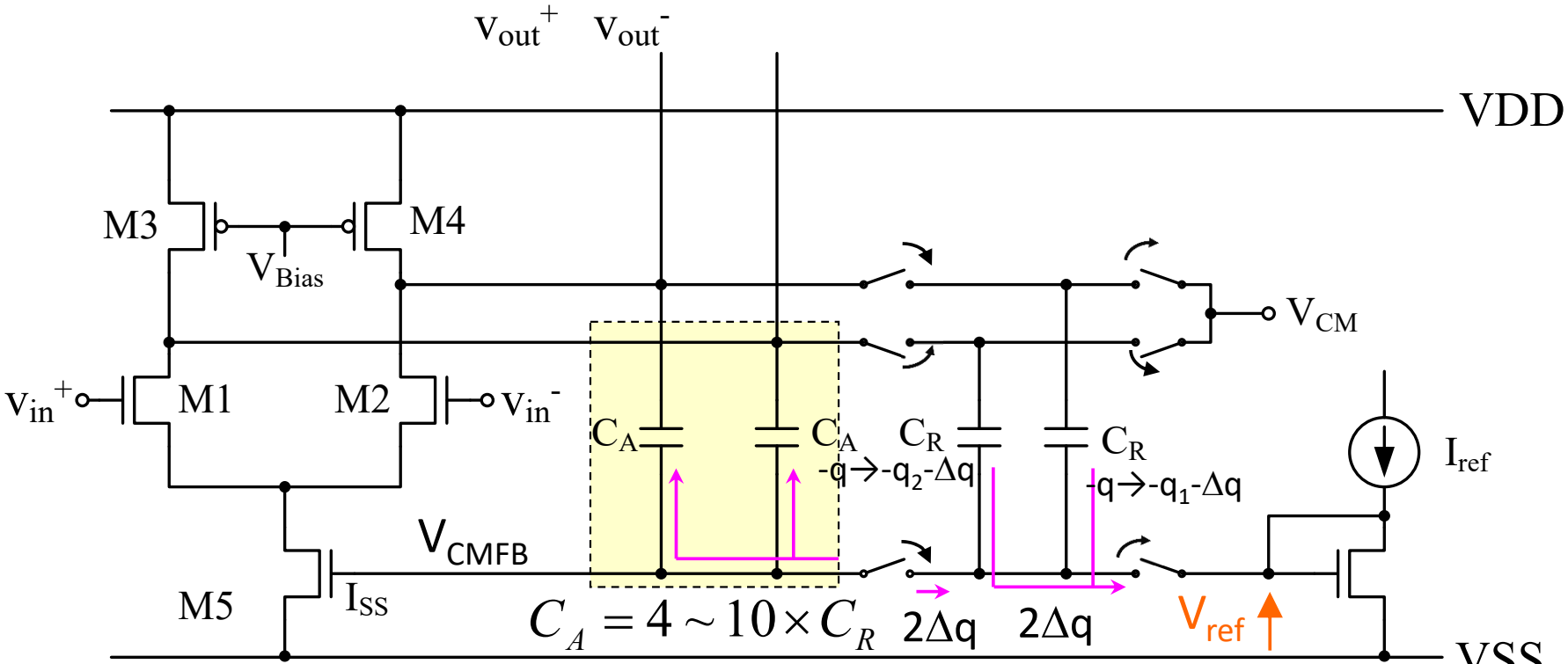
Amplification Mode in the phase $\phi 2$



$$\begin{cases} q_1 + q_2 = 2C_R(V_{CM} - V_{ref}) \\ \quad\quad = C_R(V_{out}^{+} - V_{CMFB}) + C_R(V_{out}^{-} - V_{CMFB}) \end{cases}$$

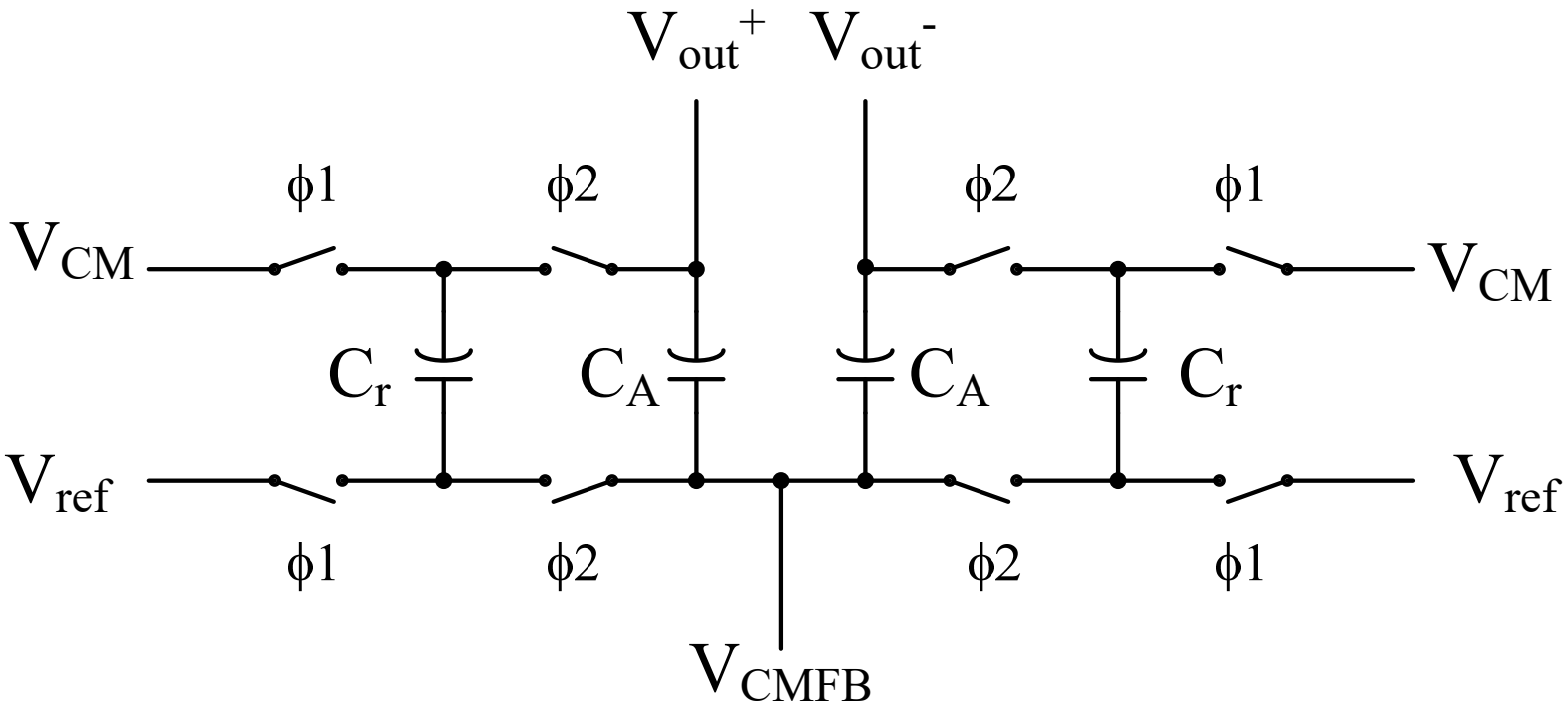
If the common-mode output $=$ V_{CM}, $I_{SS} = I_{ref}$ $\longleftarrow$ $V_{CMFB} = \dfrac{V_{out}^{+} + V_{out}^{-}}{2} - V_{CM} + V_{ref}$

Cancellation of the parasitic capacitances in the CMOS switch



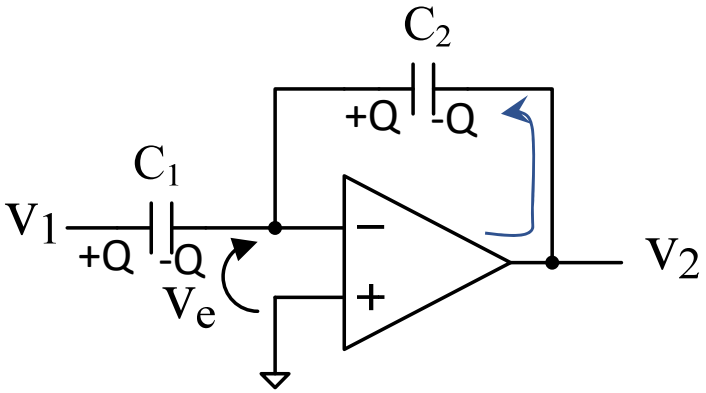
Cancel of the charge injection error of CMOS switch

Symmetrical implementation of discrete-time CMFB

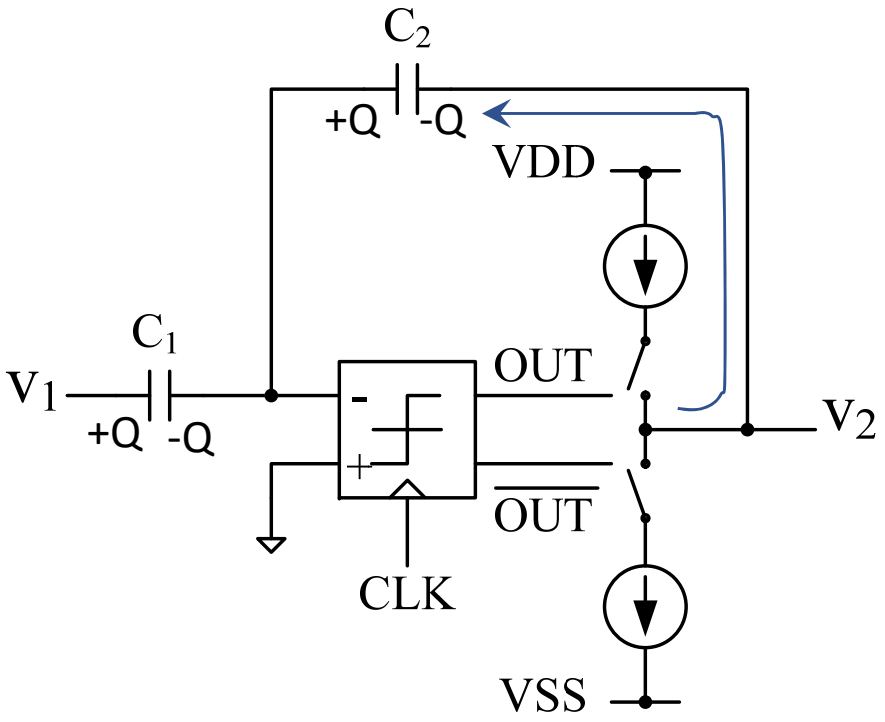


Symmetric schematic (intended for layout design)

(Appendix) Discrete-time operational amplifier with comparator



The output voltage V_2 is regulated to keep the virtual ground, i.e. V_e = 0.



Equivalent circuit with comparator

The discrete time OPA can be replaced with high-precision comparator to implement the differential amplifier, because it is difficult to design the high gain OPA with the fine processes.