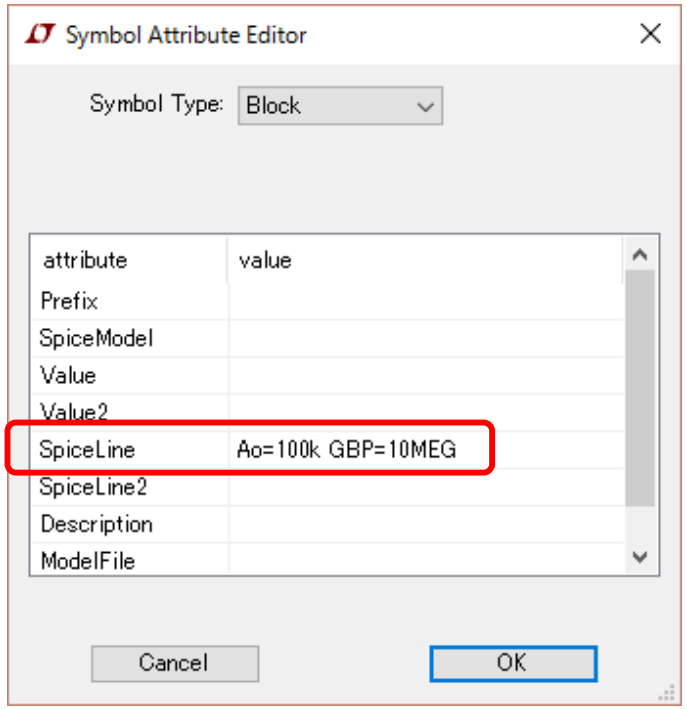
Lab. 03

CHARACTERIZATION OF ANALOG INTEGRATORS

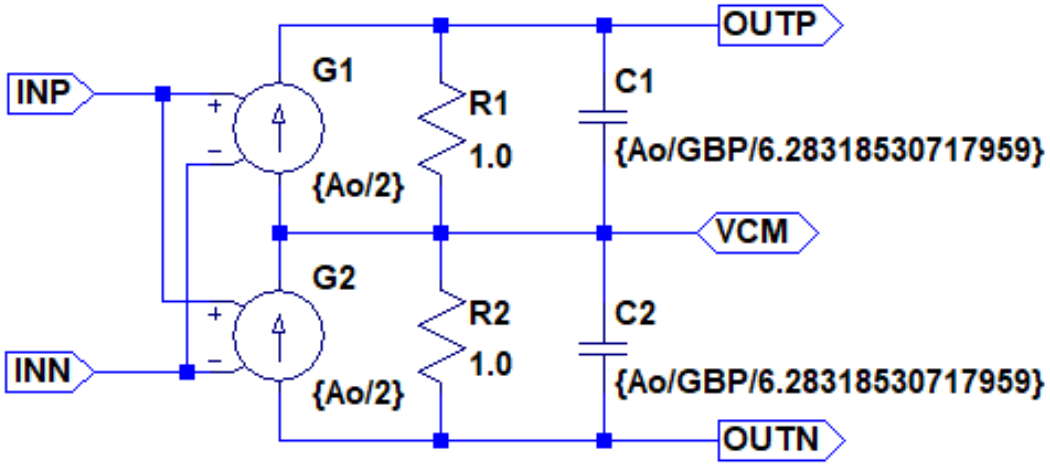
1. Behavioral model of OPA

- Draw up the schematic and symbol of the behaivioral model of the full-differential OPA. (see next slide)
- Set up the attribute of Ao and GBP for the symbol.
  - [Edit] - [Attributes] - [Edit Attributes]
    - This is used for the default value of the parameters.
  - [Edit] - [Attributes] - [Attribute Window]
    - Click "SpiceLine" and Click "OK" button to show the parameters on the schematic automatically.
- Simulate the AC response of the model.
  - Show the simulation results of V(INP)-V(INN), V(OUTP)-V(OUTN).

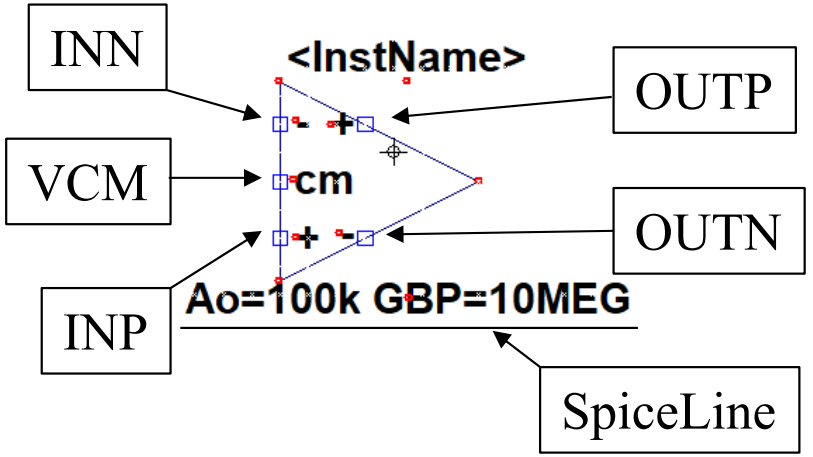


Schematic and symbol

Schematic



Symbol



Ao: Open loop gain

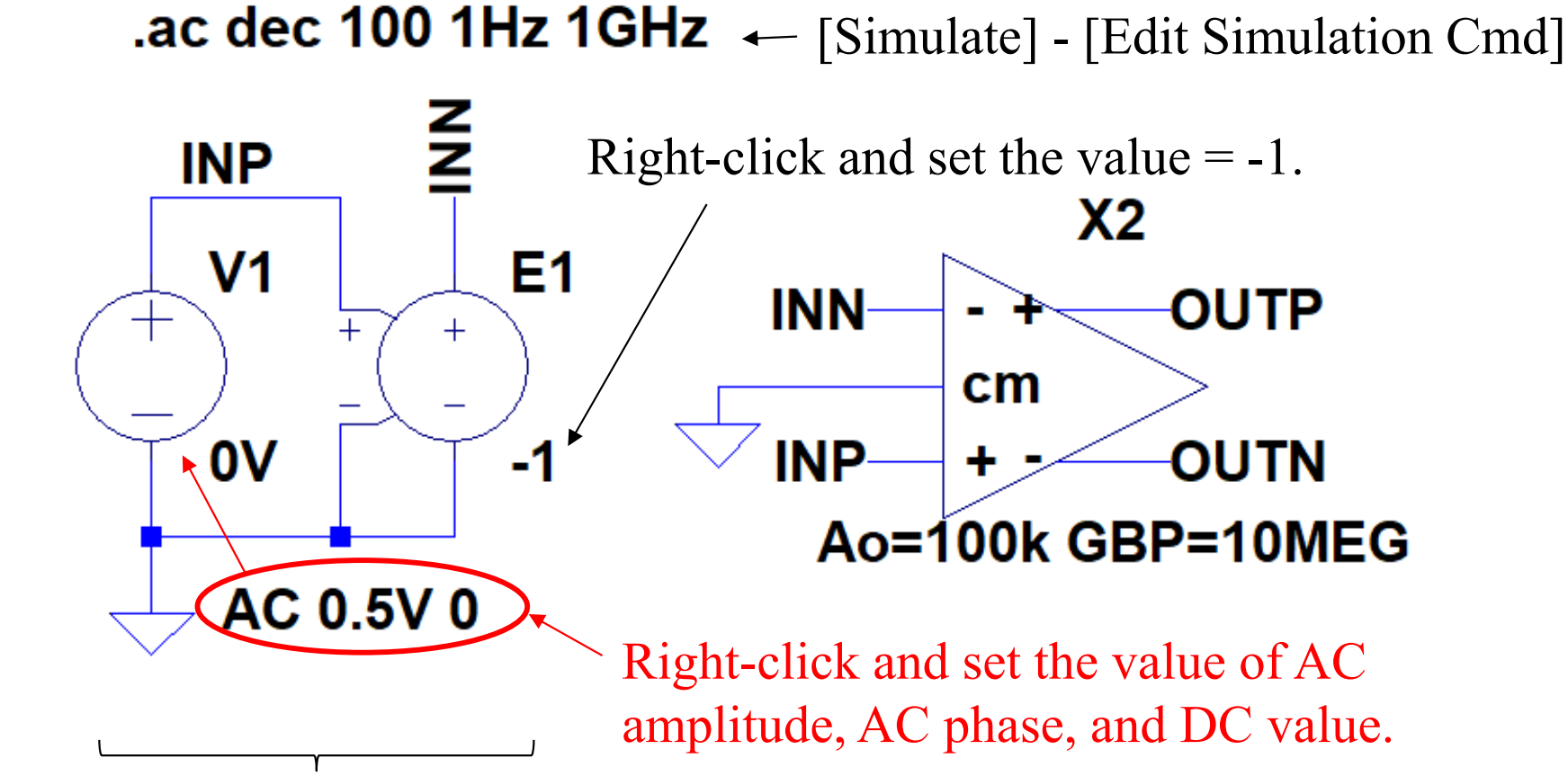
GBP: Gain bandwidth product

1. Draw the outline of the symbol.
2. [Edit] - [Add pin/port]
3. Right-click and set the label of the pin/port properties.
4. [File] - [Save as]

[Note] Files of schematic and symbol

- Use the menu [File] - [Save As] to save the file of the schematic and symbol data for the first time.
  - Do not use [File] - [Save], because the default name is used.
- The same filename have to be used as the schematic and symbol data, except for the extension. (The extension is automatically added.)
  - For example
    - OPA_BH.asc for the schematic data
    - OPA_BH.asy for the symbol data

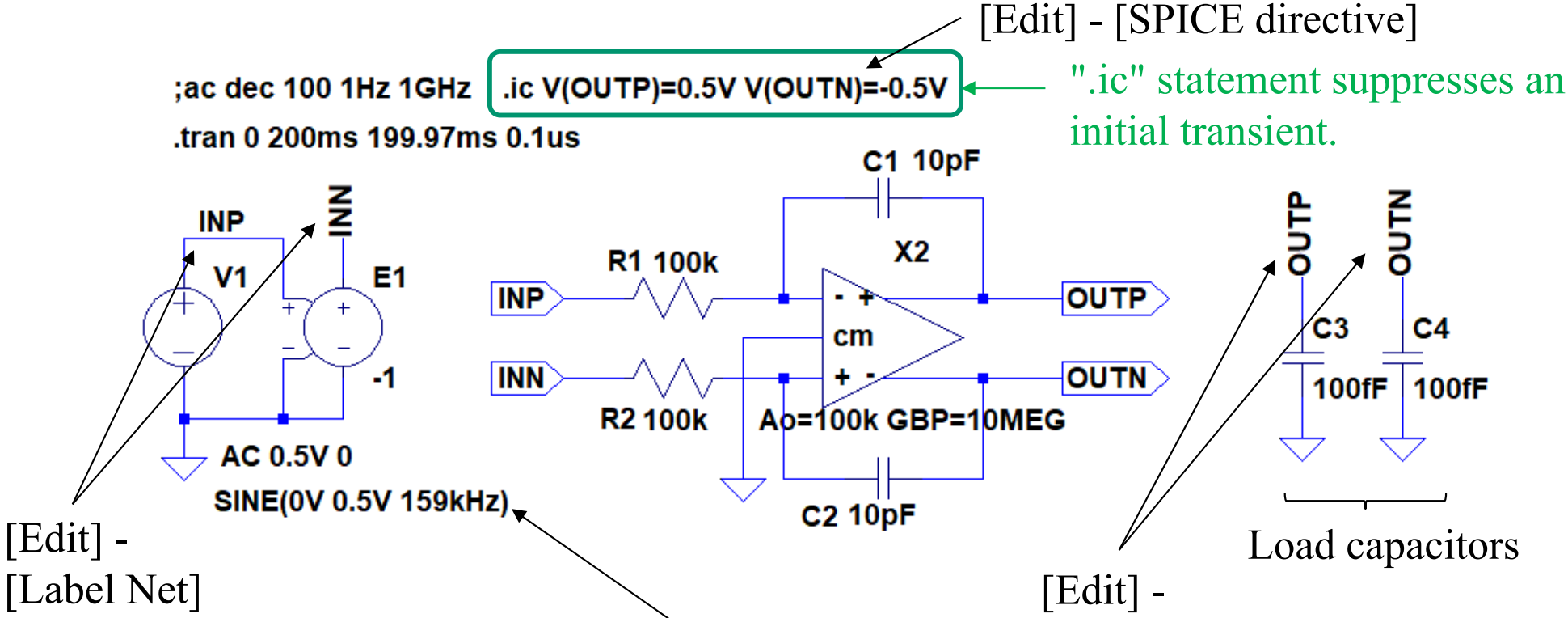
Test bench of behavior model



2. Simulation of CAI and DAI

- Carry out an AC analysis and TRAN analysis of the CAI (Continuous-time analog integrator) and the DAI (Discrete-time analog integrator) with the behavioral OPA model.
- Show the operating frequency range of the CAI in the result of the AC analysis and evaluate the gain errors of CAI and DAI at the unity gain frequency by using the TRAN analyses.

Schematic of CAI



$$H(s) = \frac{-1}{\mathrm{R1C1}}\frac{1}{s}$$

$$f_{unity} = \frac{1}{2\pi \mathrm{R1C1}} = \frac{1}{2\pi \cdot 1us} \cong 159kHz$$

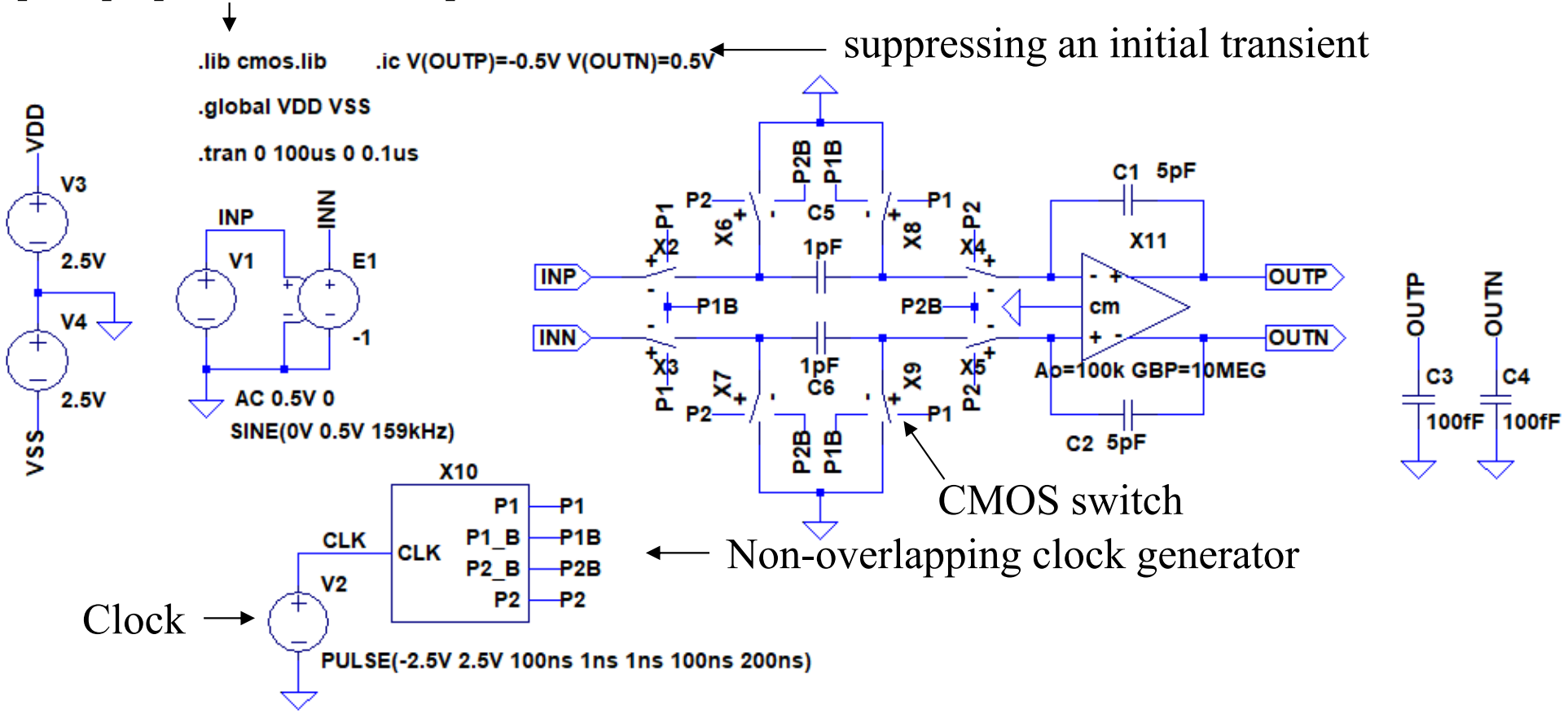
[NOTE] .IC SPICE-directive

You can set the initial condition of the circuit by using .IC directive. The initial voltage or current can be set for each node or each branch.

- Oscillator and multi-stable circuit (Required)
  - An oscillator requires the trigger to start the oscillation.
  - A circuit which has a multiple stable state requires the initial condition to break the initial meta-stable state.
- Circuit having large time constant (Advisable)
  - An appropriate initial condition helps the circuit which includes a large time constant to shift to the steady-state.

Schematic of DAI

[Edit] - [SPICE directive]



$$H(s) = \frac{C5}{C1}\frac{z^{-1}}{1-z^{-1}} \cong \frac{1}{\frac{C1}{C5}T_S s} \qquad f_{unity} = \frac{1}{2\pi\frac{C1}{C5}T_S} = \frac{1}{2\pi \cdot \frac{5pF}{1pF}200ns} \cong 159kHz$$

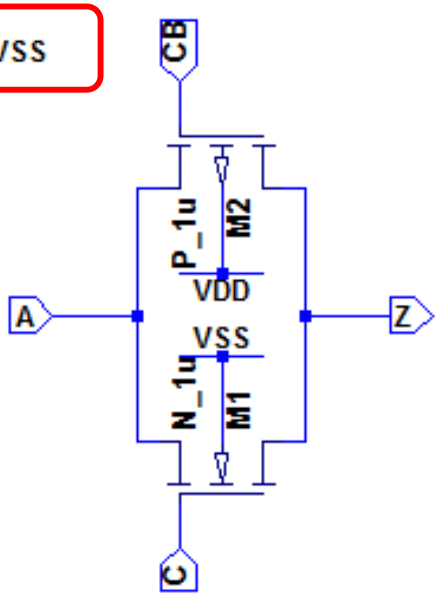
CMOS switch

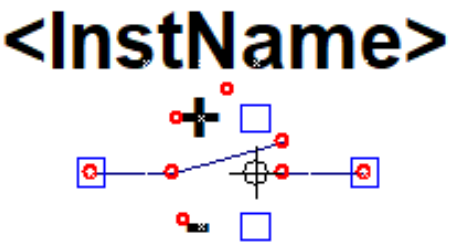
Schematic

Symbol

.global VDD VSS

The ".global" declares the global wire across the hierarchy such as the power lines.

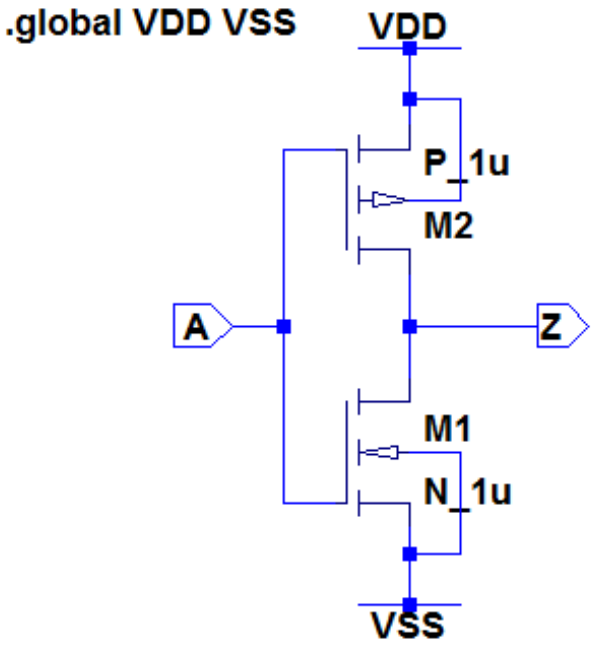




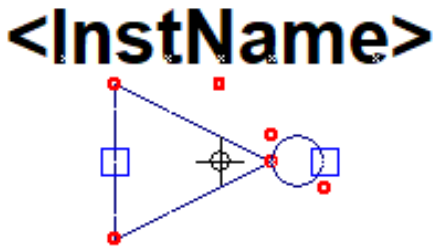
MOSFET	L(m)	W(m)	M	AD, AS(m^2)	PD, PS(m)	W/L
M1	1u	5u	1	15p	11u	5
M2	1u	15u	1	45p	21u	15

Inverter

Schematic



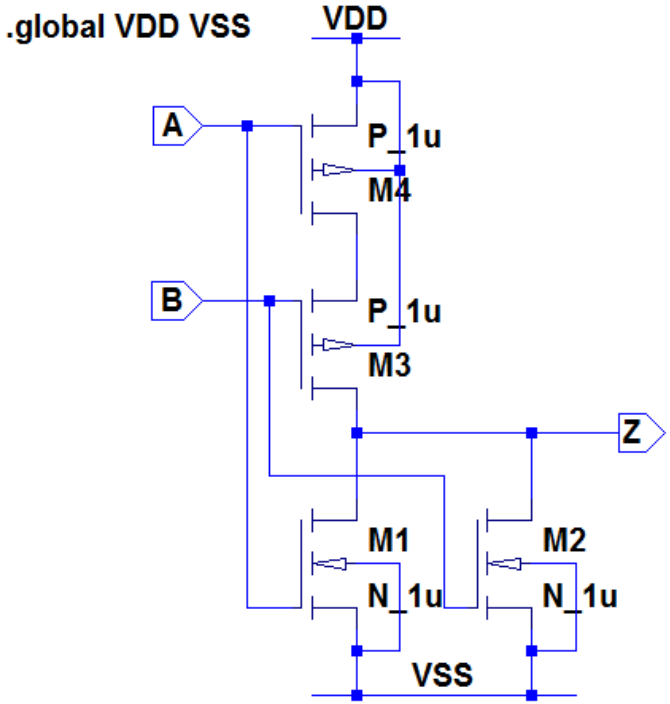
Symbol



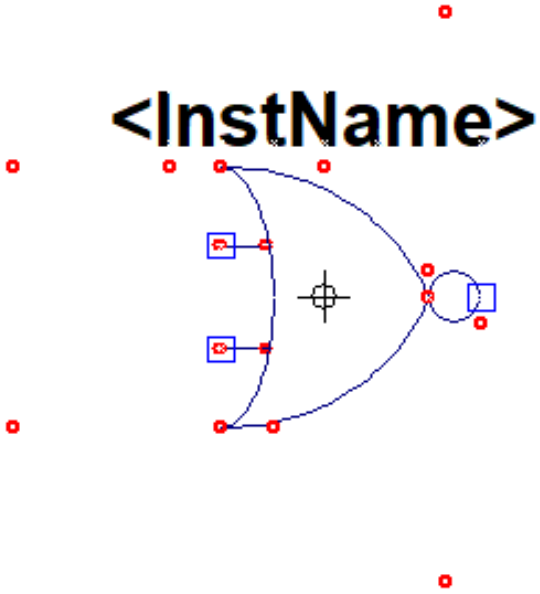
MOSFET	L(m)	W(m)	M	AD, AS(m^2)	PD, PS(m)	W/L
M1	1u	5u	1	15p	11u	5
M2	1u	15u	1	45p	21u	15

NOR

Schematic



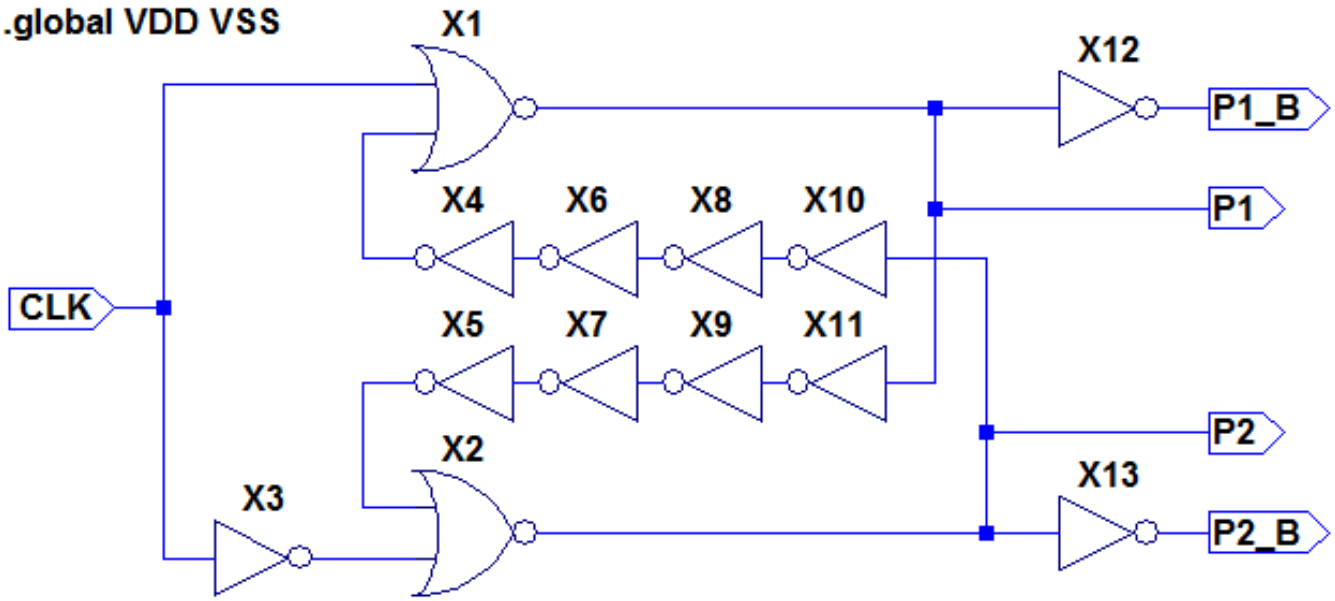
Symbol



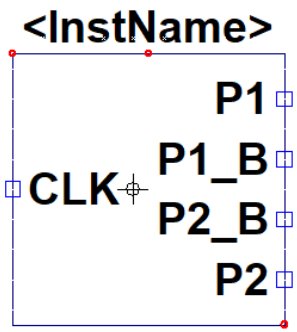
MOSFET	L(m)	W(m)	M	AD, AS(m^2)	PD, PS(m)	W/L
M1, M2	1u	5u	1	15p	11u	5
M3, M4	1u	15u	4	45p	21u	60

Non-overlapping clock generator

Schematic



Symbol



MOSFET	L(m)	W(m)	M	AD, AS(m^2)	PD, PS(m)	W/L
M1	1u	5u	1	15p	11u	5
M2	1u	15u	1	45p	21u	15