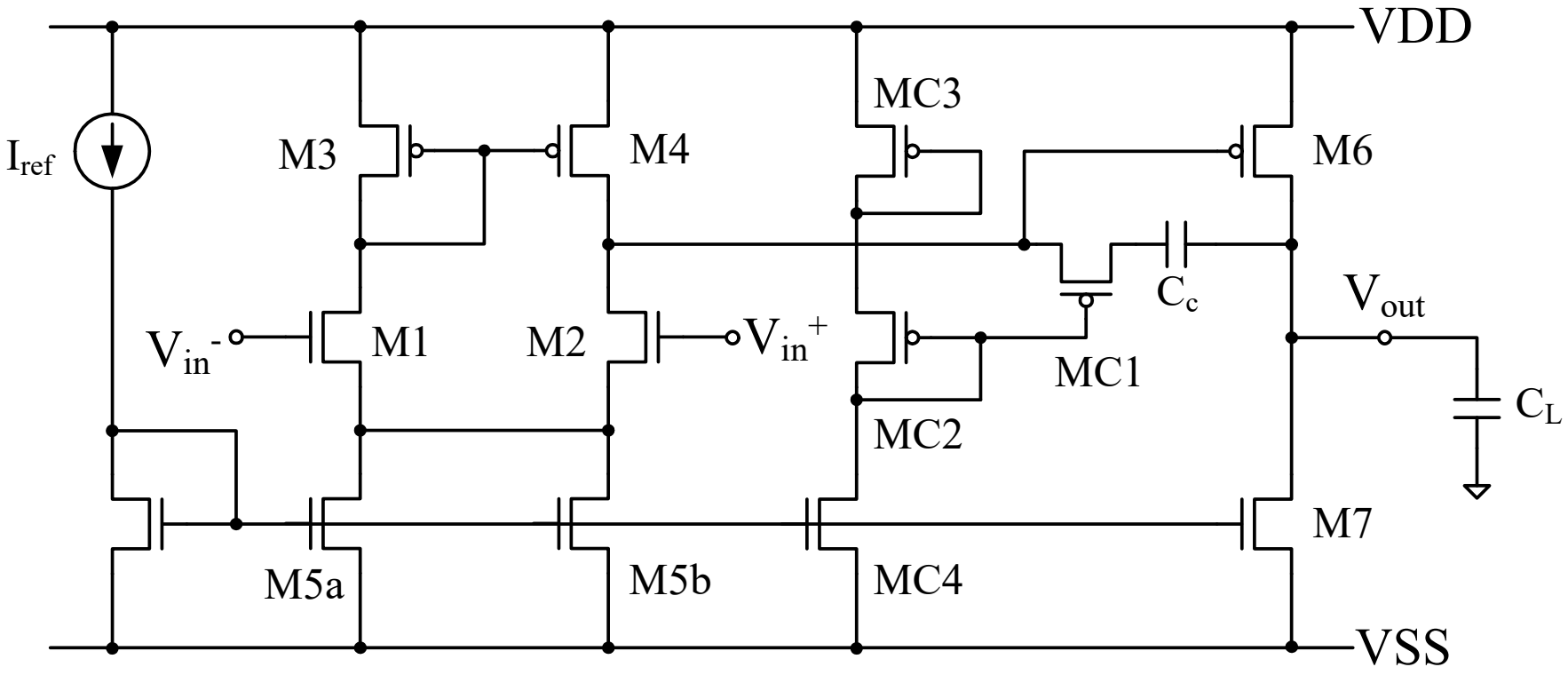
Lab. 12

DESIGN AND CHARACTERIZATION OF SINGLE-END OPA

1. Design of OPA

- Show the design procedure of the 2-stage OPA with the zero-cancellation circuit shown in next slide, with considering the following tips.
  - M6 can be acquitted from the constraint of the phase compensation by using the zero-cancellation circuit. Trim down the size of M6 and I_{DS6}.
  - You can also design more high-gain OPA by tuning the M6 and M7 with the zero-cancellation circuit.

Circuit topology



Spacification sheet for the design

Parameter	Unit	Value	Remarks
GBP	Hz	10M	CL = 1.0pF
A_d	dB	90 (low priority)	@ 100Hz
Phase Margin	degree	60	
A_c	dB	0	@ 100Hz
Slew Rate	V/us	10 (low priority)	CL = 1.0pF
Common-mode input range	V	-1.4 ~ + 2.2	
Bias Current	A	200u	
Reference Current	A	20u	I_{SS} = 40uA

2. Characterization

- Carry out the DC, AC, and TRAN analysis to evaluate your design of the single-end OPA. Fill in the blank in following specification table and attach the simulation results.
  - NOTE: Measure the input-referred offset voltage by the DC characteristic first though, as use it to perform the other analyses.
  - The drain area and perimeter of MOFET are given by W*3u and W+6u, respectively. The source area and perimeter is same as drain.
- Show the result of the noise analysis of V(OUT) and the input-referred noise V(OUT)/gain.
  - Which MOSFET is the dominant noise source? Click the MOSFETs and show the noise power of each MOSFET.

Spacification estimated by the circuit simulation

Evaluation item	Unit	Value	Remarks
GBP	MEGHz		CL = 1.0pF
A_d	dB		@ 10Hz
Phase Margin	degree		
ω_p	Hz		
A_c	dB		@ 1kHz
CMRR	dB		@ 1kHz
Slew Rate	V/us		CL = 1.0pF
Offset voltage	uV		
Quiescent current	A		