Lab. 12 Example solution

DESIGN AND CHARACTERIZATION OF SINGLE-END OPA

1. Design of OPA - the phase compensation

$\omega_{\mathrm{u}} \cong \frac{g_{m1}}{C_C}$ $\omega_{\mathrm{p2}} \cong \frac{g_{m6}}{C_L}$ $\omega_{\mathrm{z}} \cong \infty$ (Zero cancel)

The constraint among g_{m1} and g_{m6} can be eliminated by the zero-nulling circuit. Thus, say $g_{m6} = 2g_{m1}$. In the condition of phase compensation,

$$\omega_{\mathrm{p2}} > 2\omega_{\mathrm{u}}$$

$$\frac{g_{m6}}{C_L} > 2\frac{g_{m1}}{C_C}$$

$$C_C > 2C_L\frac{g_{m1}}{g_{m6}} = C_L = 1.0\mathrm{pF}$$

The larger capacitance value of Cc should be chosen to be on the safe side. For example, $C_C = 4.0\mathrm{pF}$.

2. Design of OPA - GBP

$$\text{GBP} = \omega_u = \frac{g_{m1}}{C_C}$$

$$g_{m1} = C_C \cdot GBP = 4.0\text{pF} \cdot 2\pi \cdot 10\text{MHz} = 251\text{uS}$$

$$g_{m1} = \sqrt{2\beta_1 I_{DS1}} \qquad \beta_1 = \frac{g_{m1}^2}{2I_{DS1}} \qquad I_{DS1} = \frac{I_{SS}}{2} = 20\text{uA}$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}^2}{2\mu_n C_{OX} I_{DS1}} = \frac{(251\text{uS})^2}{2 \cdot 98\text{u A/V}^2 \cdot 20\text{uA}} = 16.07 \approx 16$$

$$= 32\text{u}/2\text{u} = \underbrace{(16\text{u}/2\text{u})}_{\text{W/L}}*\underbrace{2}_{\text{M}}$$

3. Design of OPA - the maximum commom-mode voltage

$$V_{in}^{max} = \text{VDD} - \Delta_{OV3} - |V_{Tp}| + V_{Tn}$$

$$\Delta_{OV3} = \sqrt{\frac{2I_{DS3}}{\beta_3}} = \text{VDD} - |V_{Tp}| + V_{Tn} - V_{in}^{max}$$

$$\beta_3 = \frac{2I_{DS3}}{\left(\text{VDD} - |V_{Tp}| + V_{Tn} - V_{in}^{max}\right)^2}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{2I_{DS3}}{\mu_p C_{OX}} \frac{1}{\left(\text{VDD} - |V_{Tp}| + V_{Tn} - V_{in}^{max}\right)^2}$$

$$= \frac{2 \cdot 20\text{uA}}{33\text{uA/V}^2} \frac{1}{(2.5\text{V} - 0.86\text{V} + 0.78\text{V} - 2.2\text{V})^2} = 25.04 \approx 25 = 50\text{u}/2\text{u} = (10\text{u}/2\text{u})*5$$

4. Design of OPA - the minimum commom-mode voltage

$$\Delta_{OV1}= \sqrt{\frac{2I_{DS1}}{\beta_1}} = \sqrt{\frac{2 \cdot 20\text{uA}}{98\text{u A/V}^2\,16}} = 0.160\text{V}$$

$$V_{in}^{min} = \text{VSS} + V_{Tn} + \Delta_{OV1} + \Delta_{OV5}$$

$$\Delta_{OV5}= \sqrt{\frac{2I_{DS5}}{\beta_5}} = V_{in}^{min} - \Delta_{OV1} - V_{Tn} - VSS$$

$$\beta_5 = \frac{2I_{DS5}}{\left(V_{in}^{min} - \Delta_{OV1} - V_{Tn} - VSS\right)^2}$$

$$\left(\frac{W}{L}\right)_{5a} = \left(\frac{W}{L}\right)_{5b} = \frac{1}{2}\left(\frac{W}{L}\right)_5 = \frac{2I_{DS5}}{\mu_n C_{OX}} \frac{1}{\left(V_{in}^{min} - \Delta_{OV1} - V_{Tn} - VSS\right)^2}$$

$$= \frac{2 \cdot 20\text{uA}}{98\text{uA/V}^2} \frac{1}{(-1.4 - 0.160 - 0.78 + 2.5)^2} = 15.94 \approx 16 \;\; = 32\text{u}/2\text{u} = (16\text{u}/2\text{u})*2$$

5. Design of OPA - the systematic offset

From the assumption on the phase compensation,

$$g_{m6} = 2g_{m1} = 2 \cdot 251\text{uS} = 502\text{uS}$$

$$\Delta_{OV4} = \sqrt{\frac{2I_{DS4}}{\beta_4}} = \sqrt{\frac{2 \cdot 20\text{uA}}{33\text{u A/V}^2\, 25}} = 0.220\text{V}$$

$$V_{GS4} = V_{GS6} \rightarrow \frac{I_{DS6}}{I_{DS4}} = \frac{\beta_6}{\beta_4} \qquad g_{m6} = \sqrt{2\beta_6 I_{DS6}} = \sqrt{2\beta_6 \frac{\beta_6}{\beta_4} I_{DS4}} = \beta_6 \Delta_{OV4}$$

$$\beta_6 = \frac{g_{m6}}{\Delta_{OV4}}$$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{\mu_p C_{OX}} \frac{1}{\Delta_{OV4}} = \frac{502\text{uS}}{33\text{u A/V}^2} \frac{1}{0.220\text{V}} = 69.14 \approx 70 = 140/2 = (10/2)*14$$

$$\left(\frac{W}{L}\right)_7 = \frac{1}{2}\left(\frac{W}{L}\right)_5 \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{1}{2} 32 \frac{70}{25} = 44.8 \approx 45 = 90\text{u}/2\text{u} = (10\text{u}/2\text{u})*9$$

6. Design of OPA - zero cancelling

$$\left(\frac{W}{L}\right)_{MC1} = \left(\frac{W}{L}\right)_{MC2} = \left(\frac{W}{L}\right)_{MC3} = \left(\frac{W}{L}\right)_{6} = 70 = 140u/2u = (10u/2u)*14$$

$$\left(\frac{W}{L}\right)_{MC4} = \left(\frac{W}{L}\right)_{7} = 45 = 90u/2u = (10u/2u)*9$$

The bias current and quiescent power consumption

$$I_{DS6} = \frac{\beta_6}{\beta_4} I_{DS4} = \frac{70}{25} 20\text{uA} = 56\text{uA}$$

$$I_{bias} = I_{ref} + I_{DS5a} + I_{DS5a} + I_{DS\_MC4} + I_{DS7} = 3 * 20\text{uA} + 2 * 56\text{uA} = 172\text{uA}$$

$$P_{bias} = I_{bias} \cdot (VDD - VSS) = 172\text{uA} \cdot 5.0\text{V} = 860\text{uW}$$

7. Design of OPA – other properties

The differential gain

$$A_d = \frac{2\sqrt{\beta_1\beta_6}}{(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)}\frac{1}{\sqrt{I_{DS1}I_{DS6}}} = \frac{2\sqrt{\mu_n C_{OX}\left(\frac{W}{L}\right)_1 \mu_p C_{OX}\left(\frac{W}{L}\right)_6}}{(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)}\frac{1}{\sqrt{I_{DS1}I_{DS6}}}$$

$$= \frac{2\sqrt{98\mathrm{uA/V}^2\cdot 16\cdot 33\mathrm{uA/V}^2\cdot 70}}{(0.0186+0.0114)^2}\frac{1}{\sqrt{20\mathrm{uA}\cdot 56\mathrm{uA}}} = 126374 = 102\mathrm{dB}$$

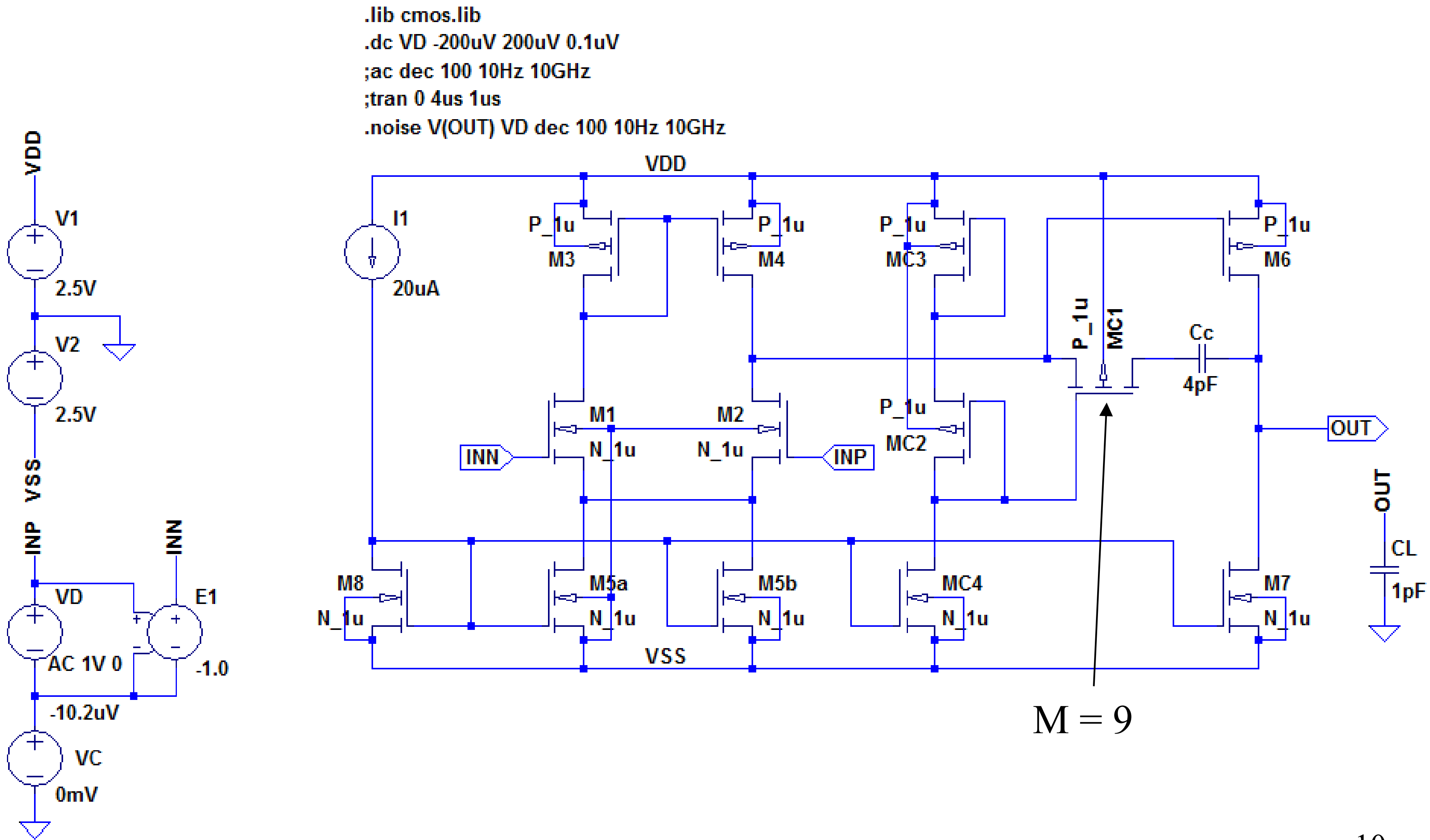
The slew rate

$$SR = \frac{I_{DS5a}+I_{DS5b}}{C_c} = \frac{40\mathrm{uA}}{4.0\mathrm{pF}} = 10\mathrm{V/us}$$

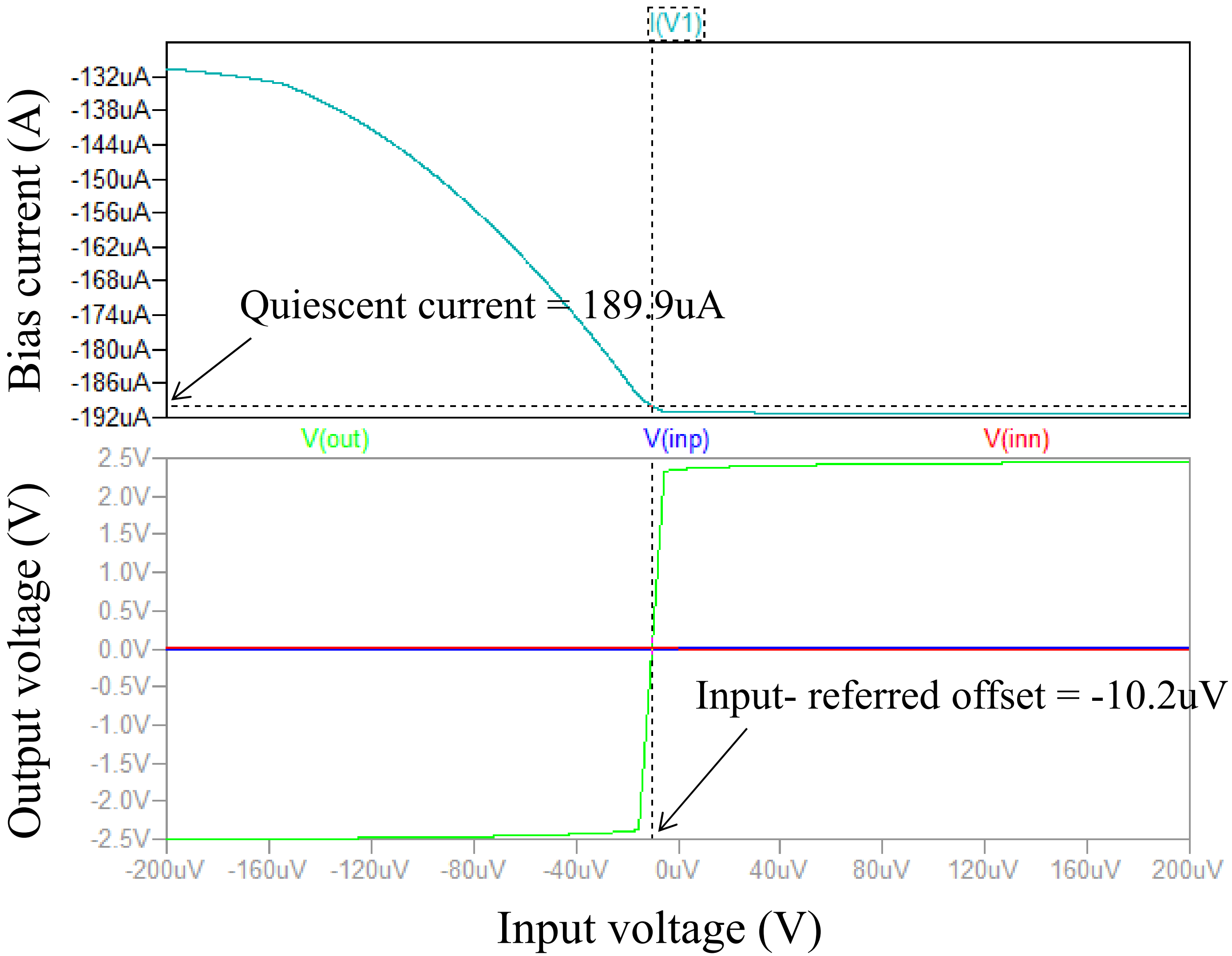
Schematic

- Draw the schematic of the single-end OPA.
  - or paste the captured schematic with the schematic editor.
- Insert the size (L, W, M) of MOSFET and capacitance value in the schematic.
  - NOTE: The size of MC1 need to be fine-tuned. You have obtained the result L = 2u, W = 10u, M = 14, but use L = 2u, W = 10u, M = 9.

Characterization of OPA

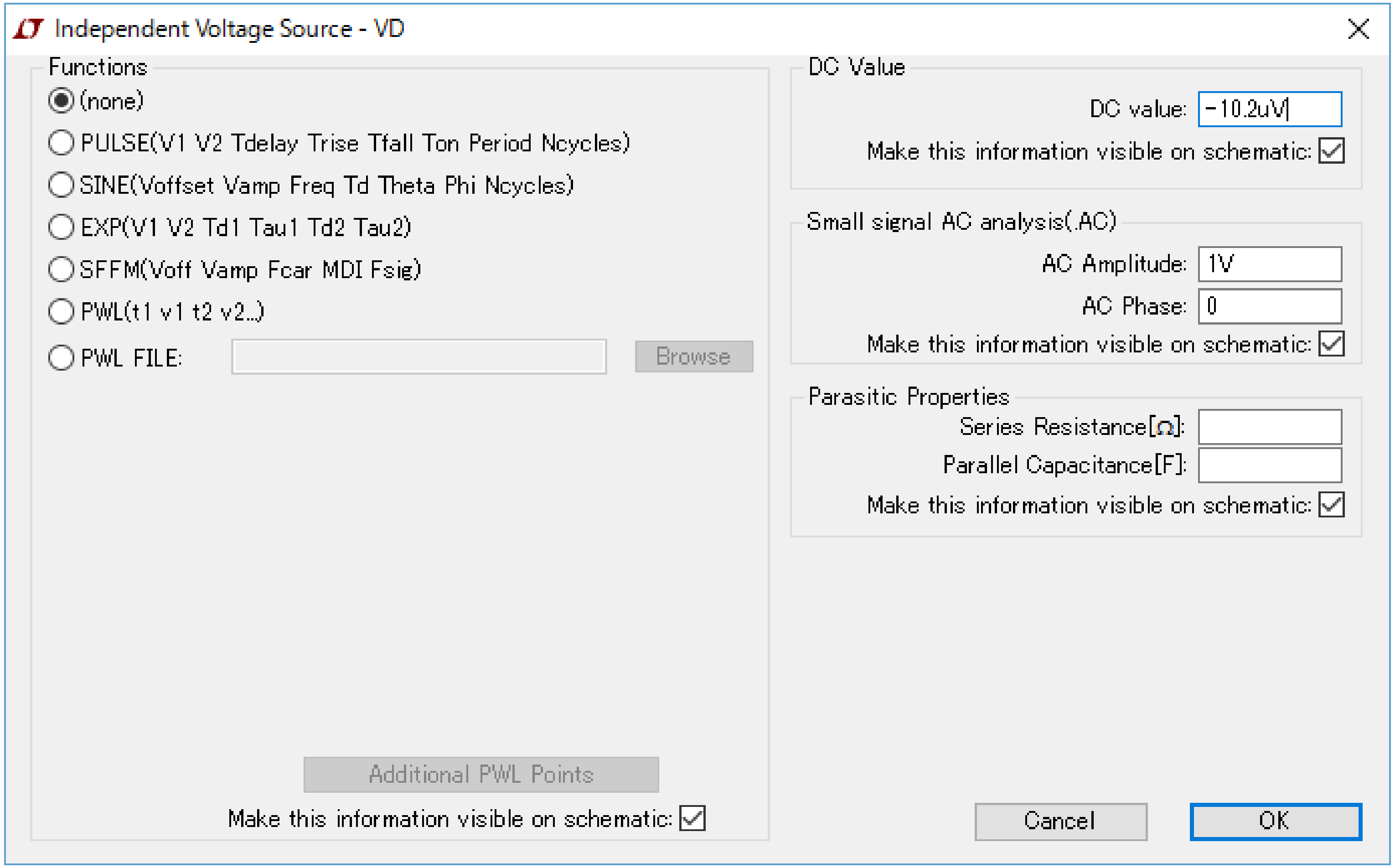


DC analysis

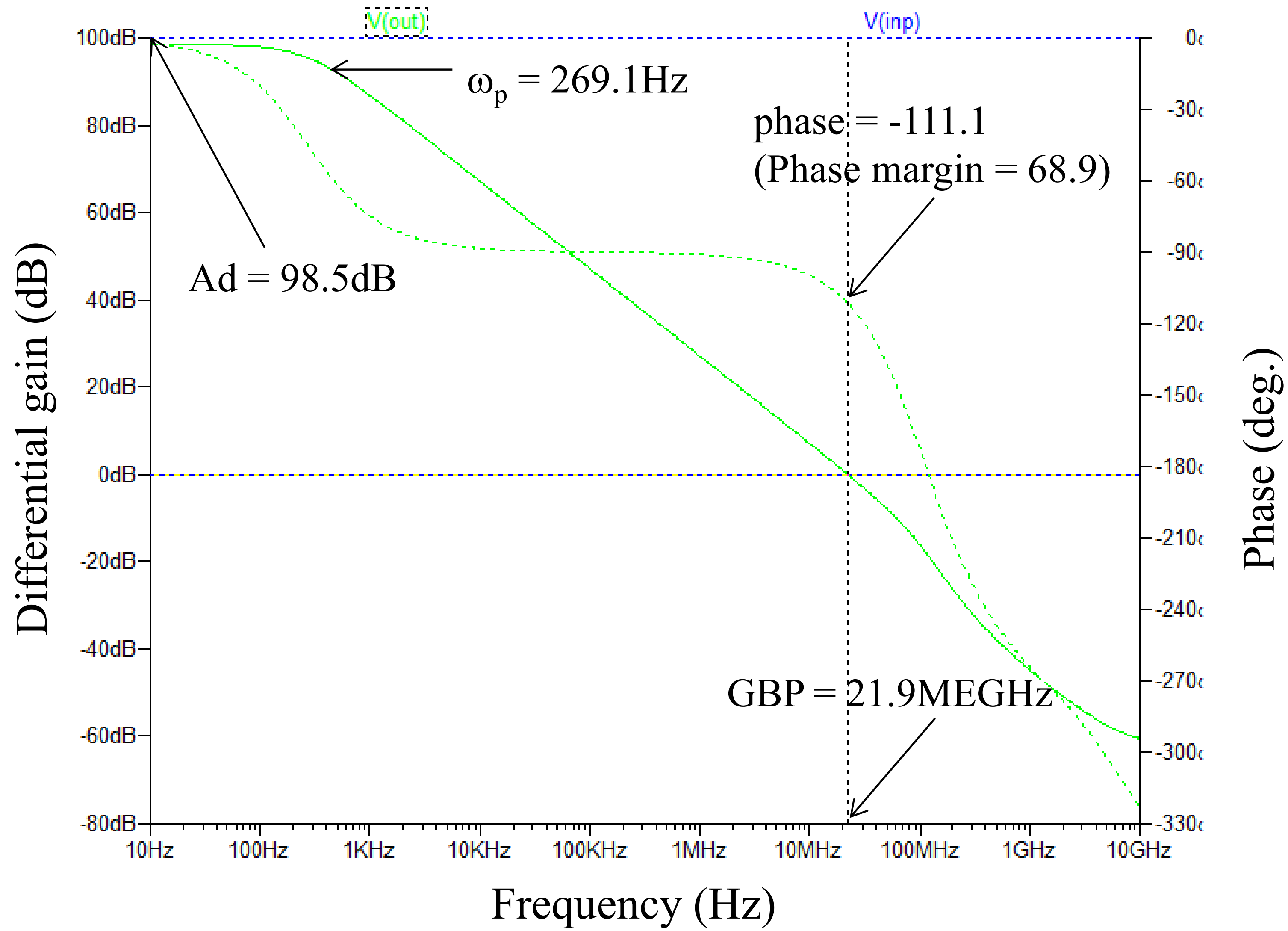


I(V1)
-132uA
-138uA
-144uA
-150uA
-156uA
-162uA
-168uA
-174uA
-180uA
-186uA
-192uA
Bias current (A)
Quiescent current = 189.9uA
V(out)
V(inp)
V(inn)
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
-1.0V
-1.5V
-2.0V
-2.5V
Output voltage (V)
Input- referred offset = -10.2uV
-200uV
-160uV
-120uV
-80uV
-40uV
0uV
40uV
80uV
120uV
160uV
200uV
Input voltage (V)

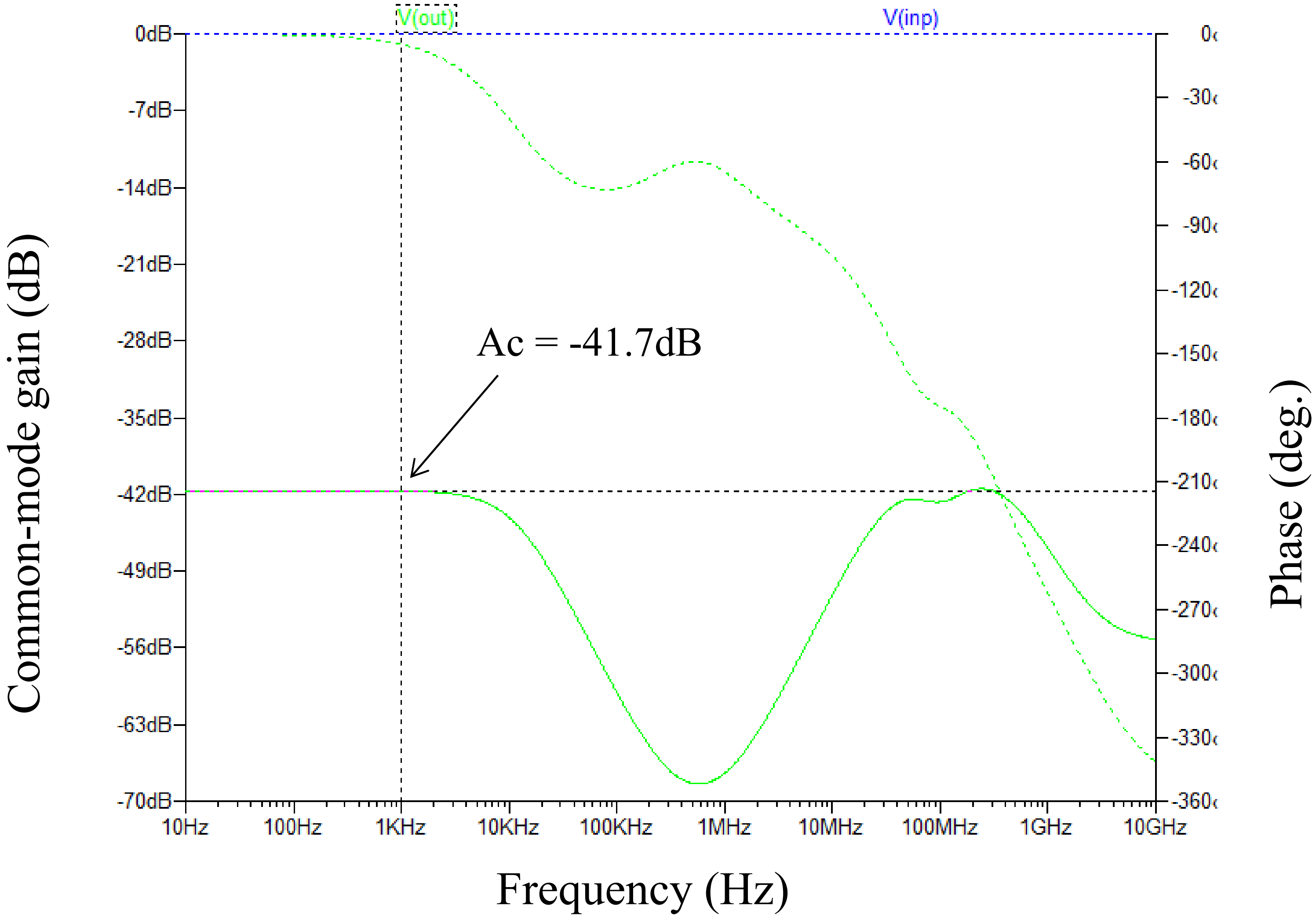
AC analysis


Independent Voltage Source - VD
Functions
(none)
PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)
SINE(Voffset Vamp Freq Td Theta Phi Ncycles)
EXP(V1 V2 Td1 Tau1 Td2 Tau2)
SFFM(Voff Vamp Fcar MDI Fsig)
PWL(t1 v1 t2 v2...)
PWL FILE:
Browse
Additional PWL Points
Make this information visible on schematic:
DC Value
DC value: -10.2uV
Make this information visible on schematic:
Small signal AC analysis(.AC)
AC Amplitude: 1V
AC Phase: 0
Make this information visible on schematic:
Parasitic Properties
Series Resistance[Ω]:
Parallel Capacitance[F]:
Make this information visible on schematic:
Cancel
OK

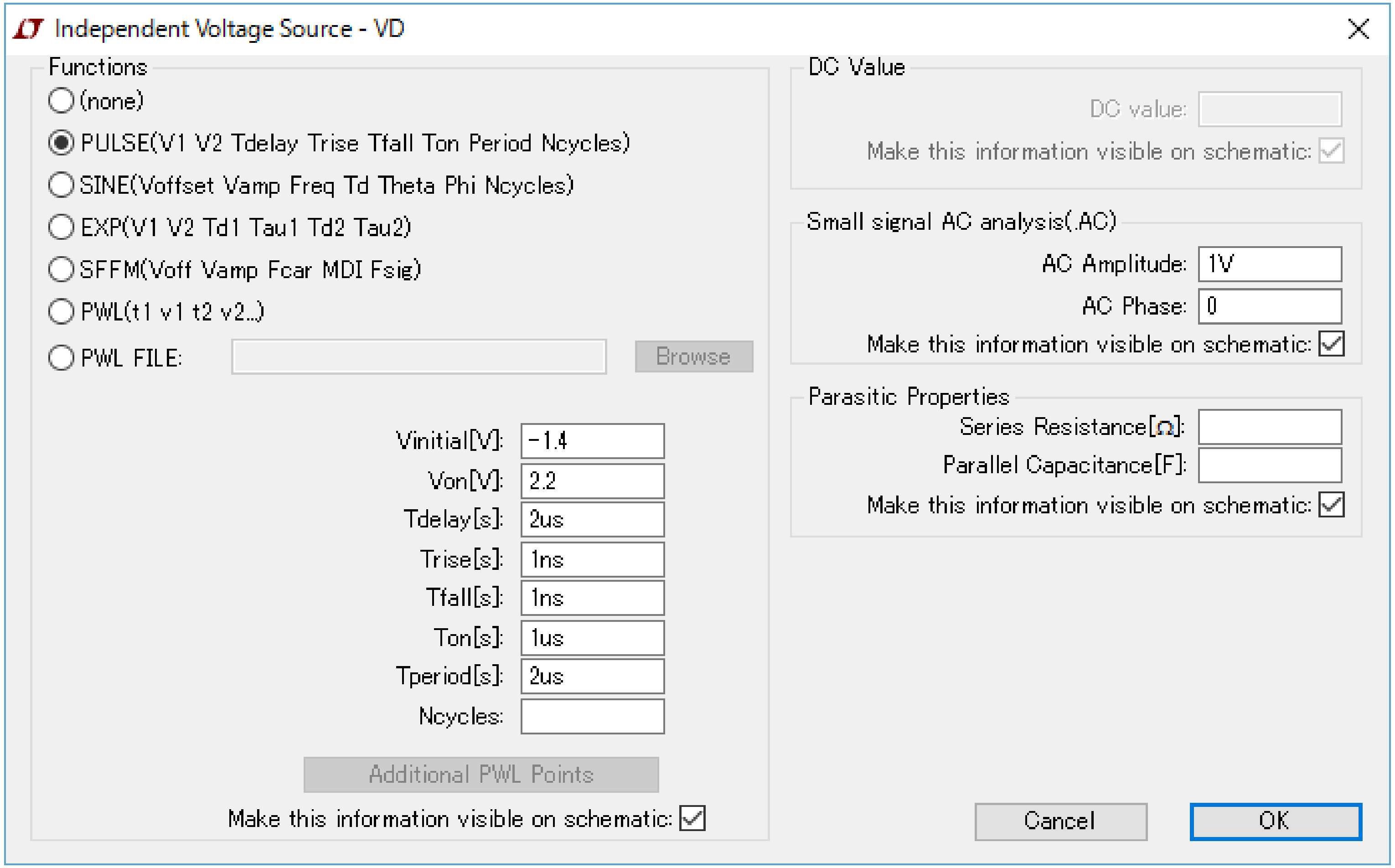
AC analysis - differential mode



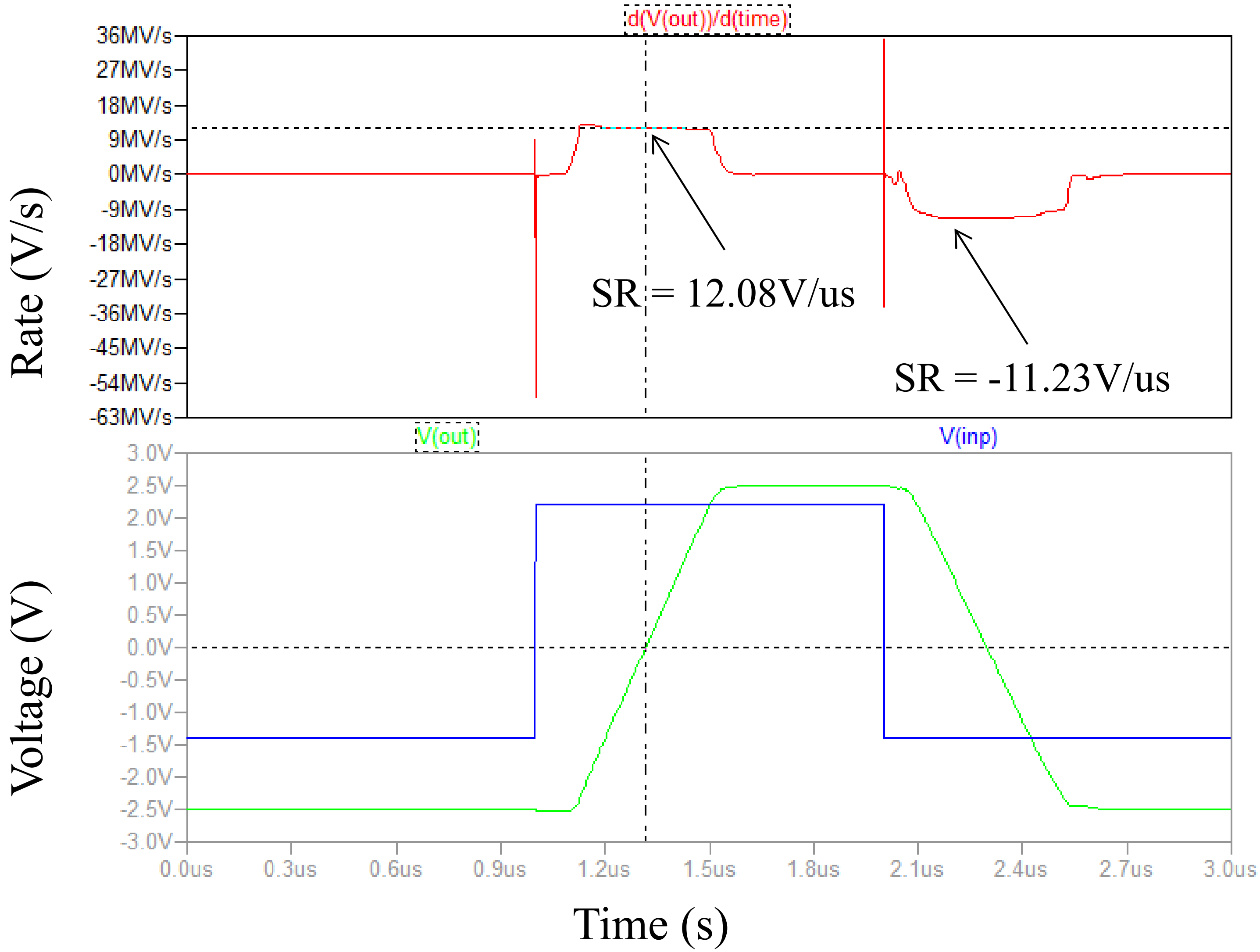
AC analysis - common mode



TRAN analysis



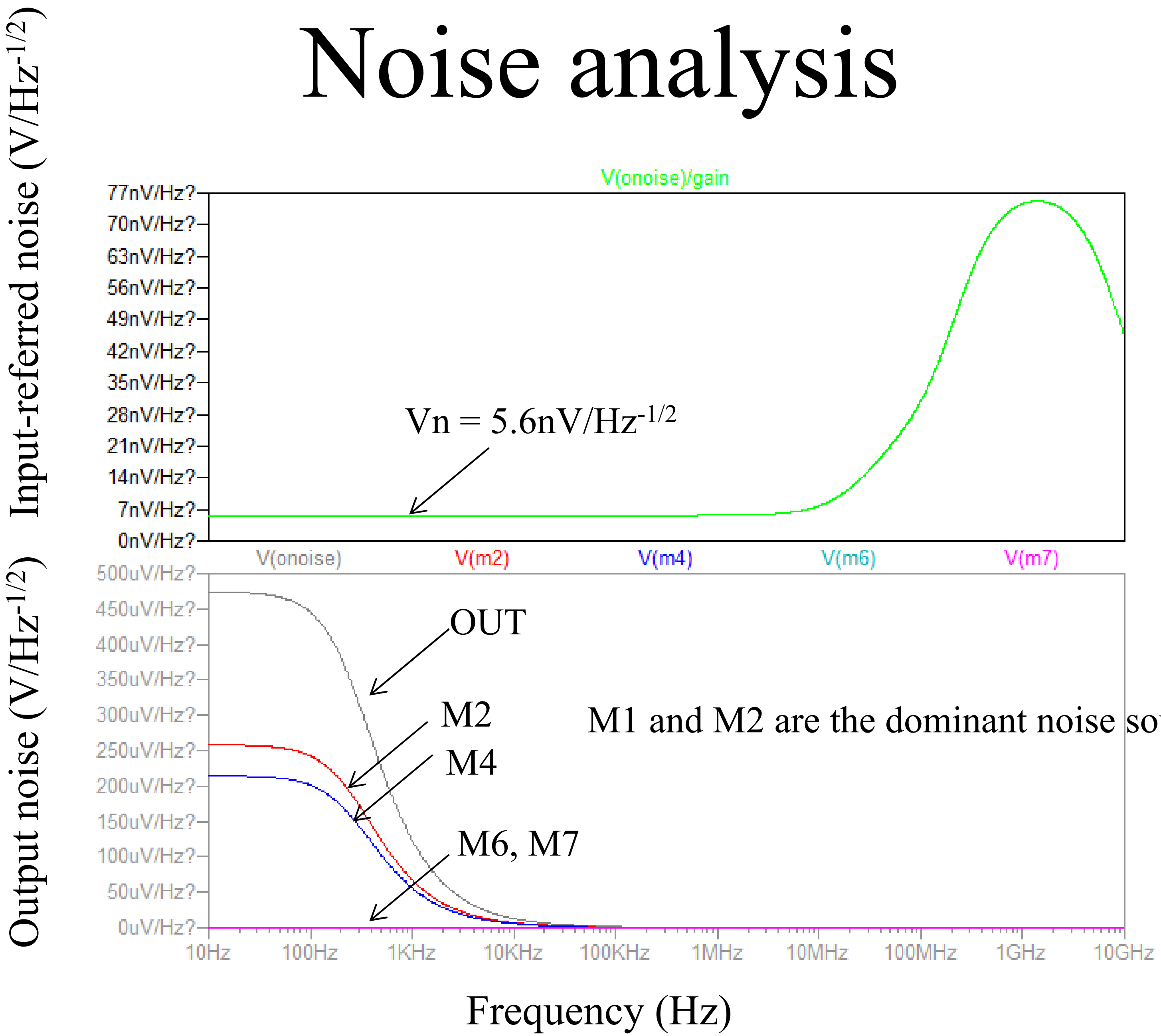
TRAN analysis - step response



Spacification estimated by the circuit simulation

Evaluation item	Unit	Value	Remarks
GBP	MEGHz	21.9	CL = 1.0pF
A_d	dB	98.5	@ 10Hz
Phase Margin	degree	68.9	
ω_p	Hz	269.1	
A_c	dB	-41.7dB	@ 1kHz
CMRR	dB	140.2	@ 1kHz
Slew Rate	V/us	11.23	CL = 1.0pF
Offset voltage	uV	-10.2	
Quiescent current	uA	189.9	

Noise analysis



M1 and M2 are the dominant noise sources.