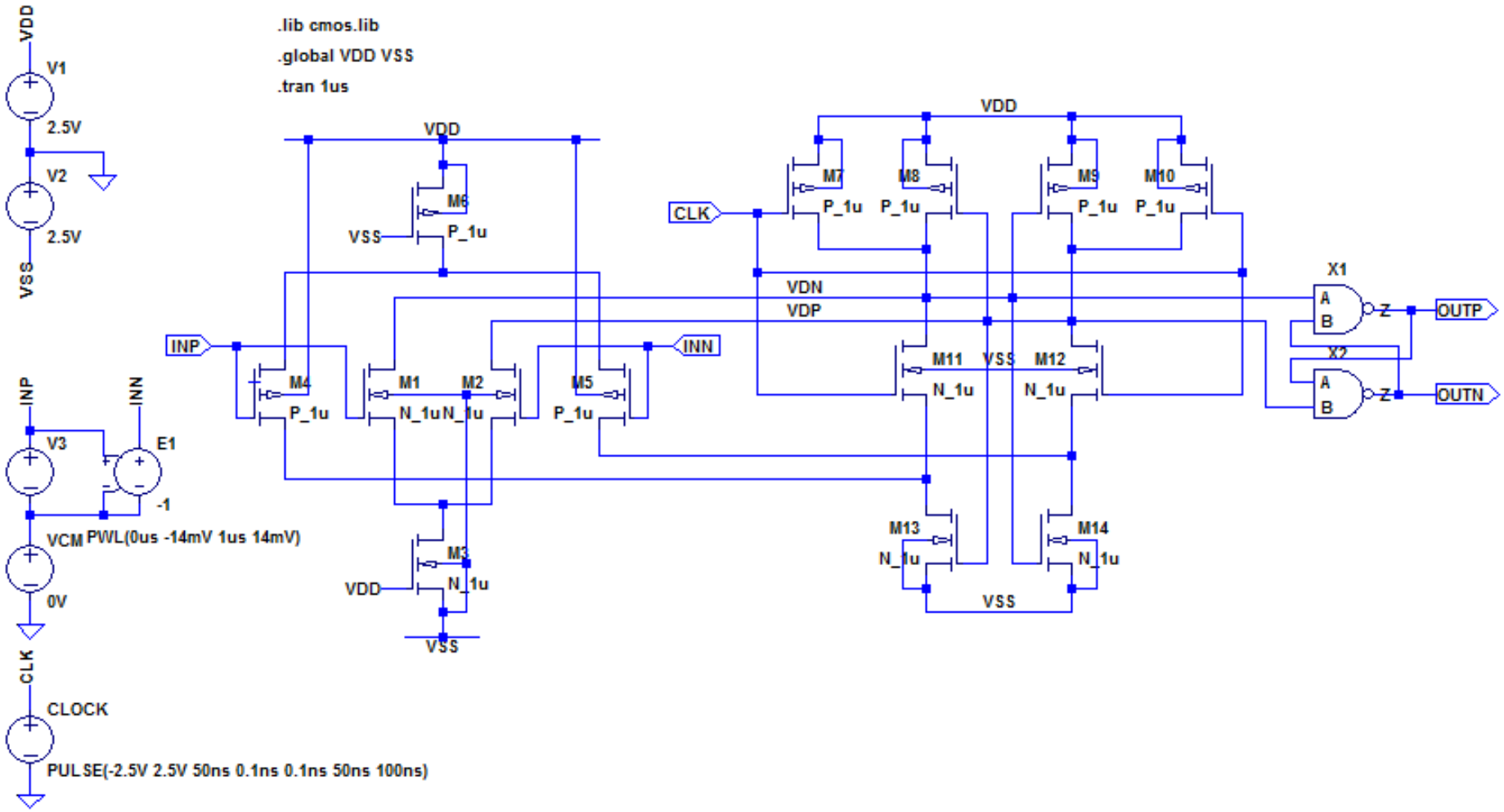
Lab. 15

CHARACTERIZATION OF CLOCKED COMPARATOR

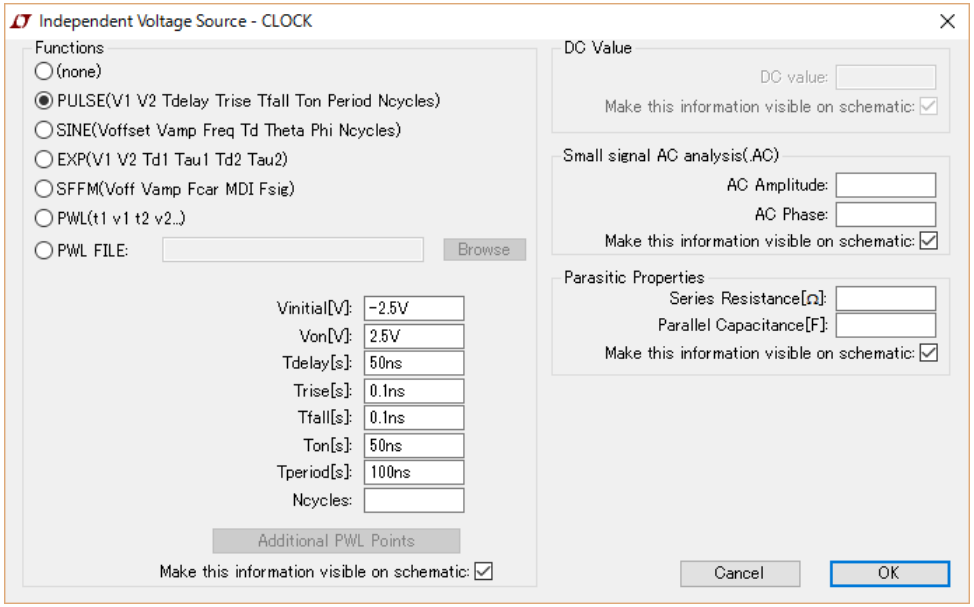
1. Characterization

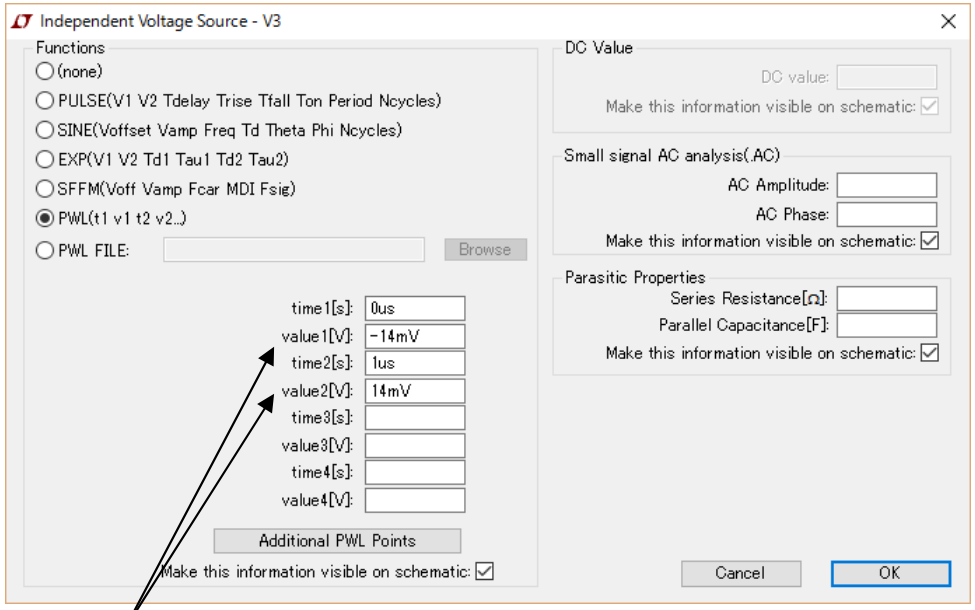
- Carry out the TRAN analysis of the clocked comparator and attach the simulation results to your report.
  - V(inp), V(inn), V(outp), V(vdn), V(vdp), and V(clk)
- Evaluate the comparison accuracy by simulation.
  - The accuracy depends on the clock frequency. Try to operate at f_{clk} = 10MHz (Tperiod = 100ns).
  - The accuracy depends on the common mode voltage too. Evaluate the comparison accuracy for VCM = -1.0V, 0.0V, and 1.0V.

Schematic


.lib cmos.lib
.global VDD VSS
.tran 1us
VDD
V1
2.5V
V2
2.5V
VSS
INP
INN
V3
E1
-1
VCM
PWL(0us -14mV 1us 14mV)
0V
CLK
CLOCK
PULSE(-2.5V 2.5V 50ns 0.1ns 0.1ns 50ns 100ns)
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
P_1u
N_1u
VDN
VDP
X1
X2
A
B
Z
OUTP
OUTN

Clock pulse and input voltage



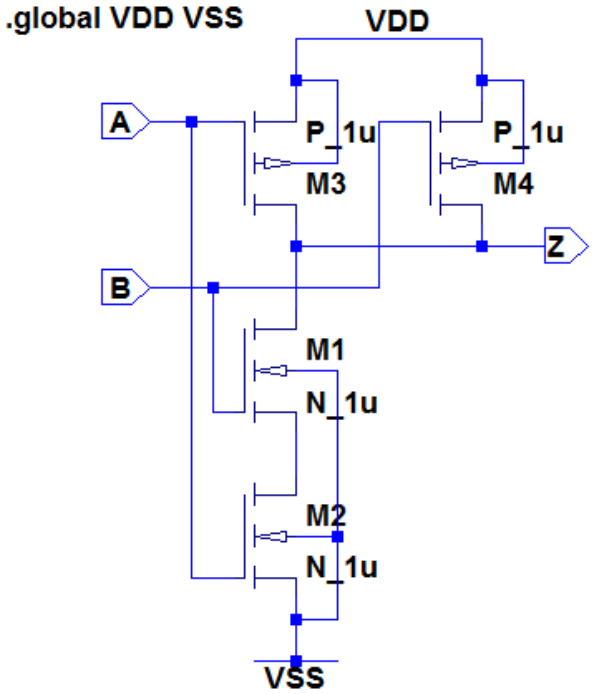


Change the Value1 and Value2 to evaluate the comparison accuracy.

MOSFET parameters

MOSFET	L(m)	W(m)	M	AD, AS(m^2)	PD, PS(m)	W/L
M1, M2	2u	10u	2	30p	16u	10
M3	4u	20u	2	60p	26u	10
M4, M5	2u	10u	6	30p	16u	30
M6	4u	20u	6	60p	26u	30
M7-M10	2u	10u	3	30p	16u	15
M11-M14	2u	10u	1	30p	16u	5

NAND2 schematic



MOSFET	L(m)	W(m)	M	AD, AS(m^2)	PD, PS(m)	W/L
M1, M2	1u	5u	4	15p	11u	5
M3, M4	1u	15u	1	45p	21u	15